1401 TIMING CHARTS

ARITHMETIC OPERATIONS

1 RESET ADD 0 (AAA)(BBB)
2 TRUE ADD
3 COMPLEMENT ADD-RECOMPLEMENT A (AAA)(BBB)
4 COMPLEMENT ADD-NO RECOMPLEMENT
5 COMPLEMENT ADD-ONE CHARACTER FIELD

MOVE, LOAD, COMPARE AND LOGIC OPERATIONS

6 MOVE M (AAA)(BBB)
7 MOVE DIGIT D (AAA)(BBB)
8 MOVE ZONE Y (AAA)(BBB)
9 MOVE ZERO SUPPRESS Z (AAA)(BBB)
10 LOAD L (AAA)(BBB)
11 CLEAR OP / (AAA)
12 WORD MARK CLEAR (AAA)(BBB)
13 WORD MARK SET (AAA)(BBB)
14 COMPARE C (AAA)(BBB)
15 HIGH-LOW-EQUAL COMPARE SEQUENCE C (AAA)(BBB)
16 BRANCH B (III), UNCONDITIONAL BRANCH
17 TEST AND BRANCH B (III) d (TEST ANY ONE OF TEN CHARACTER)
18 TEST CHARACTER AND BRANCH B (III)(BBB) d (ANY ONE OF NINE CHARACTERS)
19 TEST ZONE OR WORD MARK OR BOTH AND BRANCH V (III)(BBB) d
20 CLEAR AND BRANCH / (III)(BBB)
21 STOP AND BRANCH . (III)
22 STOP (.)
23 NO-OP (NO
24 EDIT OPERATION - ZERO SUPPRESS

ADVANCE PROGRAMMING

25 INSTRUCTION CYCLE WITH INDEXING
26 STORE A STAR Q (AAA) STORE B STAR H (AAA)
27 BRANCH B (III) ADVANCED PROGRAMMING (I-B STAR TRANSFER)
28 MOVE RECORD P (AAA)(BBB)

INPUT OUTPUT

29 READ
30 PUNCH

32 COLUMN BINARY READ SEQUENCE
33 COLUMN BINARY PUNCH SEQUENCE
34 MOVE AND UNSCRAMBLE COLUMN BINARY SEQUENCE
35 MOVE AND SCRAMBLE COLUMN BINARY SEQUENCE
36 PUNCH FEED READ SEQUENCE
37 STACKER SELECT K AND STACKER SELECT BRANCH

MAGNETIC TAPE

38 MOVE (LOAD) TAPE READ OPERATION
39 MOVE (LOAD) WRITE OPERATION
40 LOAD TAPE AND READ A WORD SEPARATOR CHARACTER
41 LOAD TAPE AND WRITE A WORD SEPARATOR CHARACTER
42 BACKSPACE TAPE OPERATION
43 ERASE TAPE OPERATION
44 WRITE TAPE MARK
45 REWIND TAPE OPERATION
46 REWIND AND UNLOAD TAPE
47 TAPE END OF FILE INDICATOR TEST AND TAPE TRANSMISSION ERROR TEST
48 MOVE COMPRESSED TAPE READ OPERATION
49 MOVE WITH ZERO INSERTION X (AAA)(BBB)

EXPANDED STORAGE

50 ADDRESS MODIFY TIMING # (AAA)(BBB)

Multiply
Divide

(900) ± ORIG A-FIELD
(901) 0 (458) (678) ORIG B-FIELD
(908) ≠

AB5 4 A2/3 6 2 5 B1 RESULTANT A-FIELD
FINAL RESULTANT B-FIELD 0 0 A2/2 6 6 5 AB5

CYCLE: 17 | A | B | A | B | A | B | B | B | I OP

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0
1		STORAGE ADDRESS REGISTER			32.35.XX.2	908	458	678	457	677	456	676	675	674	908
2		B-REGISTER	—	—	35.11.XX.2	WMC2	C41	CB1	C42	2	WMA2	C21	4	WM AB41	WM2 C
3		A-REGISTER	—	—	35.11.XX.2	8	045-075 C141	C142			WMA2	C82		C82	C82
4	-T	RESET ADD OP	01B1	A06A	35.24.11.2	OP DECODE A B 8 2 4 T									
5	-T	ARITH OPERATION	01B1	B23A	35.27.11.2	4									4
6	-T	GATED WORD MARK	01B2	C20C	31.07.11.2	B WM					A WM			B WM	
7	-T	I-E CHANGE	01B2	C22N	31.05.31.2	6								6	
8	+U	DELTA I CYCLE	01B2	E07N	31.21.11.2	7 9							7 14	DELTA CYC	LATCH GATE
9	-T	I-CYCLE LATCH	01B2	E23A	31.24.11.2	8								8	
10	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2	6 9									
11	+U	DELTA A-CYCLE	01B2	E07A	31.22.11.2	7 9		RESET 13 NOT 7		24					
12	-T	A-CYCLE LATCH	01B2	E23N	31.25.11.2		11					12			
13	-T	DELTA B-CYCLE LATCH	01B2	E13C	31.23.11.2		12							7	14
14	+U	B-CYCLE	01B2	D23N	31.26.11.2		13								
15	-T	FIRST B-CYCLE TRIGGER	01B3	E13N	34.31.13.2	5 6 9			14						
16	-T	B-REGISTER ZONE INHIBIT	01A3	D18C	35.18.21.2	9	12		12		12				9
17	-T	B-REGISTER DIGIT INHIBIT	01A3	D16A	35.18.31.2	9 NOT	MANUAL ENTRY 12		12		12				9
18	-T	B-REGISTER C-BIT INHIBIT	01A3	C11H	35.18.21.2	9 NOT	MANUAL ENTRY 12		12						
19	-T	B-REGISTER WORD MARK INHIBIT	01A3	C19C	35.18.21.2	NOT	MANUAL ENTRY								
20	-T	A-REGISTER DIGIT INHIBIT	01A3	B11G	35.18.41.2		4	NOT BLOCK	OPR AND B-CYCLE						
21	-T	ARITHMETIC ZONE INHIBIT	01A3	C05B	35.18.51.2		4	15 NOT BLOCK	OPR AND B-CYCLE						
22	+U	INHIBIT C-ZONE	01A3	C13H	35.15.11.2				4 14	NOT 15					
23	+U	A-WORD MARK LATCH	01B2	D15H	31.06.11.2						11 5				
24	+U	A-CYCLE ELIMINATE	01B2	C16 G	31.06.11.2						23				
25	-T	ARITHMETIC A-WORD MARK LATCH	01A3	B19H	35.18.61.2							14 5 NOT 15		9	
26	+U	A-REG SET 8-2-C	01A3	A18N	35.18.61.2						NOT	RECOMP 14	25 28		
27	+U	MODIFIER CONTROL ≠ 1	01A8	D06N	32.42.11.2										
28	+U	MODIFIER CONTROL - 1	01A8	B04H	32.42.11.2										
29	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2										
30	+U	MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX.2	909/908	457	677	456	676	455	675	674	673	909
31		DATA ON INHIBIT DRIVE LINES	—	—	—	WM2C	CAB41	CB41	C24	C24	WMA2	C2	C82	WM82	WMC2

FIGURE 1. RESET ADD 0 (AAA) (BBB)

(900) 4
(901) S 458 678
(908) 2

ORIGINAL A-FIELD A0 2 6 B5
ORIGINAL B-FIELD A1 9 8 A4

RESULTANT A-FIELD A0 2 6 B5
FINAL RESULTANT B-FIELD B2 2 4 A9

CYCLE: 1 7 | A | B | A | B | A | B | A | B | A | B | 1 OP

3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0

	SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC	1 7	A	B	A	B	A	B	A	B	A	B	1 OP
1	STORAGE ADDRESS REGISTER	—	—	32 35 XX 2	908	458	678	458	678	457	677	456	676	455	675	908
2	B-REGISTER	—	—	35.11.XX.2	C2	B41	CA4	B41	CA4	C42	8	2	CB1	CA82	A1	C2
3	A-REGISTER	—	—	35.11.XX.2	8	B41		B141		C142		2		CA182		CB2
4	-T SUBTRACT OP	01B1	B24P	35.26.11.2	OP DECODE A B 2 1 4 8											
5	-T ARITH OPERATION	01B1	B23A	35.27.11.2	4											7
6	-T GATED WM	01B2	C20C	31 07.11.2	B WM									A WM	B WM	
7	-T I-E CHANGE	01B2	C22N	31.05.31.2	6										16	
8	+U DELTA I CYCLE	01B2	E07N	31.21 11.2	7.9										7	
9	-T I-CYCLE LATCH	01B2	E23A	31.24.11.2	8											8
10	+U I-STAR RESTORE GATE	01A7	A20N	32.39.11.2	6.9											
11	+U DELTA A - CYCLE	01B2	E07A	31.22 11.2	7 9		NOT 7 RESET 13									
12	-T A-CYCLE LATCH	01B2	E23N	31.25 11.2	11											
13	-T DELTA B-CYCLE LATCH	01B2	E13C	31.23 11.2		12										
14	+U B-CYCLE	01B2	D23N	31 26.11.2		13										
15	-T FIRST B-CYCLE TRIGGER	01B3	E13N	34.31 13.2	5 6 9		14									
16	-T SECOND B-CYCLE TRIGGER	01B3	D13N	34.31.13.2			13 NOT 15		14							
17	-T B-REGISTER ZONE INHIBIT	01A3	D18C	35.18.21.2	8 NOT	MANUAL ENTRY				XFER B REG						
18	-T B-REGISTER DIGIT INHIBIT	01A3	F17P	35.18.31.2	8 NOT MANUAL ENTRY			XFER B REG								
19	-T B-REGISTER C-BIT INHIBIT	01A3	C11H	35.18.21.2	8 XFER B-REG											
20	-T B-REGISTER WORD MARK INHIBIT	01A3	C19C	35.18 21.2	NOT MANUAL	ENTRY										
21	-T ARITHMETIC ZONE INHIBIT	01A3	C05B	35.18.51.2										B WM 4 NOT 15 ORIG		
22	-T ARITHMETIC DIGIT INHIBIT	01A3	D16B	35.18 51.2			4 NOT 24									
23	+U INHIBIT C-ZONE	01A3	C13H	35.15.11.2					22 NOT 16	OR 21					21	
24	+U TRANSFER STAR	01B3	C20H	34.31 13.2	4 15	NOT 8	15									
25	-T ADDER CARRY	01B3	B09A	34 31.15 2												
26	-T CARRY TRIGGER	01B3	D26N	34.31.14.2						4	14 25 NOT	15 OR 16				NOT 25
27	+U ZONE ADDER GATE	01B3	F12A	34.33.11 2										B WM NOT 15		
28	+U MODIFIER CONTROL PLUS 1	01A8	D06N	32.42.11.2	8										8	
29	+U MODIFIER CONTROL MINUS 1	01A8	B04H	32.42 11.2			NOT 9 OR 30									
30	-T MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2	24		24									
31	+U MODIFIER OUTPUT ON BUS LINES	—	—	32 43.XX 2	909/908	458	678	457	677	456	676	455	675	454	674	909
32	DATA ON INHIBIT DRIVE LINES	—	—	—	C2	B41	CA4	B41	A81	C42	4	2	2	CA82	B2	C2

FIGURE 2. TRUE ADD

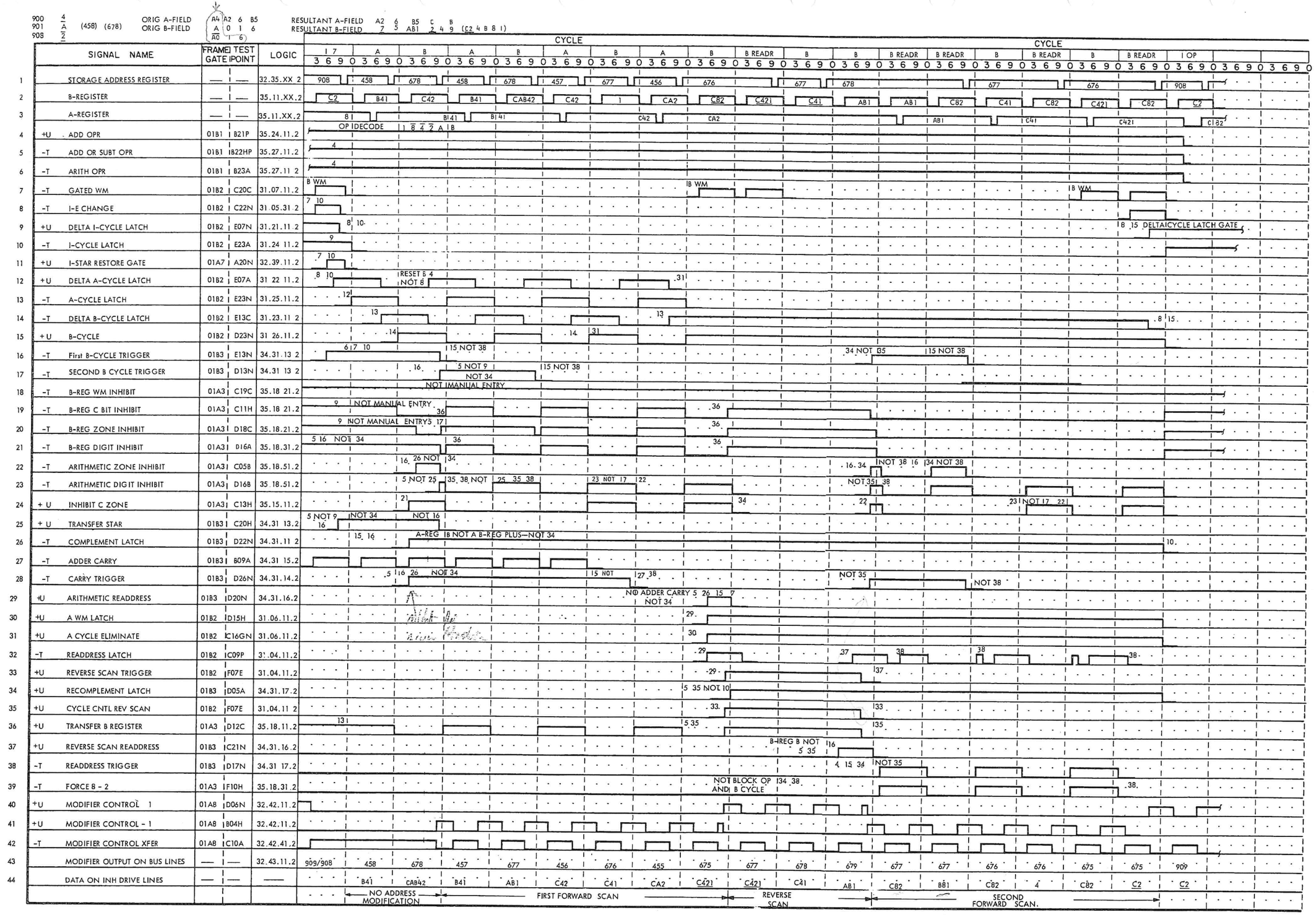


FIGURE 3. COMPLEMENT ADD-RECOMPLEMENT A (AAA) (BBB)

(900) 4
(901) A 458 678
(908) 2

ORIGINAL A-FIELD A2 6 B5
ORIGINAL B-FIELD A0 3 1 A6

RESULTANT A-FIELD A2 6 B5
FINAL RESULTANT B-FIELD 0 0 5 AB1

CYCLE: I 7 | A | B | A | B | A | B | A | B | A | B | 1 OP

3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC	
1		STORAGE ADDRESS REGISTER	—	—	32.35.XX.2	908 458 678 458 678 457 677 456 676 675 908
2		B-REGISTER	—	—	35.11.XX.2	C2 B41 A42 B41 CAB 42 C42 1 A2 C21 CA82 C2
3		A-REGISTER	—	—	35.11.XX.2	8 B41 B41 C42 A2 C82 C82
4	-T	ADD OPERATION	01B1	B21P	35.24.11.2	OP DECODE 1 2 4 8
5	-T	ARITH OPERATION	01B1	B23A	35.27.11.2	4 4
6	-T	GATED WORD MARK	01B2	C20C	31.07.11.2	B WM A WM B WM
7	-T	I-E CHANGE	01B2	C22N	31.05.31.2	6 6
8	+U	DELTA I CYCLE LATCH	01B2	E07N	31.21.11.2	79
9	-T	I-CYCLE LATCH	01B2	E23A	31.24.11.2	8
10	+U	DELTA A-CYCLE LATCH	01B2	E07A	31.22.11.2	7 9
11	-T	A-CYCLE LATCH	01B2	E23N	31.25.11.2	10
12	-T	DELTA B-CYCLE LATCH	01B2	E13C	31.23.11.2	11
13	+U	B-CYCLE	01B2	D23N	31.26.11.2	12
14	-T	FIRST B-CYCLE LATCH	01B3	E13N	34.31.13.2	5 6 9
15	-T	SECOND B-CYCLE LATCH	01B3	D13N	35.31.13.2	
16	-T	B-REGISTER ZONE INHIBIT	01A3	D18C	35.18.21.2	8 NOT MANUAL ENTRY
17	-T	B-REGISTER DIGIT INHIBIT	01A3	F17P	35.18.31.2	8 NOT MANUAL ENTRY XFER B REG
18	-T	B-REGISTER C-BIT INHIBIT	01A3	C11H	35.18.21.2	8 XFER B-REG
19	-T	B-REGISTER WORD MARK INHIBIT	01A3	C19C	35.18.21.2	NOT MANUAL ENTRY
20	-T	ARITHMETIC DIGIT INHIBIT	01A3	D16B	35.18.51.2	4 NOT 23
21	-T	ARITHMETIC ZONE INHIBIT	01A3	C05B	35.18.51.2	
22	+U	INHIBIT C-ZONE	01A3	C13H	35.15.11.2	
23	+U	TRANSFER STAR	01B3	C20H	34.31.13.2	4 14 NOT 8
24	+U	COMPLEMENT LATCH	01B3	D22H	34.31.11.2	
25	-T	ADDER CARRY	01B3	B09A	34.31.15.2	
26	-T	CARRY TRIGGER	01B3	D26N	34.31.14.2	
27	+U	A-WORD MARK LATCH	01B2	D15H	31.06.11.2	
28	+U	A-CYCLE ELIMINATE	01B2	C16GN	31.06.11.2	
29	-T	ARITHMETIC A-WORD MARK LATCH	01A3	B19H	35.18.61.2	
30		A-REGISTER SET 82 C	01A3	A18N	35.18.61.2	
31		MODIFIER CONTROL PLUS 1	01A8	D06N	32.42.11.2	
32		MODIFIER CONTROL MINUS 1	01A8	B04H	32.42.11.2	
33		MODIFIER CONTROL TRANSFER	01A8	C10A	32.42.41.2	
34		MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX.2	458 678 457 677 456 676 455 675 674 909
35		DATA ON INHIBIT DRIVE LINES	—	—	—	C2 B41 CAB 42 B41 AB1 C42 C41 A2 C82 82 C2

FIGURE 4. COMPLEMENT ADD-NO RECOMPLEMENT

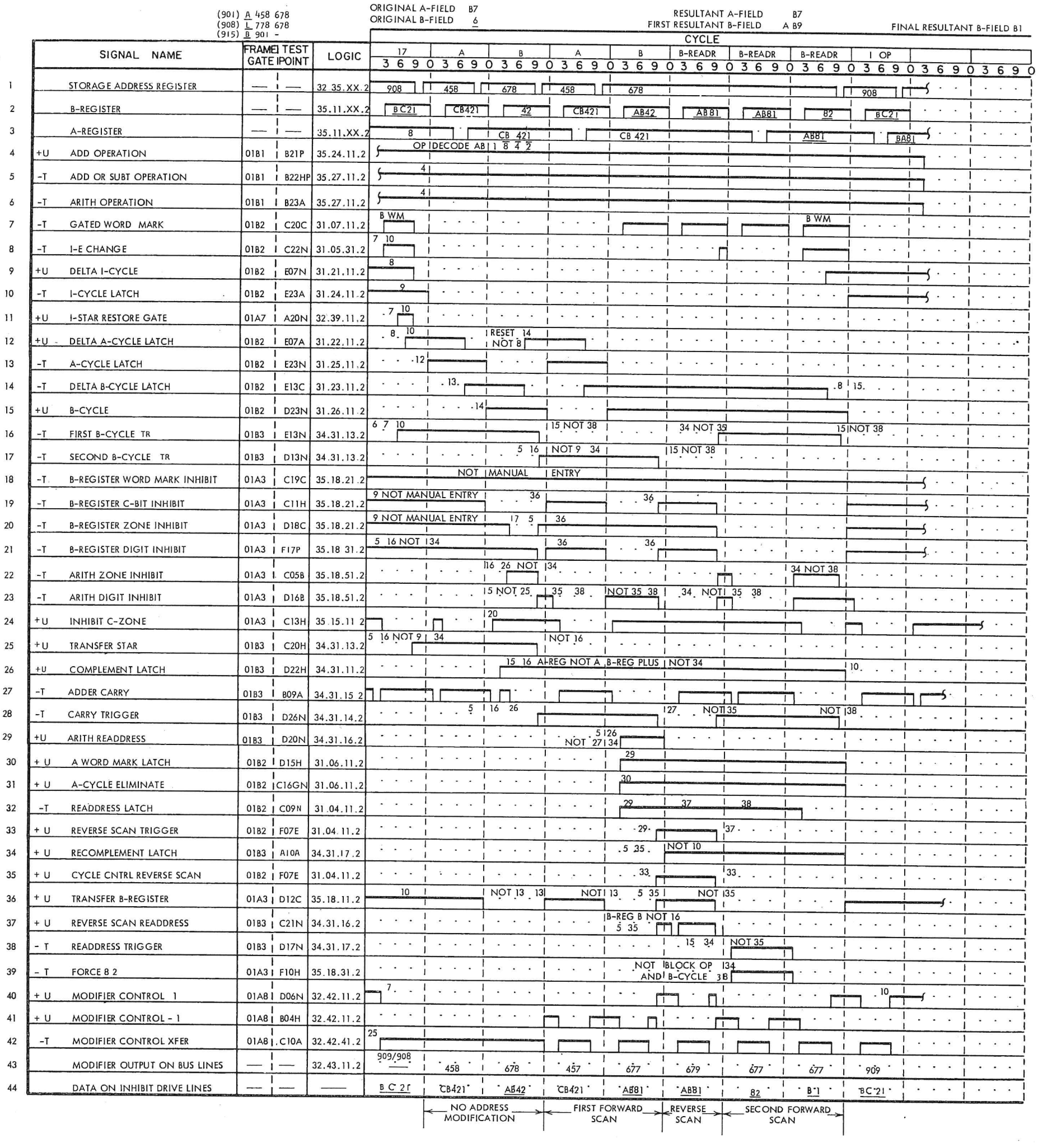


FIGURE 5. COMPLEMENT ADD-ONE CHARACTER FIELD

299 A
400 $\overline{M}$ (219) (319)
407 $\overline{S}$

ORIG A-FIELD DATA 4973
ORIG B-FIELD DATA 03965

RESULTANT A-FIELD 4973
RESULTANT B-FIELD 04973

CYCLE: 1 7 | A | B | A | B | A | B | A | B | 1 OP

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC	1 7	A	B	A	B	A	B	A	B	1 OP
						3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0
1		STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2	407	219	319	218	318	217	317	216	316	407
2		B-REGISTER LATCHES	—	—	35.XX.XX.2	$\overline{5}$	3	5	7	6	9	9	$\overline{4}$	$\overline{3}$	
3		A-REGISTER LATCHES	—	—	35.XX.XX.2		3		7		9		$\overline{4}$		
4	+U	MOVE OPERATION	01B1	B12N	35.25.11.2	OP DECODE B $\overline{A}$ 4 $\overline{8}$ $\overline{2}$ $\overline{1}$									
5	-T	GATED WORD MARK	01B2	C20C	31.07.11.2	B-WM							B-WM		
6	-T	I-E CHANGE	01B2	C22N	31.05.31.2	5 NO EXE ELIM 8							13 15	13 23	
7	+U	DELTA I-CYCLE	01B2	E07N	31.21.11.2	6 8								6 13 DELTA CYC LAT GATE	
8	-T	I-CYCLE LATCH	01B2	E23A	31.24.11.2	7	RESET CY LATS								
9	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2	5 8	ALTER								
10	+U	DELTA A-CYCLE	01B2	E07A	31.22.11.2	6 8	NOT A-CYCLE ELIM	RESET DELTA B			11 075				
11	-T	A-CYCLE LATCH	01B2	E23N	31.25.11.2	10				RESET CY LATS					
12	-T	DELTA B-CYCLE LATCH	01B2	E13C	31.23.11.2		075-105 11	075						6 13	
13	+U	B-CYCLE	01B2	D23N	31.26.11.2		12	GATE CY OUT			RESET CY LATS				
14	+U	TRANSFER B-REGISTER	01A3	E18H	35.18.11.2		11								
15	+U	I-E CONTROL 1	01B2	C16A	31.05.21.2	4									
16	-T	B-REG ZONE INHIBIT	01A3	D18C	35.18.21.2	14									
17	-T	B-REG DIGIT INHIBIT	01A3	F17P	35.18.31.2	14									
18	-T	B-REG C-BIT INHIBIT	01A3	C11H	35.18.21.2	14									
19	-T	B REG WM INHIBIT	01A3	C19C	35.18.21.2	14									
20	-T	A-REG ZONE INHIBIT	01A3	F20H	35.18.41.2		4	NOT BLOCK	OPR & B-CYCLE						
21	-T	A-REG DIGIT INHIBIT	01A3	B11G	35.18.41.2		4	NOT BLOCK	OPR & B-CYCLE						
22	+U	A-REG DIGIT AND ZONE C BIT GEN TAKES OVER													
23	+U	A-REG WM LATCH	01B2	D15H	31.06.11.2								5	090—000	8
24	+U	MODIFIER CONTROL - 1	01A8	B04H	32.42.11.2										
25	+U	MODIFIER CONTROL 1	01A8	D06N	32.42.11.2									26	
26	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2										
27		MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX.2		218	318	217	317	216	316	215	315	408
28		DATA ON INHIBIT DRIVE LINES	—	—	—		3	3	7	7	9	9	$\overline{4}$	4	
	+U	INHIBIT DRIVE C	01A3	E15B	35.17.11.2										

FIGURE 6. MOVE M (AAA) (BBB)

599 A ORIG A-FIELD CHAR C-B-A-8-4
600 D (407) (507) ORIG B-FIELD CHAR WM-B-2
607 A

RESULTANT B-FIELD CHAR WM-C-B-8-4

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC	CYCLE: 1 7 (3 6 9 0)	A (3 6 9 0)	B (3 6 9 0)	1 OP (3 6 9 0)	(3 6 9 0)	(3 6 9 0)	(3 6 9 0)	(3 6 9 0)	(3 6 9 0)	(3 6 9 0)	(3 6 9 0)
1		STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2	090-105 607	407	507	607							
2		B-REGISTER LATCHES	—	—	35.XX.XX.2	025-STROBE 000-015	CBA 84	WM B2	A							
3		A-REGISTER LATCHES	—	—	35.XX.XX.2											
4	+U	MOVE DIGIT OP	01B1	A12N	35.24.11.2	OP DECODE A B 4 8 2 1										
5	-T	GATED WORD MARK	01B2	C20C	31.07.11.2	B-WM										
6	-T	I-E CHANGE	01B2	B13H	31.05.31.2	5 NO EXE ELIM 8		13 14								
7	+U	DELTA I-CYCLE	01B2	E07N	31.21.11.2	6	DELTA CYC 6	B-CYC	LATCH CNTL 1							
8	-T	I-CYCLE	01B2	A23F	31.24.11.2	7	000-015 DELTA PROCESS									
9	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2	5	I-CYCLE									
10	+U	DELTA A-CYCLE	01B2	E07A	31.22.11.2	6 8	NOT A CYCLE ELIM 11 075									
11	-T	A-CYCLE	01B2	E17F	31.25.11.2	10	000-060	000-015 DELTA PROCESS								
12	-T	DELTA B-CYCLE	01B2	E15H	31.23.11.2		075-105 A-CYC		13							
13	+U	B-CYCLE	01B2	D23N	31.26.11.2		12	000-060	000-015 DELTA PROCESS							
14	+U	1 CHAR I-E CHANGE	01B2	C08G	31.05.11.2	4										
15	+U	TRANSFER B-REGISTER	01A3	E18H	35.18.11.2		8/11									
16	-T	B-REG ZONE INHIBIT	01A3	D18C	35.18.21.2	4										
17	-T	B-REG DIGIT INHIBIT	01A3	F17P	35.18.31.2		15									
18	-T	B-REG C-BIT INHIBIT	01A3	C11H	35.18.21.2		15									
19	-T	B-REG WM INHIBIT	01A3	C19C	35.18.21.2	15										
20	-T	A-REG DIGIT INHIBIT	01A3	B11G	35.18.41.2		NOT BLOCK OPR AND B-CYCLE 4									
21	+U	MODIFIER CONTROL - 1	01A8	B04H	32.42.11.2											
22	+U	MODIFIER CONTROL + 1	01A8	D06N	32.42.11.2											
23	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2											
24		MODIFIER OUTPUT ON BUS LINES	—	—	32.42.XX.2		406	506	608							
25		DATA ON INHIBIT DRIVE LINES	—	—	—	7	C-B-A-8-4	WM-C-B-8-4	A							

FIGURE 7. MOVE DIGIT D (AAA) (BBB)

599 $\overline{A}$
600 $\overline{Y}$ (407) (507) ORIG A-FIELD CHAR C-B-A-8-4
607 $\overline{A}$ ORIG B-FIELD CHAR WM-B-2

RESULTANT B-FIELD CHAR WM-C-B-A-2

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1		STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2
2		B-REGISTER LATCHES	—	—	35.XX.XX.2
3		A-REGISTER LATCHES	—	—	35.XX.XX.2
4	+U	MOVE ZONE OP	01B1	C12N	35.26.11.2
5	-T	GATED WORD MARK	01B2	C20C	31.07.11.2
6	-T	I-E CHANGE	01B2	B13H	31.05.31.2
7	+U	DELTA I-CYCLE	01B2	E07N	31.21.11.2
8	-T	I-CYCLE	01B2	A23F	31.24.11.2
9	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2
10	+U	DELTA A-CYCLE	01B2	E07A	31.22.11.2
11	-T	A-CYCLE	01B2	E17F	31.25.11.2
12	-T	DELTA B-CYCLE	01B2	E15H	31.23.11.2
13	+U	B-CYCLE	01B2	D23N	31.26.11.2
14	+U	1 CHAR I-E CHANGE	01B2	C08G	31.05.11.2
15	+U	TRANSFER B-REGISTER	01A3	E18H	35.18.11.2
16	-T	B-REG ZONE INHIBIT	01A3	D18C	35.18.21.2
17	-T	B-REG DIGIT INHIBIT	01A3	F17P	35.18.31.2
18	-T	B-REG C-BIT INHIBIT	01A3	C11H	35.18.21.2
19	-T	B-REG WM INHIBIT	01A3	C19C	35.18.21.2
20	-T	A-REG ZONE INHIBIT	01A3	F20H	35.18.41.2
21	+U	MODIFIER CONTROL - 1	01A8	B04H	32.42.11.2
22	+U	MODIFIER CONTROL + 1	01A8	D06N	32.42.11.2
23	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2
24		MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX.2
25		DATA ON INHIBIT DRIVE LINES	—	—	—

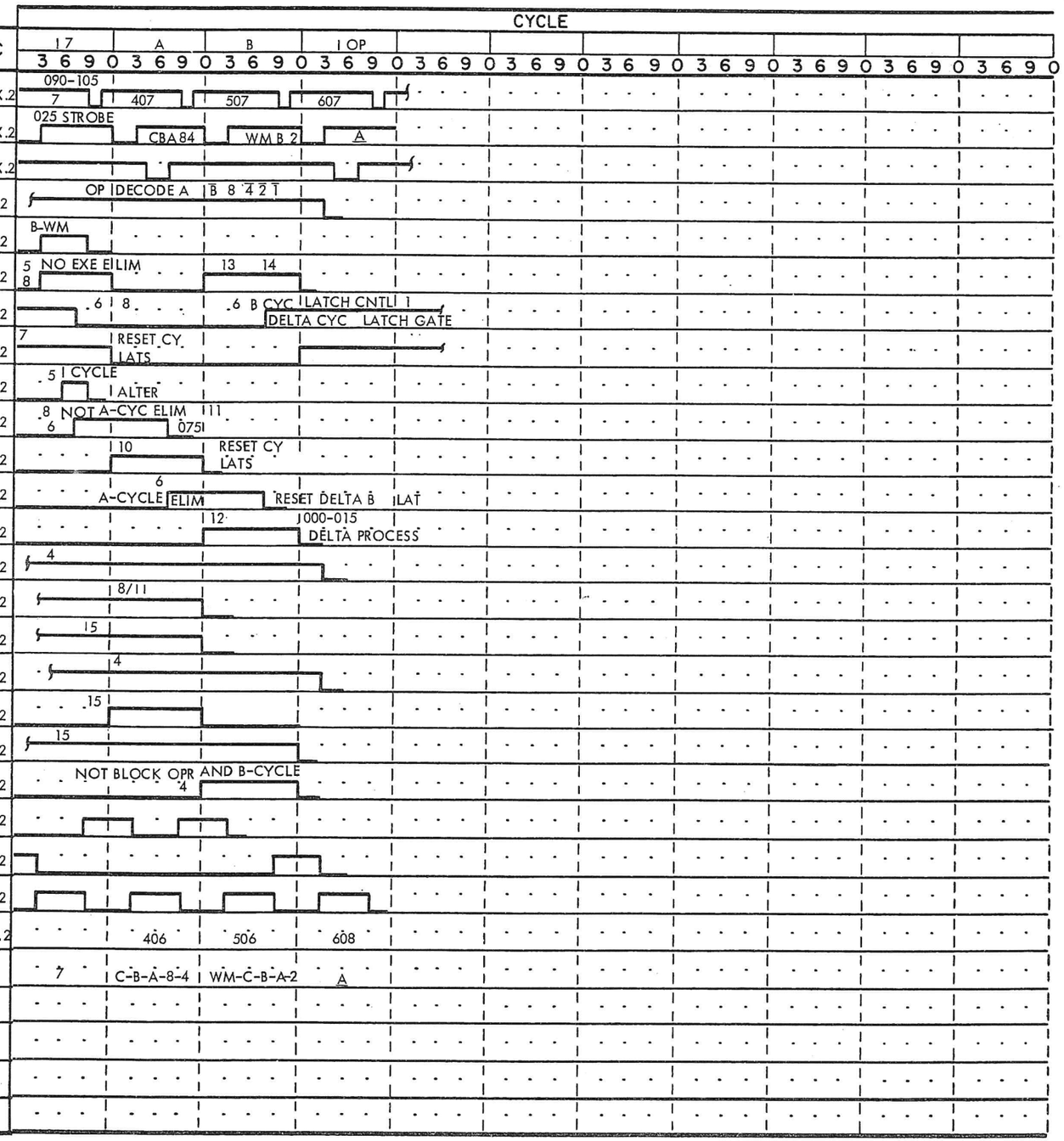


FIGURE 8. MOVE ZONE Y (AAA) (BBB)

700 Z 809 419
707 M 519 419
714 B 700 -

A-FIELD DATA 007601
B-FIELD DATA bbbbbb

RESULTANT A-FIELD (BEFORE ZERO SUPP - AFTER MOVE) 007601
RESULTANT B-FIELD (BEFORE ZERO SUPP - AFTER MOVE) 00760b

RESULTANT B-FIELD (AFTER ZERO SUPP) bb7601

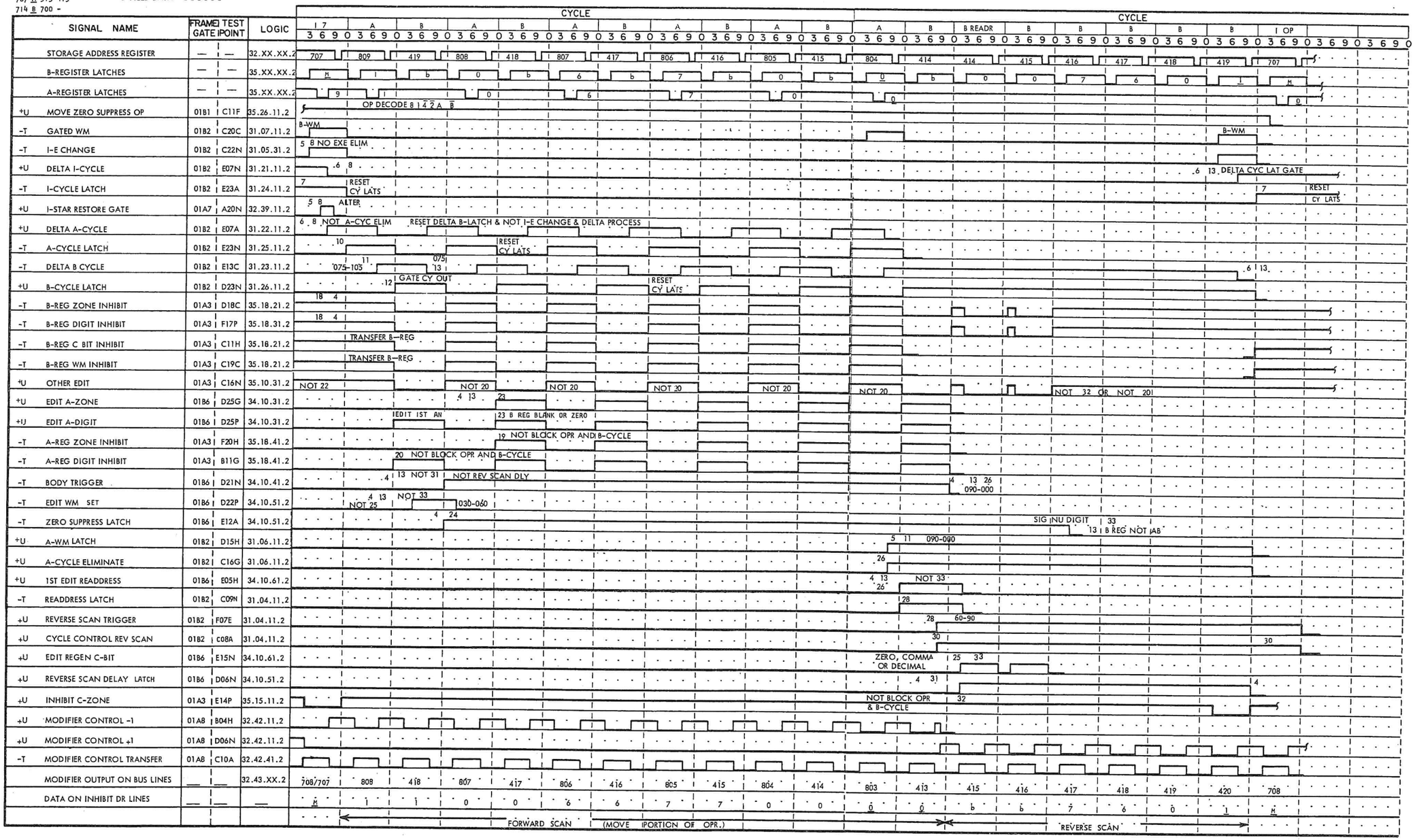


FIGURE 9. MOVE ZERO SUPPRESS Z (AAA) (BBB)

899 S
900 L (409) (509)
907 A

ORIGINAL A-FIELD DATA 4 9 7 3
ORIGINAL B-FIELD DATA 0 3 9 6 5

RESULTANT B-FIELD 0 4 9 7 3

CYCLE: I 7 | A | B | A | B | A | B | A | B | I OP

		SIGNAL NAME	FRAME	TEST GATE POINT	LOGIC	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0	3 6 9 0
1		STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2	907	409	409	408	508	407	507	406	506	
2		B-REGISTER LATCHES	—	—	.XX.2	A	3	9	7	6	9	9	4	3	
3		A-REGISTER LATCHES	—	—	35.XX.XX.2		3		7		9		4		
4	+U	LOAD OPERATION	01B1	B11F	35.25.11.2	OP DECODE B Ā 1 2 4 8									
5	-T	GATED WORD MARK	01B2	C20C	31.07.11.2	B-WM							B-WM 11		
6	-T	I-E CHANGE	01B2	C22N	31.05.31.2	5 8 NO EXE ELIM							13	16 26	
7	+U	DELTA I-CYCLE	01B2	E07N	31.21.11.2	6	8						6 B CY LAT CTRL 1	DELTA CYC LAT GATE	
8	-T	I-CYCLE	01B2	A23F	31.24.11.2	7	RESET CYCLE LATCHES							7	
9	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2	5 8	NOT ALTER								
10	+U	DELTA A-CYCLE	01B2	E07A	31.22.11.2	6	8 NOT A CYC ELIM		RESET DELTA B LATCH		11 075				
11	-T	A-CYCLE	01B2	E21P	31.25.11.2	10		10		RESET CYCLE LATCHES					
12	-T	DELTA B-CYCLE	01B2	E15H	31.23.11.2		075-10 11	075 13						6	13
13	+U	B-CYCLE	01B2	D23N	31.26.11.2		12	GATE CY OUT			RESET CY LATCHES				
14	+U	TRANSFER A-REGISTER	01A3	D12G	35.18.41.2		4 NOT BLOCK OPR AND B CYCLE								
15	+U	TRANSFER B-REGISTER	01A3	E18H	35.18.11.2	11									
16	+U	I-E CONTROL 1	01B2	C16A	31.05.21.2	4									
17	+U	I-E CONTROL 2	01B2	C16B	31.05.21.2	4									
18	-T	B-REG ZONE INHIBIT	01A3	D18C	35.18.21.2	15									
19	-T	B-REG DIGIT INHIBIT	01A3	F17P	35.18.31.2	15									
20	-T	B-REG C-BIT INHIBIT	01A3	C11H	35.18.21.2	15									
21	-T	B-REG WM INHIBIT	01A3	C19C	35.18.21.2		SUPPRESSED BY 4								
22	-T	A-REG ZONE INHIBIT	01A3	F20H	35.18.41.2		4	NOT BLOCK OPR AND B- CYCLE							
23	-T	A-REG DIGIT INHIBIT	01A3	B11G	35.18.41.2		4	NOT BLOCK OPR AND B- CYCLE							
24	+U	INHIBIT C	01A3	E12C	35.14.11.2		14	A REG C							
25	+U	INHIBIT DRIVE WM	01A3	E13C	35.14.51.2		14	A REG WM							
26	+U	A-WORD MARK LATCH	01B2	D15H	31.06.11.2								5	11	8
27	+U	MODIFIER CONTROL - 1	01A8	B04H	32.42.11.2										
28	+U	MODIFIER CONTROL + 1	01A8	D06N	32.42.11.2										
29	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2										
30		MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX.2		408	508	407	507	406	506	405	505	
31		DATA ON INHIBIT DRIVE LINES	—	—	—		3	3	7	7	9	9	4	4	

FIGURE 10. LOAD L (AAA) (BBB)

899 2
900 7 (404)
904 A

ORIG B-FIELD 73487
RESULTANT B-FIELD bbbbb

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1		STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2
2		B-REGISTER LATCHES	—	—	35.XX.XX.2
3		A-REGISTER LATCHES	—	—	35.XX.XX.2
4	+U	CLEAR OPERATION	01B1	C13N	35.26.11.2
5	-T	GATED WORD MARK	01B2	C20C	31.07.11.2
6	-T	I-E CHANGE	01B2	C22N	31.05.31.2
7	+U	DELTA I-CYCLE	01B2	E07N	31.21.11.2
8	-T	I-CYCLE	01B2	A23F	31.24.11.2
9	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2
10	-T	DELTA B-CYCLE	01B2	E15H	31.23.11.2
11	+U	B-CYCLE	01B2	D23N	31.26.11.2
12	-T	B-REG ZONE INHIBIT	01A3	D18P	35.18.21.2
13	-T	B-REG DIGIT INHIBIT	01A3	F17P	35.18.31.2
14	-T	FIRST ROW	01A3	E16H	35.15.11.2
15	-T	B-REG WM INHIBIT	01A3	C19C	35.18.21.2
16	+U	A-CYCLE ELIM	01B2	D16D	31.06.11.2
17	+U	UNITS BORROW-CARRY	01A8	D03P	32.42.31.2
18	+U	TENS BORROW-CARRY	01A8	D03C	32.42.31.2
19	+U	MODIFIER CONTROL - 1	01A8	B04H	32.42.11.2
20	+U	MODIFIER CONTROL + 1	01A8	D06N	32.42.11.2
21	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2
22		MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX.2
23		DATA ON INHIBIT DRIVE LINES	—	—	—

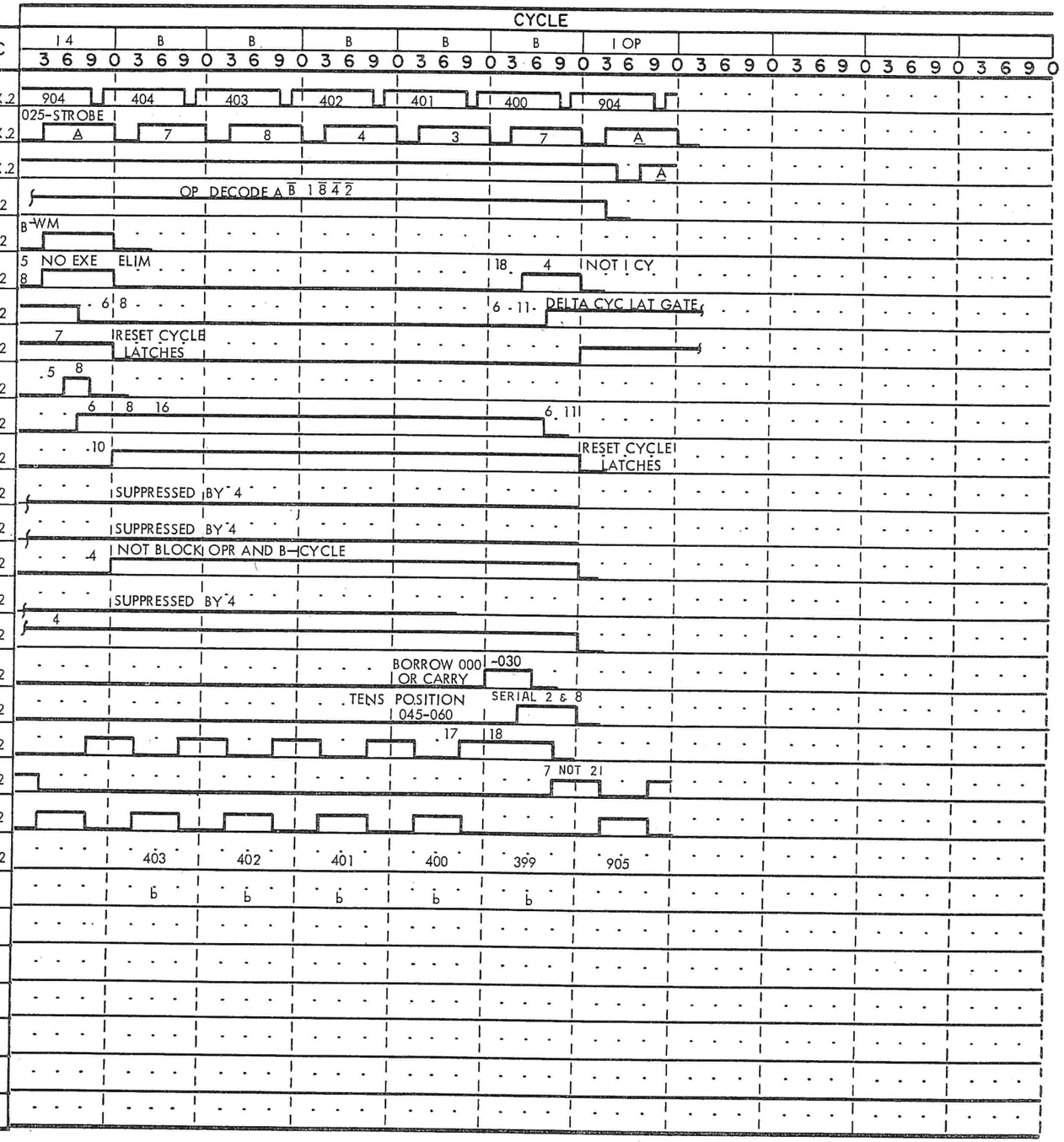


FIGURE 11. CLEAR OP / (AAA)

899 S
900 ◇ (409) (509) ORIG A-FIELD 8 RESULTANT A-FIELD 8
907 A ORIG B-FIELD B RESULTANT B-FIELD B

		SIGNAL NAME	FRAME	TEST GATE	TEST POINT	LOGIC
1		STORAGE ADDRESS REGISTER	—	—		32.XX.XX.2
2		B-REGISTER LATCHES	—	—		35.XX.XX.2
3		A-REGISTER LATCHES	—	—		35.XX.XX.2
4	+U	WORD MARK CLEAR	01B1	A14N		35.24.11.2
5	-T	GATED WORD MARK	01B2	C20C		31.07.11.2
6	-T	I-E CHANGE	01B2	B13H		31.05.31.2
7	+U	DELTA I-CYCLE	01B2	E07N		31.21.11.2
8	-T	I-CYCLE	01B2	A23F		31.24.11.2
9	+U	I-STAR RESTORE GATE	01A7	A20N		32.39.11.2
10	+U	DELTA A-CYCLE	01B2	E07A		31.22.11.2
11	-T	A-CYCLE	01B2	E17F		31.25.11.2
12	-T	DELTA B-CYCLE	01B2	E15H		31.23.11.2
13	+U	B-CYCLE	01B2	D23N		31.26.11.2
14	+U	B-REG TRANSFER DIGIT AND ZONE	01A3	D15C		35.18.11.2
15	+U	1 CHAR I-E CHANGE	01B2	C08G		31.05.11.2
16	-T	B-REG ZONE INHIBIT	01A3	D19A		35.18.21.2
17	-T	B-REG DIGIT INHIBIT	01A3	D16A		35.18.31.2
18	-T	B-REG WM INHIBIT	01A3	C19C		35.18.21.2
19	+U	MODIFIER CONTROL -1	01A8	B04H		32.42.11.2
20	+U	MODIFIER CONTROL +1	01A8	D06N		32.42.11.2
21	-T	MODIFIER CONTROL XFER	01A8	C10A		32.42.41.2
22		MODIFIER OUTPUT ON BUS LINES	—	—		32.43.XX.2
23		DATA ON INHIBIT DRIVE LINES	—	—		—

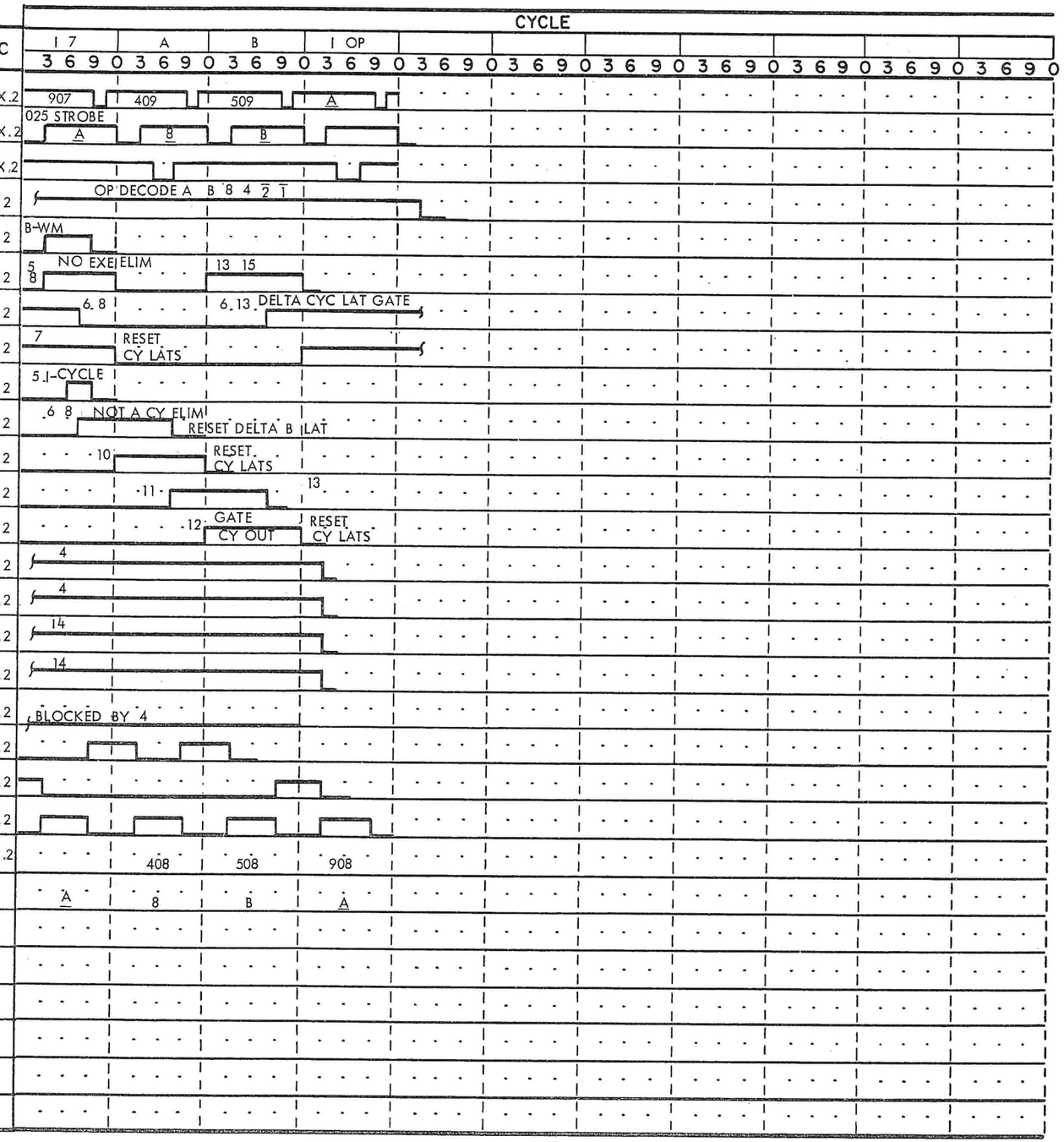


FIGURE 12. WORD MARK CLEAR (AAA) (BBB)

899 S
900 , (409) (509)
907 A

ORIG A-FIELD DATA
ORIG B-FIELD DATA

8 RESULTANT A-FIELD 8
B RESULTANT B-FIELD B

CYCLE: 1 7 | A | B | 1 OP

3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1		STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2
2		B-REGISTER LATCHES	—	—	35.XX.XX.2
3		A-REGISTER LATCHES	—	—	35.XX.XX.2
4	+U	WORD MARK SET	01B1	B14F	35.26.11.2
5	-T	GATED WORD MARK	01B2	C20C	31.07.11.2
6	-T	I-E CHANGE	01B2	B13H	31.05.31.2
7	+U	DELTA I-CYCLE	01B2	E07N	31.21.11.2
8	-T	I-CYCLE	01B2	A23F	31.24.11.2
9	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2
10	+U	DELTA A-CYCLE	01B2	E07A	31.22.11.2
11	-T	A-CYCLE	01B2	E17F	31.25.11.2
12	-T	DELTA B-CYCLE	01B2	E15H	31.23.11.2
13	+U	B-CYCLE	01B2	D23N	31.26.11.2
14	+U	B-REG TRANSFER DIGIT AND ZONE	01A3	D15C	35.18.11.2
15	+U	1 CHAR I-E CHANGE	01B2	C08G	31.05.11.2
16	-T	B-REG ZONE INHIBIT	01A3	D19A	35.18.21.2
17	-T	B-REG DIGIT INHIBIT	01A3	D16A	35.18.31.2
18	+U	INHIBIT DRIVE WORD MARK	01A3	E15A	35.14.51.2
19	+U	MODIFIER CONTROL - 1	01A3	B04H	32.42.11.2
20	+U	MODIFIER CONTROL + 1	01A8	D06N	32.42.11.2
21	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2
22		MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX.2
23		DATA ON INHIBIT DRIVE LINES	—	—	—

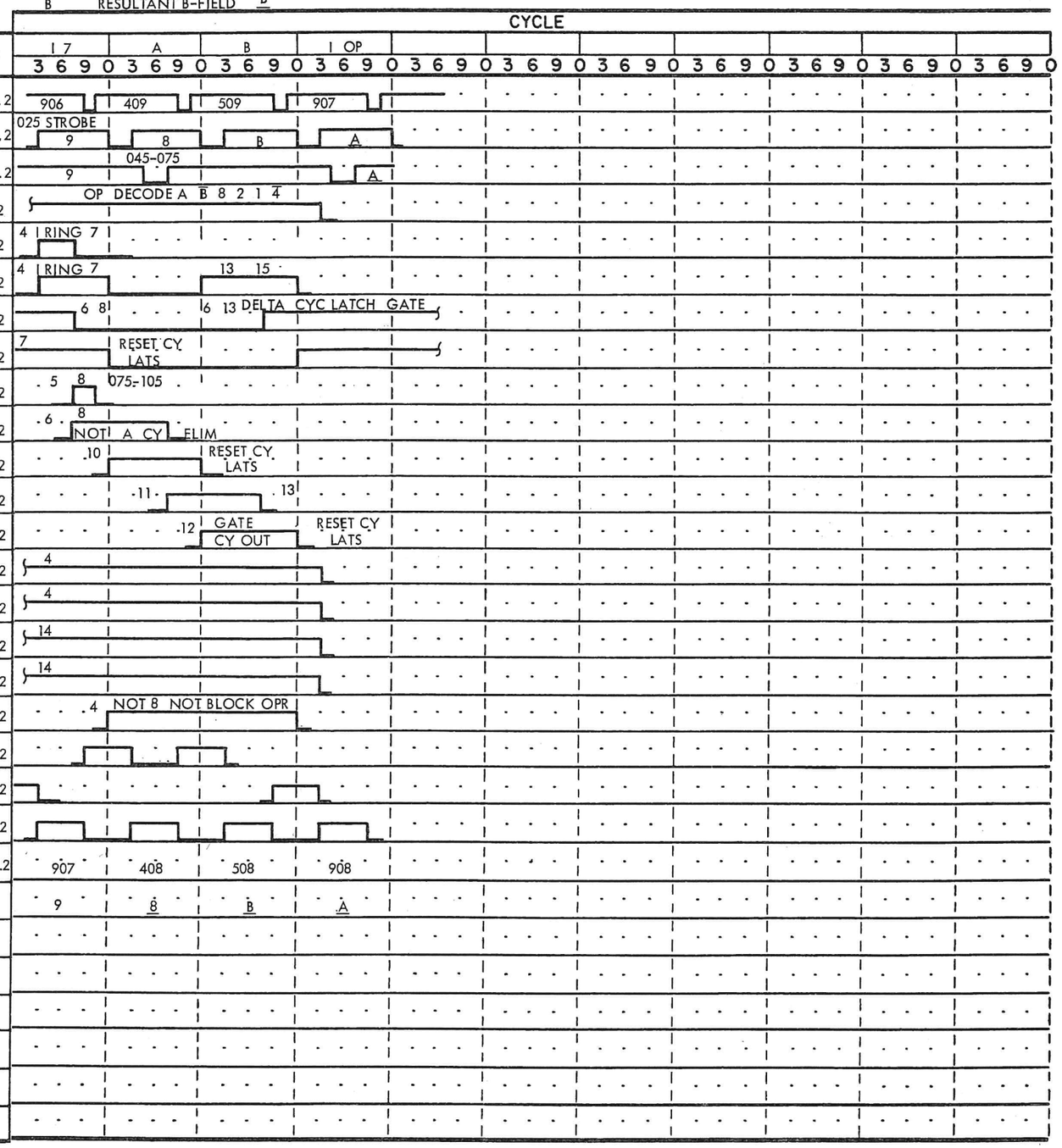


FIGURE 13. WORD MARK SET (AAA) (BBB)

899 A
900 C (458) (378)
907 S

ORIG A-FIELD AB2
ORIG B-FIELD B9 7

C6 3
CAB3 3

RESULTANT B-FIELD (SAME AS ORIG)

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1		STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2
2		B-REGISTER LATCHES	—	—	35.XX.XX.2
3		A-REGISTER LATCHES	—	—	35.XX.XX.2
4	+U	COMPARE OPERATION	01B1	A11F	35.24.11.2
5	-T	GATED WORD MARK	01B2	C20C	31.07.11.2
6	-T	I-E CHANGE	01B2	C22N	31.05.31.2
7	+U	DELTA I-CYCLE	01B2	E07N	31.21.11.2
8	-T	I-CYCLE	01B2	A23F	31.24.11.2
9	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2
10	+U	DELTA A-CYCLE	01B2	E07A	31.22.11.2
11	-T	A-CYCLE	01B2	E21P	31.25.11.2
12	-T	DELTA B-CYCLE	01B2	E15H	31.23.11.2
13	+U	B-CYCLE	01B2	D23N	31.26.11.2
14	-T	B-REG ZONE INHIBIT	01A3	D18P	35.18.21.2
15	-T	B-REG DIGIT INHIBIT	01A3	F17P	35.18.31.2
16	-T	B-REG C-BIT INHIBIT	01A3	C11H	35.18.21.2
17	-T	B-REG WM INHIBIT	01A3	C19C	35.18.21.2
18	+U	TRANSFER B-REG	01A3	E18H	35.18.11.2
19	+U	I-E CONTROL 1	01B2	C16A	31.05.21.2
20	+U	(COMPARE) EQUAL LATCH	01B6	A16P	34.21.21.2
21	-T	EQUAL CHAR	01B6	B05H	34.21.11.2
22	+U	UNEQUAL CHAR	01B6	B18H	34.21.21.2
23	-T	(COMPARE) UNEQUAL LATCH	01B6	B16P	34.21.21.2
24	+U	A-REG WM LATCH	01B2	D15H	31.06.11.2
25	U	MODIFIER CONTROL - 1	01A8	B04H	32.42.11.2
26	+U	MODIFIER CONTROL + 1	01A8	D06N	32.42.11.2
27	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2
28		MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX.2
29		DATA ON INHIBIT DRIVE LINES	—	—	—

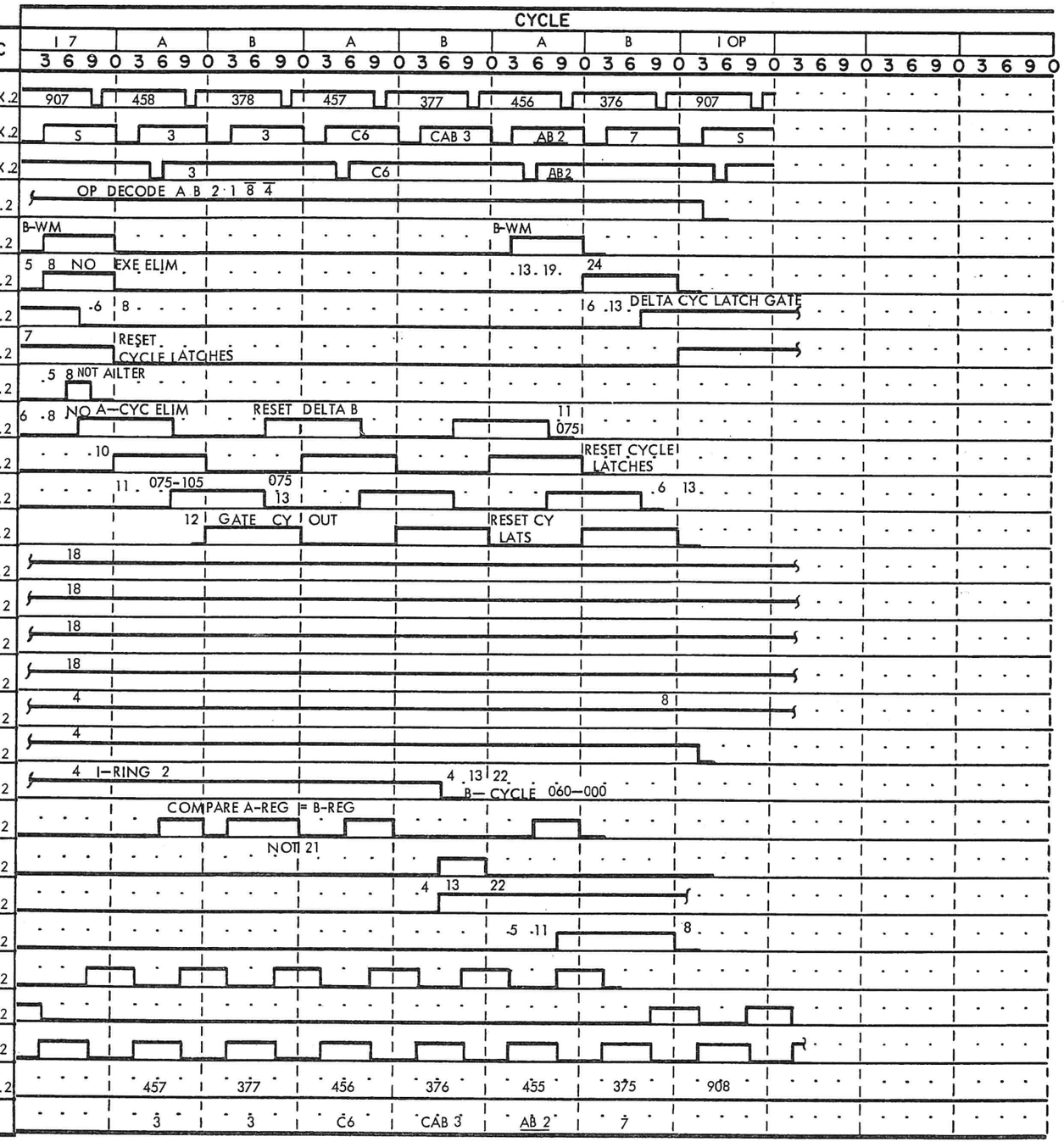


FIGURE 14. COMPARE C (AAA) (BBB)

ORIGINAL A FIELD "B63" OR WM/AB2 C42 21

ORIGINAL B FIELD "7C3" WM/42T CAB21 21

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1		STORAGE ADDRESS REGISTER	—	—	32.35.XX 32.36.XX
2		B-REGISTER	—	—	35.11.XX
3		A-REGISTER	—	—	35.16.XX
4	+U	COMPARE OPERATION	01B1	A11F	35.24.11
5	-T	GATED WORD MARK	01B2	C20C	31.07.11
6	-T	I/E CHANGE	01B2	C22N	31.05.31
7	+U	DELTA I CYCLE	01B2	E07N	31.21.11
8	-T	I CYCLE	01B2	A23F	31.24.11
9	+U	I STAR RESTORE	01A8	B17H	32.39.11
10	-T	DELTA A CYCLE	01B2	E07A	31.22.11
11	-T	A CYCLE	01B2	E21P	31.25.11
12	-T	DELTA B CYCLE	01B2	E15H	31.23.11
13	+U	B CYCLE	01B2	D23N	31.26.11
14	+U	TRANSFER B REGISTER	01A3	E18H	35.18.11
15	+U	I/E CONTROL 1	01B2	C16A	31.05.21
16	-T	B REG ZONE INHIBIT	01B4	D18P	36.13.21
17	-T	B REG DIGIT INHIBIT	01B4	F17P	36.13.21
18	-T	B REG C BIT INHIBIT	01A3	C11H	35.18.21
19	-T	B REG WM INHIBIT	01A3	C19C	35.40.21
20	+U	COMPARE EQ LATCH OUTPUT	01B6	A16P	34.21.21
21	-T	EQUAL CHARACTER	01B6	B05H	34.21.11
22	-T	COMPARE UNEQUAL LAT OUTPUT	01B6	B16P	34.21.21
23	+U	HIGH LATCH	02A8	F04A	44.34.21
24	+U	A REG WM LATCH	01B2	D15H	31.06.11
25	-T	MODIFIER CONTROL -1	01A8	B04H	32.42.21
26	-T	MODIFIER CONTROL TRANSFER	01A8	C10A	32.42.41

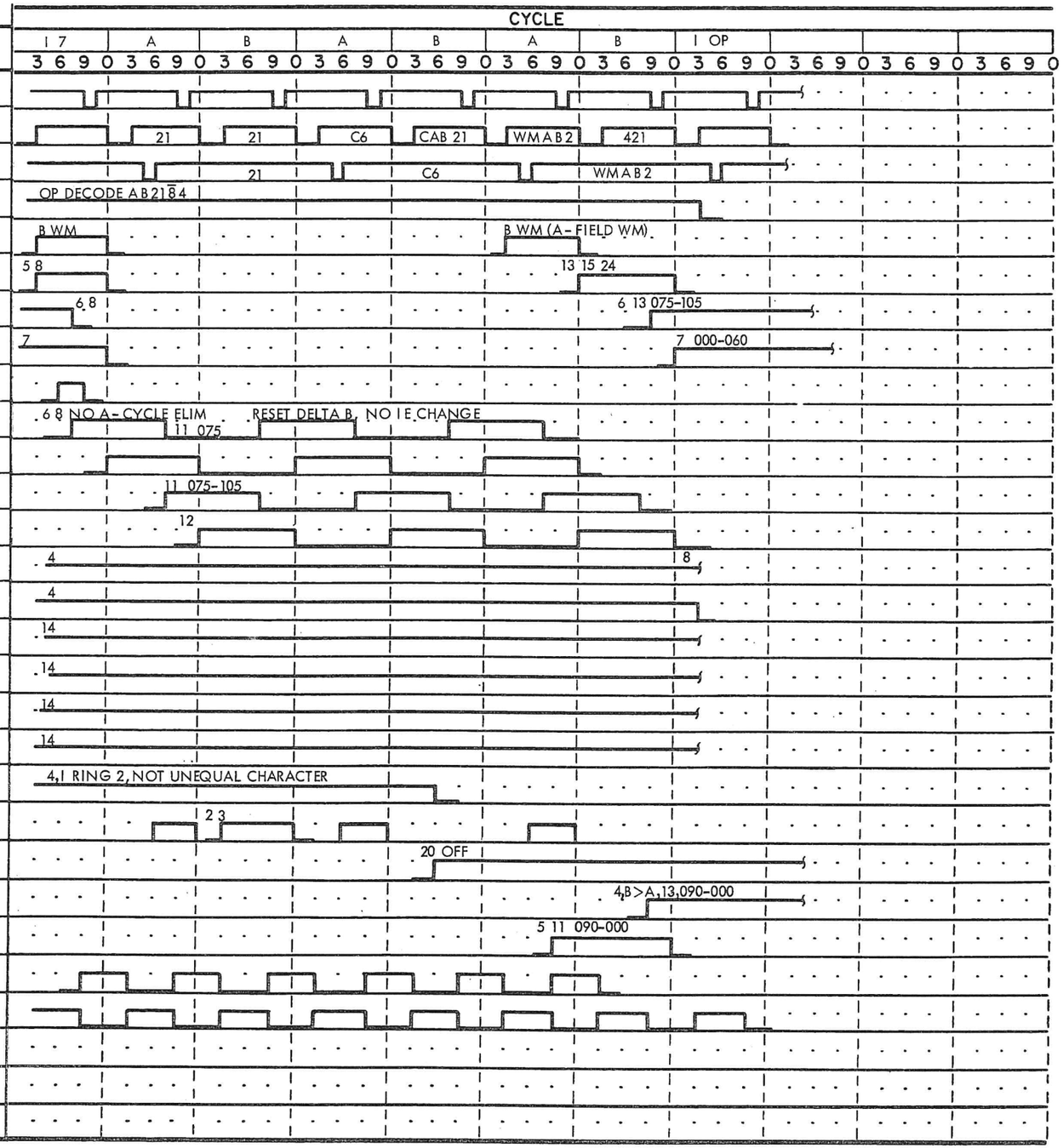


FIGURE 15. HIGH-LOW-EQUAL COMPARE SEQUENCE C (AAA) (BBB)

653 A
654 B (701)
658 BLANK

701 A

		SIGNAL NAME	FRAME	TEST POINT	LOGIC	CYCLE (1 4 / 1 OP; 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0)
1		STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2	658 701
2		B-REGISTER LATCHES	—	—	35.XX.XX.2	C-BIT A
3		A-REGISTER LATCHES	—	—	35.XX.XX.2	
4	-T	BRANCH OPR	01B1	A09N	35.26.11.2	OP DEC A B 2 8 4 1
5	-T	GATED WORD MARK	01B2	C20C	31.07.11.2	B-WM OR 6
6	+U	UNCOND TRANSFER	01B2	D08N	31.08.11.2	B-REG BLANK 030-000 14 I-RING 14
7						
8	+U	DELTA I-CYCLE LATCH	01B2	E07N	31.21.11.2	B-CYC LAT CNTL / DELTA CYC LAT GT 7 19
9	-T	I-CYCLE LATCH	01B2	E23A	31.24.11.2	8 000-060
10	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2	5 8 NOT ALTER 060-090
11	+U	EXECUTE ELIMINATE	01B2	C15C	31.05.11.2	4 I-RING 4
12	+U	TRANSFER PROGRAM SKIP	01B6	A11N	34.21.41.2	I-RING 4 4 5
13	-T	PROGRAM SKIP LATCH	01B2	C23A	31.08.11.2	4 OR 12 17 045-060
14	+U	I-A STAR GATE	01B2	D05C	31.08.11.2	13
15	+U	SET TO I-RING OP	01B2	D21B	31.30.11.2	13 17
16	-T	A-STAR GATE OUT	01A7	A07N	32.32.21.2	8 14 NOT SET-UP 090-000 NOT I-B STAR 1
17	-T	I-RING OP TRG	01B2	E20N	31.31.31.2	015-030 8 15 DELTA PROC
18						
19	+U	MODIFIER CONTROL +1	01A8	D06N	32.42.11.2	
20	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2	
21		MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX.2	702
22		DATA ON INHIBIT DRIVE LINES	—	—	—	C A

FIGURE 16. BRANCH B (III), UNCONDITIONAL BRANCH

653 A
654 $\overline{B}$ (701) d
659 $\overline{S}$

701 M

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC	CYCLE (1 5 … 1 OP; 3 6 9 0 3 6 9 0 …)
1		STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2	659 701
2		B-REGISTER LATCHES	—	—	35.XX.XX.2	S M
3		A-REGISTER LATCHES	—	—	35.XX.XX.2	d CHAR
4	-T	BRANCH OPR	01B1	A09N	35.26.11.2	OP DEC A B 2 8 4 1
5	-T	GATED WORD MARK	01B2	C20C	31.07.11.2	B - WM
6	-T	I-E CHANGE	01B2	C22N	31.05.31.2	5,10
7	+U	DELTA I-CYCLE	01B2	E07N	31.21.11.2	B-CYC LAT CNTL 6 8 / DELTA CYC LAT GT
8	-T	I-CYCLE	01B2	A23F	31.24.11.2	7 000-060
9	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2	5 8
10	+U	EXECUTE ELIMINATE	01B2	C15C	31.05.11.2	4 I-RING 4
11	+U	TEST BRANCH GATE	01B6	A08N	34.21.41.2	4 5 I-RING 5 (TESTS FOR CONDITION SPECIFIED BY ANY ONE OF 10 CHARACTERS)
12	+U	TRANSFER PROGRAM SKIP	01B6	A10H	34.21.41.2	TEST POS 11 (TURNED ON BY TEST BRANCH GATE IF TEST IS SUCCESSFUL)
13	-T	PROGRAM SKIP LATCH	01B2	C23A	31.08.11.2	12 17 045-060
14	+U	I-A STAR GATE	01B2	D05C	31.08.11.2	13
15	+U	SET TO I-RING OP	01B2	D21B	31.30.11.2	5 10 17
16	-T	A-STAR GATE OUT	01A7	A07N	32.32.21.2	7 14
17	-T	I-RING OP TGR	01B2	E20N	31.31.31.2	7 15 015-030 DELTA PROC AND 000-015
18	+U	MODIFIER CONTROL - 1	01A8	B04H	32.42.11.2	
19	+U	MODIFIER CONTROL +1	01A8	D06N	32.42.11.2	
20	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2	
21		MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX.2	702
22		DATA ON INHIBIT DRIVE LINES	—	—	——	S M

FIGURE 17. TEST AND BRANCH B (III) d (TEST ANY ONE OF TEN CHARACTERS)

699 A
700 B (308) (905) d ORIG A-FIELD DATA M
708 S

ORIG B-FIELD DATA Z = 1 BRANCH ON OVERFLOW

		SIGNAL NAME	FRAME	TEST POINT	LOGIC	CYCLE (1 8 / B / 1 OP; 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0)
1		STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2	708 905 308
2		B-REGISTER LATCHES	—	—	35.XX.XX.2	S Z M
3		A-REGISTER LATCHES	—	—	35.XX.XX.2	d CHAR
4	-T	BRANCH OPR	01B1	A09N	35.26.11.2	OP DECODE A B 2 8 4 1
5	-T	GATED WORD MARK	01B2	C20C	31.07.11.2	B-WM
6	-T	I-E CHANGE	01B2	C22N	31.05.31.2	5 8 NO EXE 11 13 ELIM
7	+U	DELTA I-CYCLE	01B2	E07N	31.21.11.2	6 8 6 DELTA CYCLE LATCH GATE B-CYCLE LATCH CNTL
8	-T	I-CYCLE	01B2	A23F	31.24.11.2	7 RESET CY LATS 7 RESET CY LATS
9	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2	5 8
10	-T	DELTA B-CYCLE	01B2	A21P	31.23.11.2	6 8 12 6 11
11	+U	B-CYCLE	01B2	D23N	31.26.11.2	10 RESET CY LATS
12	+U	A-CYCLE ELIM	01B2	D16D	31.06.11.2	4
13	+U	1 CHAR I-E CHANGE	01B2	C08N	31.05.11.2	4
14	-T	EQUAL CHARACTER	01B6	B05H	34.21.11.2	COMPARE A-REG = B-REG
15	+U	TRANSFER PROG SKIP	01B6	A08H	34.21.41.2	14 11 14 060-000
16	-T	PROGRAM SKIP LATCH	01B2	C23A	31.08.11.2	15 20 045-060
17	+U	I-A STAR GATE	01B2	D05C	31.08.11.2	16
18	+U	SET TO I-RING OP	01B2	E14A	31.30.11.2	16 20
19	-T	A-STAR GATE OUT	01A7	A07N	32.32.21.2	7 17
20	-T	I-RING OP TRG	01B2	E20N	31.31.31.2	7 18 015-030 DELTA IPROC
21	+U	MODIFIER CONTROL - 1	01A8	B04H	32.42.11.2	
22	+U	MODIFIER CONTROL + 1	01A8	D06N	32.42.11.2	
23	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2	
24		MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX.2	904 309
25		DATA ON INHIBIT DRIVE LINES	—	—	—	S Z M

FIGURE 18. TEST CHARACTER AND BRANCH B (III) (BBB) d (ANY ONE OF NINE CHARACTERS)

902 S
903 V (303) (402) C
911 M (409) (307)

402 T (WM - C-A-2 -1)
303 S

TEST BOTH ZONE AND WM AND BRANCH

CYCLE

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1		STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2
2		B-REGISTER LATCHES	—	—	35.XX.XX.2
3		A-REGISTER LATCHES	—	—	35.XX.XX.2
4	+U	ZONE TEST OPR	01B1	C11N	35.26.11.2
5	-T	GATED WORD MARK	01B2	C20C	31.07.11.2
6	-T	I-E CHANGE	01B2	C22N	31.05.31.2
7	+U	DELTA I-CYCLE	01B2	E07N	31.21.11.2
8	-T	I-CYCLE	01B2	A23F	31.24.11.2
9	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2
10	-T	DELTA B-CYCLE	01B2	E15H	31.23.11.2
11	+U	B-CYCLE	01B2	D23N	31.26.11.2
12	+U	1 CHAR I-E CHANGE	01B2	C08G	31.05.11.2
13	+U	TRANSFER B-REGISTER	01A3	E18H	35.18.11.2
14	+U	A-CYCLE ELIM	01B2	C16G	31.06.11.2
15	-T	A ZONE BIT EQUAL	01B6	A09P	34.21.11.2
16	-T	B ZONE BIT EQUAL	01B6	A09A	34.21.11.2
17	+U	ZONE TRANSFER GATE	01B6	A07N	34.21.41.2
18	+U	TRANSFER PROGRAM SKIP	01B6	A07H	34.21.41.2
19	-T	PROGRAM SKIP LATCH	01B2	C23A	31.08.11.2
20	+U	I-A STAR GATE	01B2	D05C	31.08.11.2
21	+U	SET TO I-RING OP LATCH	01B2	D21B	31.30.11.2
22	-T	A-STAR GATE OUT	01A7	A07N	32.32.21.2
23	-T	I-RING OP TRG	01B2	E20N	31.31.31.2
24	+U	MODIFIER CONTROL - 1	01A8	B04H	32.42.11.2
25	+U	MODIFIER CONTROL +1	01A8	D06N	32.42.11.2
26	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2
27		MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX.2
28		DATA ON INH DR LINES	—	—	

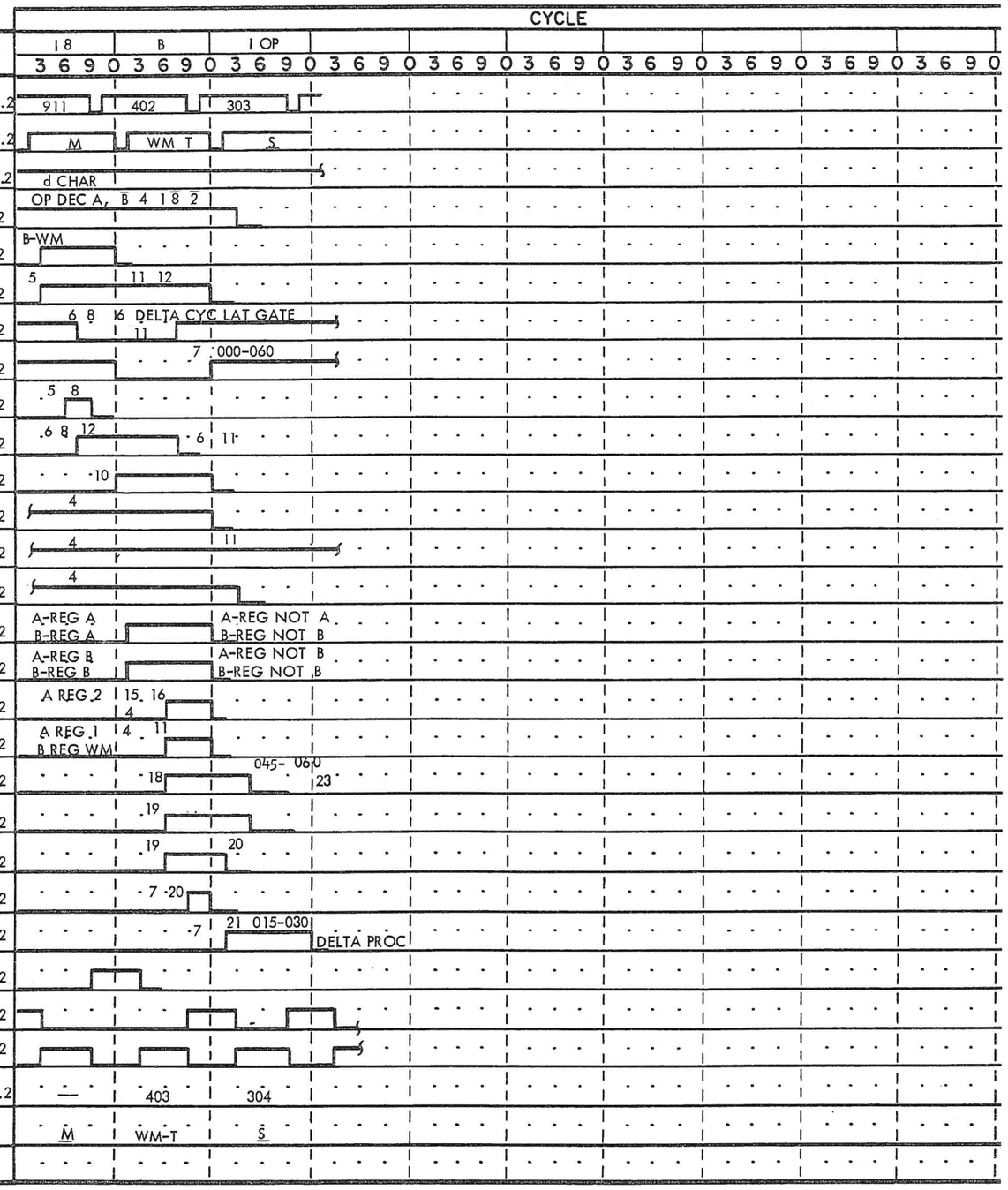


FIGURE 19. TEST ZONE OR WORD MARK OR BOTH AND BRANCH V (III) (BBB) d

899 2
900 7 (700) (404) ORIG B-FIELD 7 2 4 8 7
907 A RESULTANT B-FIELD b b b b b

CYCLE: I 7 | B | B | B | B | B | I OP

3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0 3 6 9 0

	SIGNAL NAME	FRAME	TEST POINT	LOGIC	CYCLE
1	STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2	907 404 403 402 401 400 700
2	B-REGISTER LATCHES	—	—	35.XX.XX.2	025-STROBE A 7 8 4 2 7
3	A-REGISTER LATCHES	—	—	35.XX.XX.2	
4	+U CLEAR OPERATION	01B1	C13N	35.26.11.2	OP DECODE A $\overline{B}$ 1 $\overline{8}$ $\overline{4}$ $\overline{2}$
5	-T GATED WORD MARK	01B2	C20C	31.07.11.2	B-WM
6	-T I-E CHANGE	01B2	C22N	31.05.31.2	5 NO EXE ELIM 8 4 22 NOT I CY
7	+U DELTA I-CYCLE	01B2	E07N	31.21.11.2	6 8 DELTA CYCLE LATCH GATE 6 B CYCLE LAT CNTL 1
8	-T I-CYCLE	01B2	E23A	31.24.11.2	7 RESET CY LATS 7 RESET CY LATS
9	+U I-STAR RESTORE GATE	01A7	A20N	32.39.11.2	5 8
10	-T DELTA B-CYCLE	01B2	E11H	31.23.11.2	6 8 16 NOT 16 11
11	+U B-CYCLE	01B2	D23N	31.26.11.2	10
12	-T B-REG ZONE INHIBIT	01A3	D18C	35.18.21.2	SUPPRESSED BY 4
13	-T B-REG DIGIT INHIBIT	01A3	D16A	35.18.31.2	SUPPRESSED BY 4
14	-T FIRST ROW	01A3	E16H	35.15.11.2	4 NOT BLOCK OP AND B-CYCLE (INSERT BLANKS)
15	-T B-REG WM INHIBIT	01A3	C19C	35.18.21.2	SUPPRESSED BY 4
16	+U A-CYCLE ELIM	01B2	D16D	31.06.11.2	4
17	+U I-A STAR GATE	01B2	D05C	31.08.11.2	4 I-RING 7 030 PRG SKIP LAT
18	+U UNCOND TRANSFER	01B2	D08H	31.08.11.2	4 I-RING 7
19	-T PROGRAM SKIP LATCH	01B2	C23A	31.08.11.2	4 I RING OP
20	+U SET TO I-RING OP	01B2	E14A	31.30.11.2	19
21	+U UNITS BORROW-CARRY	01A8	D03P	32.42.31.2	BORROW OR CARRY 000-030 060
22	+U TENS BORROW-CARRY	01A8	D03C	32.42.31.2	TENS POSITION 82 045-060
23	-T A-STAR GATE OUT	01A7	A07N	32.32.21.2	7 17
24	+U I-RING OP TRG	01B6	E20E	31.31.31.2	NOT I-B STAR 1 20 015-030 7 RESET I RING
25	+U MODIFIER CONTROL - 1	01A8	B04H	32.42.11.2	19 20
26	+U MODIFIER CONTROL + 1	01A8	D06N	32.42.11.2	
27	-T MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2	
28	MODIFIER OUTPUT ON BUS LINES	—	—	32.42.XX.2	403 402 401 400 399 701
29	DATA ON INHIBIT DRIVE LINES	—	—	—	b b b b b

FIGURE 20. CLEAR AND BRANCH / (III) (BBB)

691 S
692 . (305)
696 A

305 M

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1		STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2
2		B-REGISTER LATCHES	—	—	35.XX.XX.2
3		A-REGISTER LATCHES	—	—	35.XX.XX.2
4	+U	STOP OPR	01B1	A13F	35.24.11.2
5	-T	GATED WORD MARK	01B2	C20C	31.07.11.2
6	+U	DELTA I-CYCLE LATCH	01B2	E07N	31.21.11.2
7	-T	I-CYCLE LATCH	01B2	E23A	31.24.11.2
8	+U	DELTA PROCESS LATCH	01B2	B11N	31.02.11.2
9	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2
10	+U	EXECUTE ELIM	01B2	C12N	31.05.11.2
11	-T	PROGRAM SKIP LATCH	01B2	D12H	31.08.11.2
12	+U	I-A STAR GATE	01B2	D05C	31.08.11.2
13	+U	SET TO I-RING OP LATCH	01B2	D21B	31.30.11.2
14	+U	DELTA PROCESS RESET	01B2	B19A	31.02.31.2
15	-T	A-STAR GATE OUT	01A7	A07N	32.32.21.2
16	-T	I-RING OP TRG	01B6	E20N	31.31.31.2
17	+U	MODIFIER CONTROL - 1	01A8	B04H	32.42.11.2
18	+U	MODIFIER CONTROL + 1	01A8	D06N	32.42.11.2
19	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2
20		MODIFIER OUTPUT ON BUS LINES	—	—	—
21		DATA ON INH DRIVE LINES	—	—	—

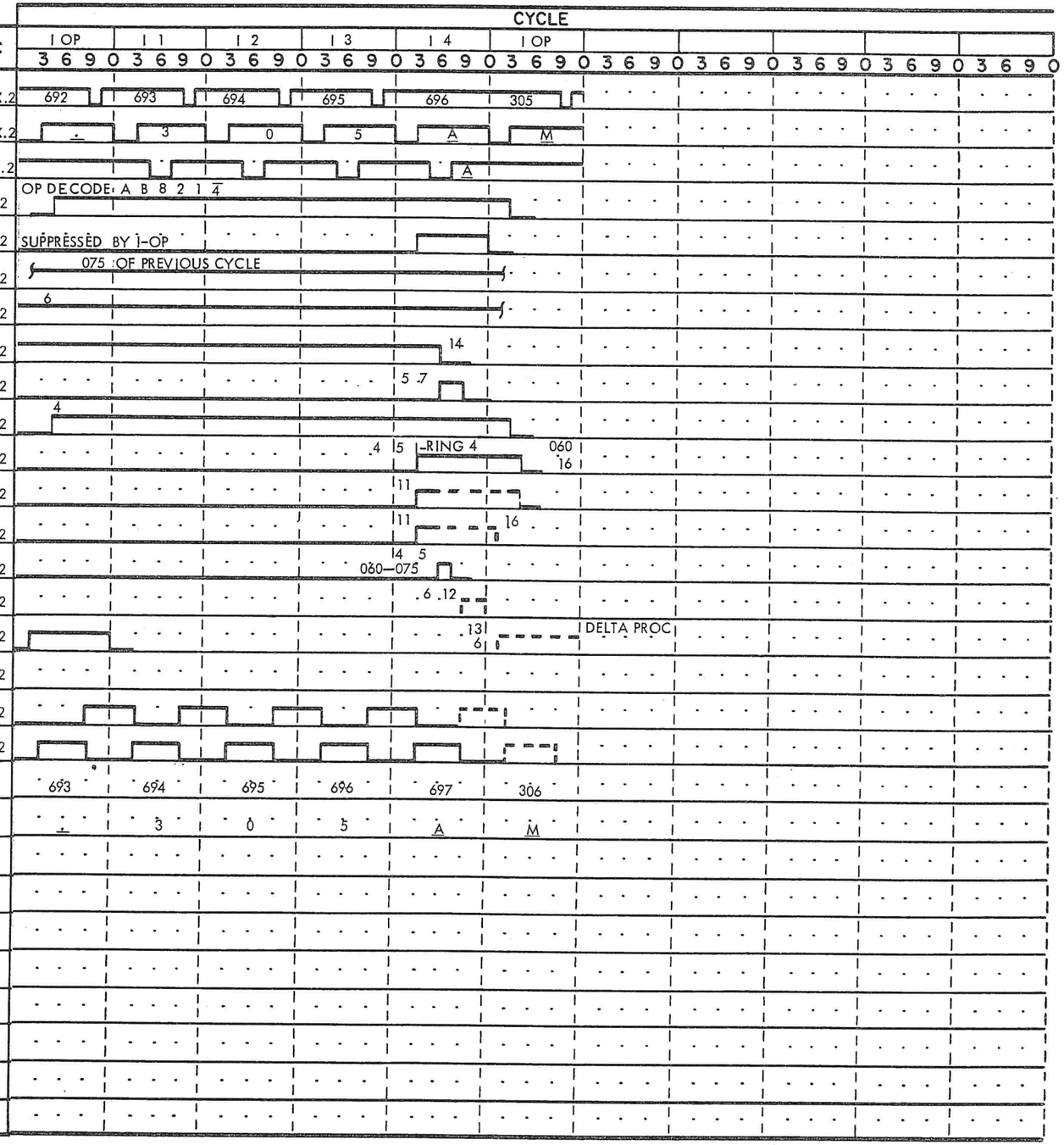


FIGURE 21. STOP AND BRANCH. (III)

673 9
674 ÷
675 A

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1		STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2
2		B-REGISTER LATCHES	—	—	35.XX.XX.2
3		A-REGISTER LATCHES	—	—	35.XX.XX.2
4	+U	STOP OPR	01B1	A13F	35.24.11.2
5	-T	GATED WORD MARK	01B2	C20C	31.07.11.2
6	+U	UNCOND TRANSFER	01B2	D08H	31.08.11.2
7	+U	DELTA I-CYCLE	01B2	E07N	31.23.11.2
8	-T	I-CYCLE LATCH	01B2	E23A	31.24.11.2
9	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2
10	+U	EXECUTE ELIM	01B2	C12N	31.05.11.2
11	+U	DELTA PROCESS LATCH	01B2	B11N	31.02.11.2
12	+U	DELTA PROCESS RESET	01B2	B19A	31.02.31.2
13	+U	MODIFIER CONTROL - 1	01A8	B04H	32.42.11.2
14	+U	MODIFIER CONTROL + 1	01A8	D06N	32.42.11.2
15	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2
16		MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX.2
17		DATA ON INHIBIT DRIVE LINES	—	—	—

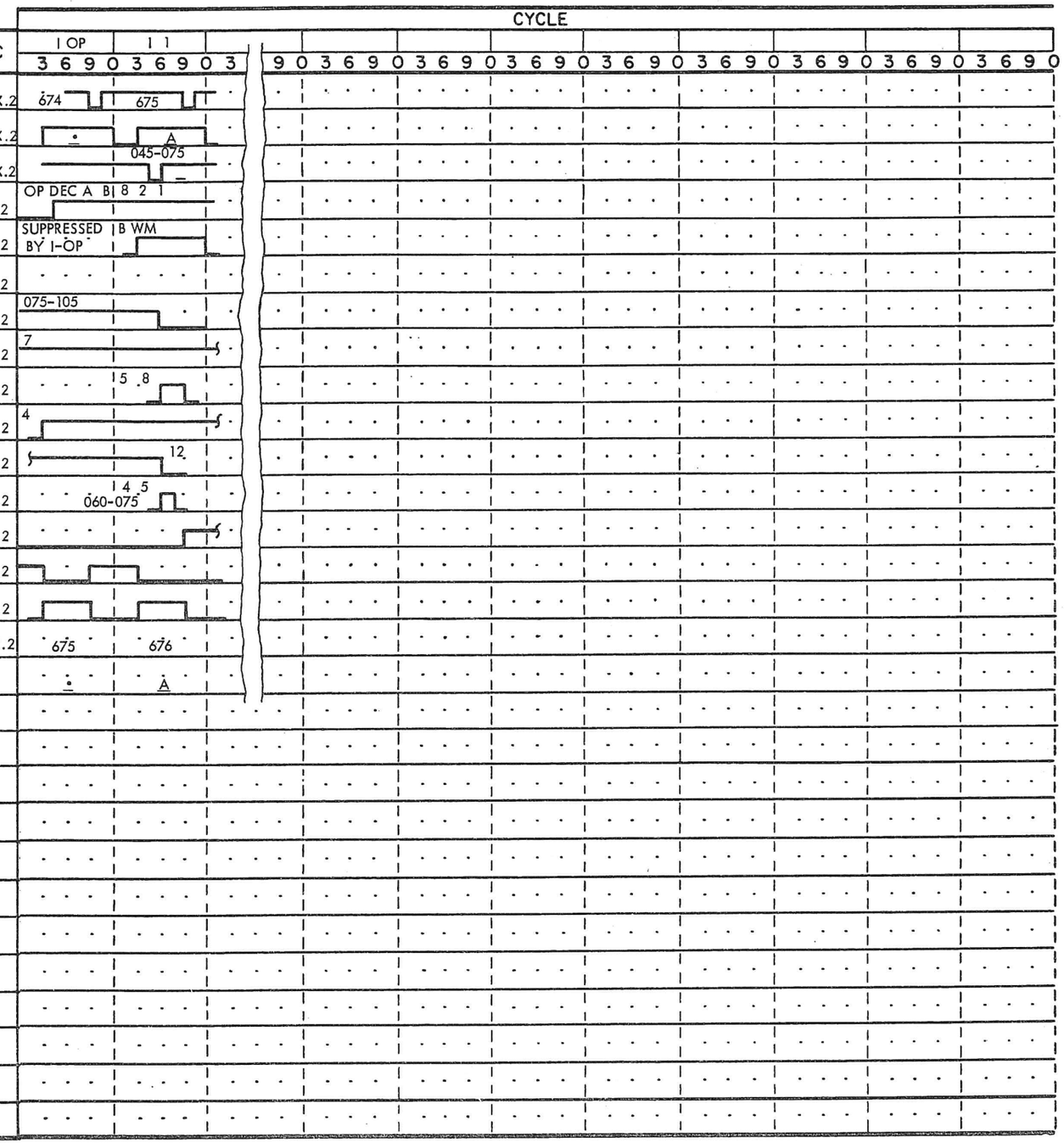


FIGURE 22. STOP (.)

651 S
652 N (496)
656 A

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC	CYCLE
1		STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2	652 653 654 655 656 656
2		B-REGISTER LATCHES	—	—	35.XX.XX.2	N 4 9 6 A A
3		A-REGISTER LATCHES	—	—	35.XX.XX.2	4 9 6
4	+U	NO-OP OPR	01B1	B12F	35.25.11.2	OP DEC B $\overline{A}$ 4 1 8 $\overline{2}$
5	-T	GATED WORD MARK	01B2	C20C	31.07.11.2	SUPPRESSED BY I OP; B WM
6	-T	I-E CHANGE	01B2	C22N	31.05.31.2	SUPPRESSED BY 11
7	+U	DELTA I-CYCLE	01B2	E07N	31.21.11.2	075 OF PREVIOUS CYCLE
8	-T	I-CYCLE LATCH	01B2	E23A	31.24.11.2	7 000-060
9	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2	5 8
10	+U	UNCOND TRANSFER	01B2	D08H	31.08.11.2	
11	+U	EXECUTE ELIMINATE	01B2	C12G	31.05.11.2	4
12	+U	SET TO I-RING OP LATCH	01B2	D21B	31.30.11.2	5 11 075-105 13
13	-T	I-RING OP TRG	01B2	E20N	31.31.31.2	7 12 015-030; DELTA PROC 000-015
14	+U	MODIFIER CONTROL - 1	01A8	B04H	32.42.11.2	
15	+U	MODIFIER CONTROL + 1	01A8	D06N	32.42.11.2	
16	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2	
17		MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX.2	653 654 655 656 657 657
18		DATA ON INHIBIT DRIVE LINES	—	—	—	N 4 9 6 A A

FIGURE 23. NO-OP (N)

651 S
652 N (496)
656 A

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC	CYCLE: I OP (3 6 9 0)	I 1 (3 6 9 0)	I 2 (3 6 9 0)	I 3 (3 6 9 0)	I 4 (3 6 9 0)	I OP (3 6 9 0)	(3 6 9 0)	(3 6 9 0)	(3 6 9 0)	(3 6 9 0)	(3 6 9 0)
1		STORAGE ADDRESS REGISTER	—	—	32.XX.XX.2	652	653	654	655	656	656					
2		B-REGISTER LATCHES	—	—	35.XX.XX.2	N	4	9	6	A	A					
3		A-REGISTER LATCHES	—	—	35.XX.XX.2		4	9	6							
4	+U	NO-OP OPR	01B1	B12F	35.25.11.2	OP DEC B $\overline{A}$ 4 1 8 $\overline{2}$										
5	-T	GATED WORD MARK	01B2	C20C	31.07.11.2	SUPPRESSED BY I OP				B WM						
6	-T	I-E CHANGE	01B2	C22N	31.05.31.2	SUPPRESSED BY 11										
7	+U	DELTA I-CYCLE	01B2	E07N	31.21.11.2	075 OF PREVIOUS CYCLE										
8	-T	I-CYCLE LATCH	01B2	E23A	31.24.11.2	7 000-060										
9	+U	I-STAR RESTORE GATE	01A7	A20N	32.39.11.2				5	8						
10	+U	UNCOND TRANSFER	01B2	D08H	31.08.11.2											
11	+U	EXECUTE ELIMINATE	01B2	C12G	31.05.11.2	4										
12	+U	SET TO I-RING OP LATCH	01B2	D21B	31.30.11.2				075–105	5 11	13					
13	-T	I-RING OP TRG	01B2	E20N	31.31.31.2					7 12 015-030		DELTA PROC 000-015				
14	+U	MODIFIER CONTROL - 1	01A8	B04H	32.42.11.2											
15	+U	MODIFIER CONTROL + 1	01A8	D06N	32.42.11.2											
16	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2											
17		MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX.2	653	654	655	656	657	657					
18		DATA ON INHIBIT DRIVE LINES	—	—	—	N	4	9	6	A	A					

FIGURE 23. NO-OP (N)

A-FIELD 000504 601 E 410 510 RESULTANT A-FIELD (AFTER EDIT) $0,005.04* RESULTANT B-FIELD (AFTER ZERO SUPP) $bbbb.5 0 4 *
B-FIELD $b,bb0.bb* 608 L 710 510 RESULTANT B-FIELD
615 B 601

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1		STORAGE ADDRESS REGISTER	—	—	32.35.XX 32.36.XX
2		B-REGISTER	—	—	35.11.XX
3		A-REGISTER	—	—	35.16.XX
4	+U	EDIT	01B1	B21A	35.24.11
5	-T	GATED WM	01B2	C25B	31.07.11
6	-T	I-E CHANGE	01B2	B13H	31.05.31
7	+U	DELTA I-CYCLE	01B2	E07N	31.21.11
8	-T	I-CYCLE LATCH	01B2	E19N	31.24.11
9	+U	I-STAR RESTORE	01A8	B17H	32.39.11
10	+U	DELTA A-CYCLE LATCH	01B2	E09N	31.22.11
11	-T	A-CYCLE LATCH	01B2	B20N	31.25.11
12	-T	DELTA B-CYCLE LATCH	01B2	E09E	31.23.11
13	+U	B-CYCLE LATCH	01B2	E24H	31.26.11
14	-T	B-REG ZONE INHIBIT	01A3	D18C	35.18.21
15	-T	B-REG DIGIT INHIBIT	01A3	D16A	35.18.31
16	-T	B-REG C-BIT INHIBIT	01A3	C11H	35.18.21
17	-T	B REG WM INHIBIT	01A3	C19C	35.18.21
18	-T	A-REG DIGIT INHIBIT	01A3	B11G	35.18.41
19	-T	A-REG ZONE INHIBIT	01A3	F20N	35.18.41
20	+U	INHIBIT C-ZONE	01A3	E14A	35.15.11
21	+U	OTHER EDIT	01A3	C16N	35.10.31
22	+U	EDIT A-DIGIT	01B6	D25C	34.10.31
23	+U	EDIT A-ZONE	01B6	D25G	34.10.31
24	-T	NOT A-CYCLE ELIM	01B2	D18C	31.06.11
25	-T	EDIT 1ST A CYCLE	01B6	D15N	34.10.41
26	-T	BODY TRIGGER	01B6	D21N	34.10.41
27	+U	SET WM LATCH	01B6	D06A	34.10.51
28	-T	EDIT WM SET	01B6	D22P	34.10.51
29	-T	ZERO SUPPRESS LATCH	01B6	D22C	34.10.51
30	-T	A-FIELD WM LATCH	01A3	C10G	35.14.51
31	+U	1ST EDIT READDRESS	01B6	E14H	34.10.61
32	-T	NOT READDRESS	01B2	C09P	31.04.11
33	-T	REV SCAN TRIGGER	01B2	F07N	31.04.11
34	+U	CYCLE CONTROL REV SCAN	01B2	C08A	31.04.11
35	-T	REV SCAN DELAY	01B6	D22A	34.10.51
36	+U	EDIT REGEN C-BIT	01B6	E16N	34.10.61
37	+U	MZS OR E-IE CHANGE	01B6	E15H	34.10.61
38	+U	MODIFIER CONTROL -1	01A8	C04G	32.42.11
39	+U	MODIFIER CONTROL +1	01A8	C04H	32.42.11
40	-T	MODIFIER CONTROL XFER	01A8	C01E	32.42.41
41		MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX
42		DATA ON INHIBIT DRIVE LINES	—	—	—
43		(BEFORE ZERO B-FIELD AFTER EDIT SUPPRESSION)	—	—	—
44		B-FIELD AFTER ZERO SUPPRESSION	—	—	—

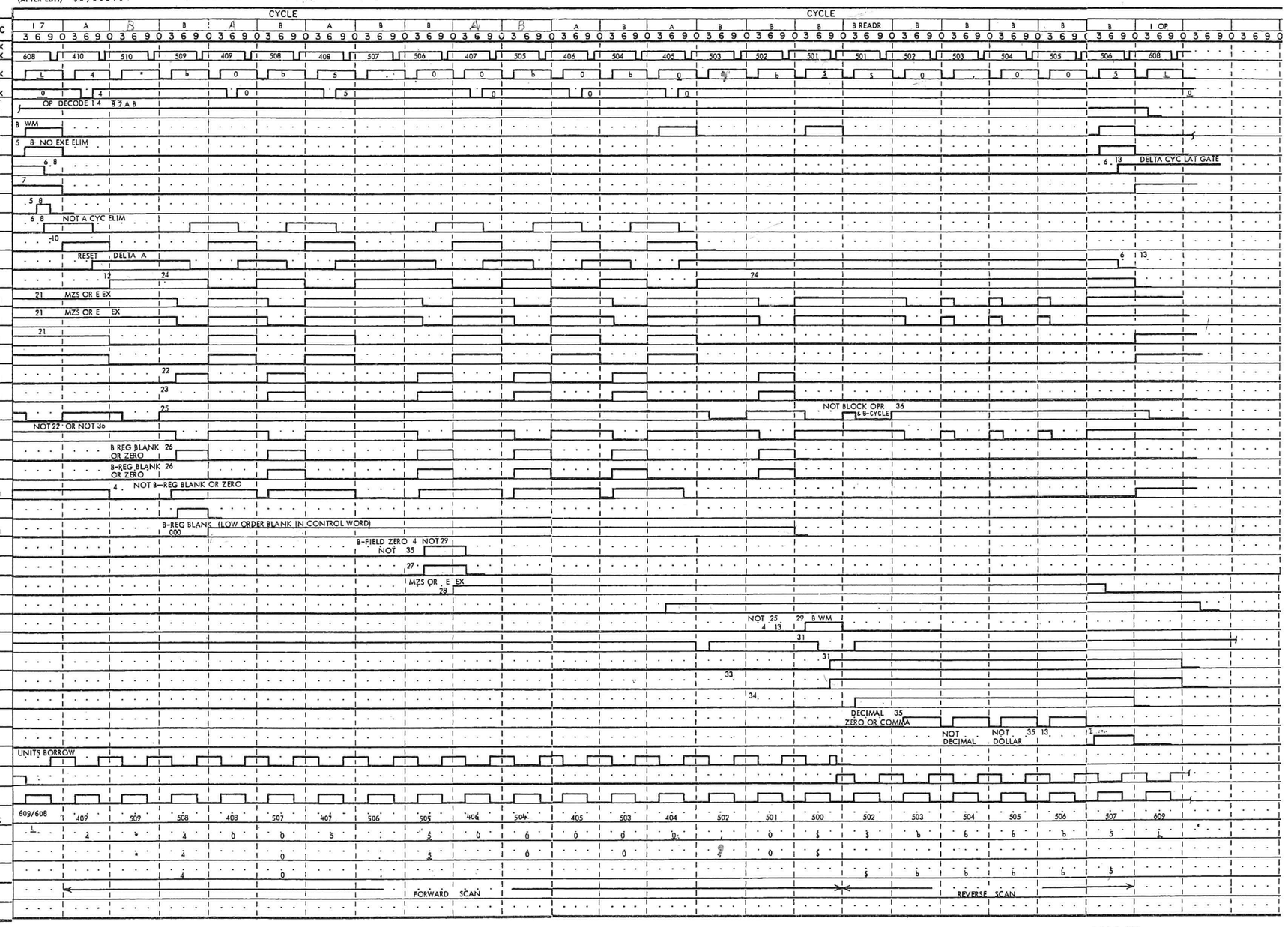


FIGURE 24. EDIT OPERATION - ZERO SUPPRESS

E (AAA) (BBB)

701 A (ATW) (4C2) A-TAG = V 0 ‡ RESULTANT A-STAR = 63F
708 S — — AB-TAG = 106 B-STAR = 53B

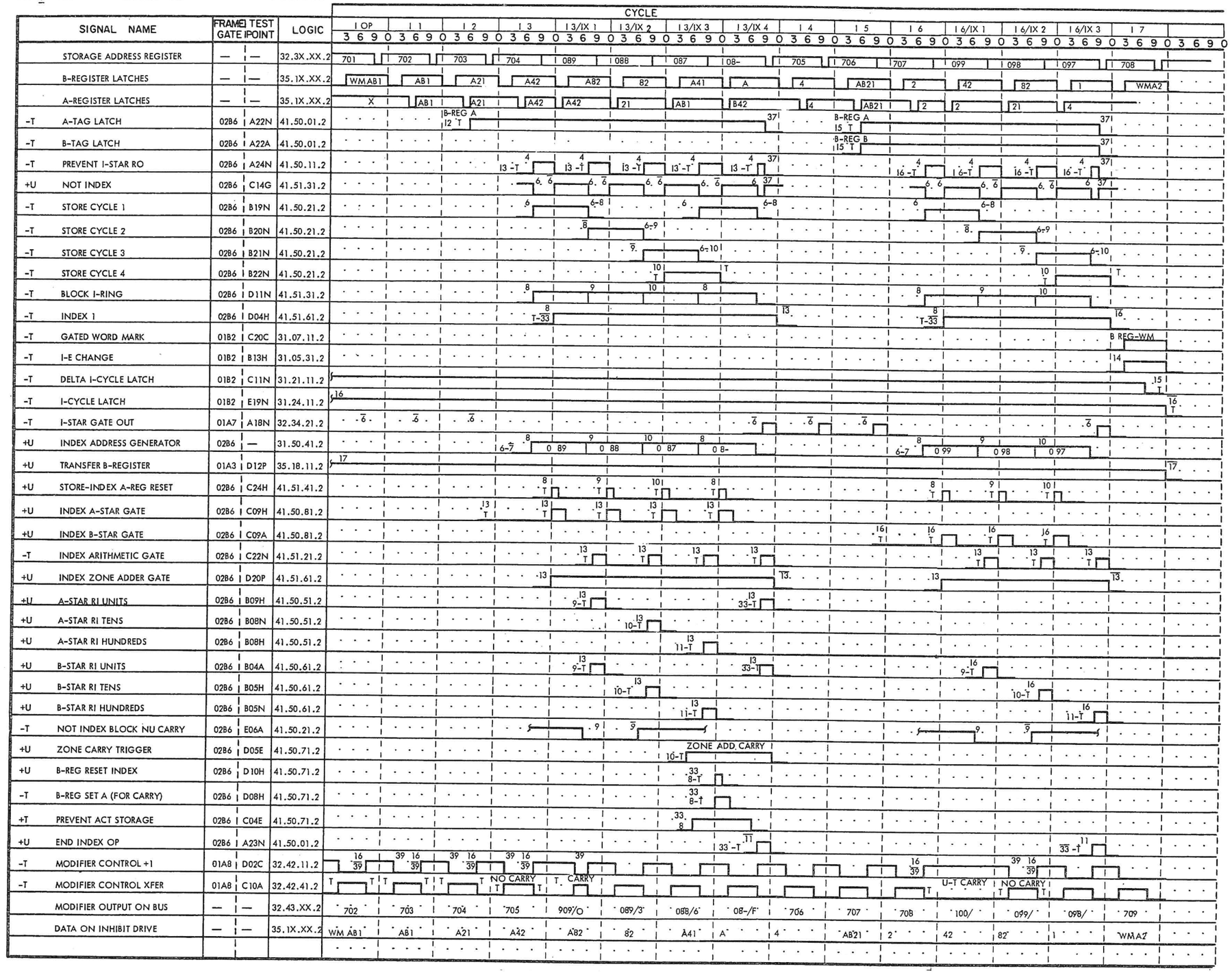


FIGURE 25. INSTRUCTION CYCLE WITH INDEXING

253 Q/H (336) PREVIOUS A-STAR 654 STORE Q OPR 654
257 A — — ADDRESSES B-STAR 824

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1		STORAGE ADDRESS REGISTER	—	—	32.35.XX
2		B-REGISTER LATCHES	—	—	35.11.XX
3		A-REGISTER LATCHES	—	—	36.16.XX
4	+U	H OPR (STORE B-STAR) Q OPR (STORE A-STAR)	01B1	A25A A25H	41.52.31
5	+U	Q TRIGGER ON	02B5	G17E	41.51.31
6	+U	Q MODIFY	02B6	D04E	41.51.31
7	-T	NOT INDEX	02B6	C13N	41.51.31
8	-T	GATED WORD MARK	01B2	C25B	31.07.11
9	-T	DELTA I-CYCLE LATCH	01B2	E07N	31.21.11
10	-T	I-CYCLE LATCH	01B2	E19N	31.24.11
11	-T	DELTA A-CYCLE LATCH	01B2	E09N	31.22.11
12	-T	A-CYCLE LATCH	01B2	B20N	31.25.11
13	+U	STORE CYCLE 1	02B6	B19N	41.50.11
14	+U	STORE CYCLE 2	02B6	B20N	41.50.11
15	+U	STORE CYCLE 3	02B6	B21N	41.50.11
16	-T	I-STAR GATE OUT	01A7	B16N	32.34.21
17	-T	A-STAR GATE OUT	01A7	B16B	32.32.21
18	-T	B-STAR RI GATE	02B6	C13G	41.50.31
19	+U	TRANSFER B-REGISTER	01A3	D12C	35.18.11
20	-T	A-REG STORE INHIBIT	02B6	D16H	41.51.71
21	-T	STORE OPR Q H AND A CYCLE	02B6	C23A	41.51.31
22	-T	A-REG ZONE INHIBIT	01B4	D09D	36.13.21
23	-T	A-REG DIGIT INHIBIT	01B4	D09A	36.13.21
24	+U	MODIFIER CONTROL -1	01A8	C04G	32.42.11
25	+U	MODIFIER CONTROL +1	01A8	C04H	32.42.11
26	-T	MODIFIER CONTROL XFER	01A8	C01E	32.42.41
27	-T	DELTA I SET Q-H	02B6	A21A	41.51.51
28	-T	I/E CHANGE	01B2	B13H	31.05.31
29		MODIFIER OUTPUT ON BUS	—	—	32.43.XX
30		DATA ON INHIBIT DRIVE	—	—	—

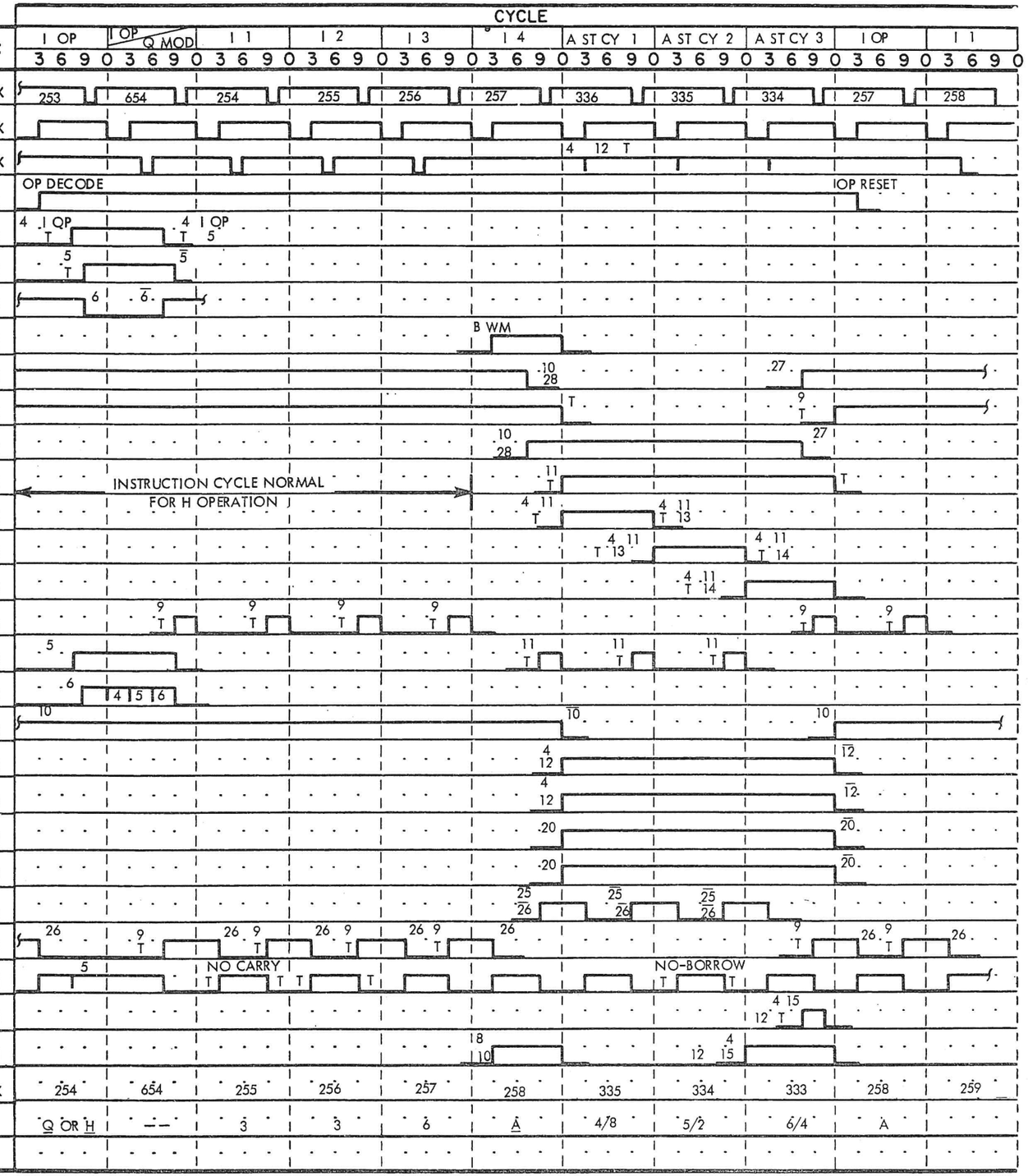


FIGURE 26. STORE A STAR Q (AAA) STORE B STAR H (AAA)

654 B (701)	BEFORE XFER	I-STAR A-STAR B-STAR
658 A — —	AFTER XFER	658 701 xxx
701 H (336)		658 701 658

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1		STORAGE ADDRESS REGISTER	—	—	32.35.XX 32.36.XX
2		B-REGISTER LATCHES	—	—	35.11.XX
3		A-REGISTER LATCHES	—	—	36.16.XX
4	-T	BRANCH OPERATION	01B1	A09N	35.26.11
5	-T	GATED WORD MARK	01B2	C25B	31.07.11
6	-T	I/E CHANGE	01B2	B13H	31.05.31
7	-T	DELTA I-CYCLE LATCH	01B2	E07N	31.21.11
8	-T	I-CYCLE LATCH	01B2	E19N	31.24.11
9	+U	I-STAR RESTORE	01A8	B17H	32.39.11
10	+U	EXECUTE ELIMINATION	01A2	C08H	31.05.11
11	+U	TRANSFER PROGRAM SKIP	01B6	A08H	34.21.41
12	-T	PROGRAM SKIP LATCH	01B2	D11N	31.08.11
13	+U	I-A STAR GATE	01B2	D05C	31.08.11
14	+U	SET TO I RING OP	01B2	E20H	31.30.11
15	-T	I-B STAR 1	02B6	C06N	41.51.51
16	+U	I-B STAR TRIGGER	02B6	C06N	41.51.51
17	+U	I STAR RO	02B6	C26A	41.51.51
18	-T	I-B STAR 2 (B-STAR RI)	02B6	D26C	41.51.51
19	+U	I RING OP	01B2	A16A	31.31.11
20	-T	A-STAR GATE OUT	01A7	B16B	32.32.21
21	-T	I-STAR GATE OUT	01A7	B16H	32.34.21
22	+U	MODIFIER CONTROL +1	01A8	C04H	32.42.41
23	-T	MODIFIER CONTROL XFER	01A8	C01E	32.42.41
24		MODIFIER OUTPUT ON BUS	—	—	32.43.XX
25		DATA ON INHIBIT DRIVE	—	—	—

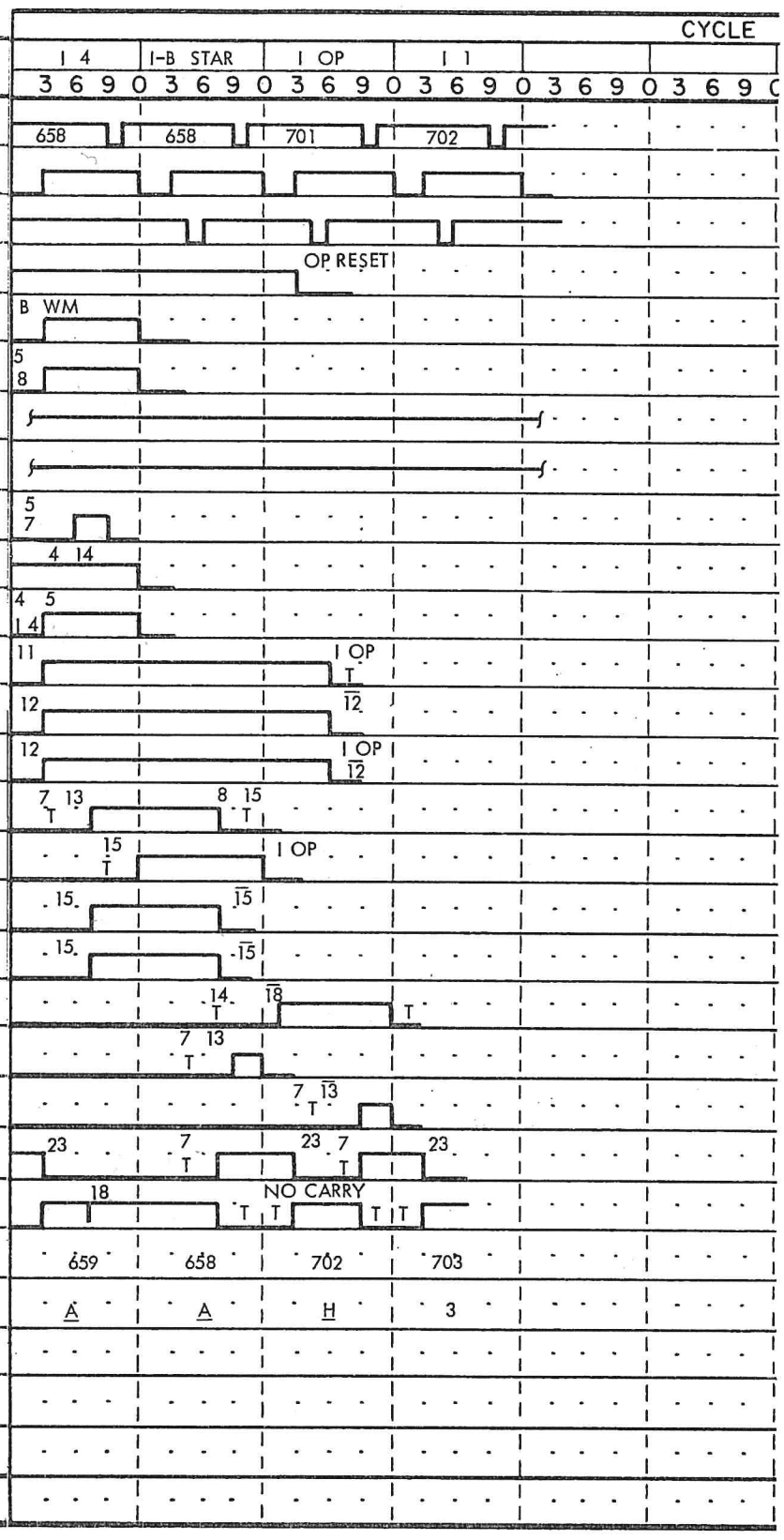


FIGURE 27. BRANCH B (III) ADVANCED PROGRAMMING (I-B STAR TRANSFER)

523 P (398) (437) A-FIELD ORIG 1 2 3 4 5 6 RM 7 RESULT 1 2 3 4 5 6 RM 7
529 S — — B-FIELD ORIG A B C D E F G H RESULT 1 2 3 4 5 6 RM H

	SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1	STORAGE ADDRESS REGISTER	—	—	32.36.XX 32.35.XX
2	B-REGISTER LATCHES	—	—	35.11.XX
3	A-REGISTER LATCHES	—	—	35.16.XX
4	+U P OPR (MOVE RECORD)	01B1	A25N	41.52.31
5	-T GATED WORD MARK	01B2	C25B	31.07.11
6	+U I/E CONTROL 2	01B2	C16B	31.05.21
7	-T DELTA I-CYCLE LATCH	01B2	E07H	31.21.11
8	-T I-CYCLE LATCH	01B2	E19N	31.24.11
9	-T DELTA A-CYCLE	01B2	E09N	31.22.11
10	-T A-CYCLE LATCH	01B2	B20N	31.25.11
11	-T DELTA B-CYCLE LATCH	01B2	E09E	31.23.11
12	-T B-CYCLE LATCH	01B2	E23H	31.26.11
13	-T I-STAR GATE OUT	01A7	B16H	32.32.81
14	-T A-STAR GATE OUT	01A7	B16B	32.32.81
15	-T B-STAR GATE OUT	01A7	B16A	32.32.81
16	+U TRANSFER B-REGISTER	01A3	D12C	35.18.11
17	-T B-REG ZONE INHIBIT	01A3	C21A	
18	-T B-REG DIGIT INHIBIT	01A3	D09C	
19	-T B-REG WM INHIBIT	01A3	C19C	35.18.21
20	+U A-REG ST INH	02B6	D16H	41.51.71
21	-T A-REG ZONE INHIBIT	01A3	D09P	36.13.21
22	-T A-REG DIGIT INHIBIT	01A3	D09A	36.13.21
23	+U MODIFIER CONTROL +1	01A8	C09H	32.42.21
24	-T MODIFIER CONTROL XFER	01A8	C01E	32.42.41
25	-T I/E CHANGE	01B2	B13H	31.05.31
26	MODIFIER OUTPUT ON BUS	—	—	32.43.XX
27	DATA ON INHIBIT DRIVE	—	—	—

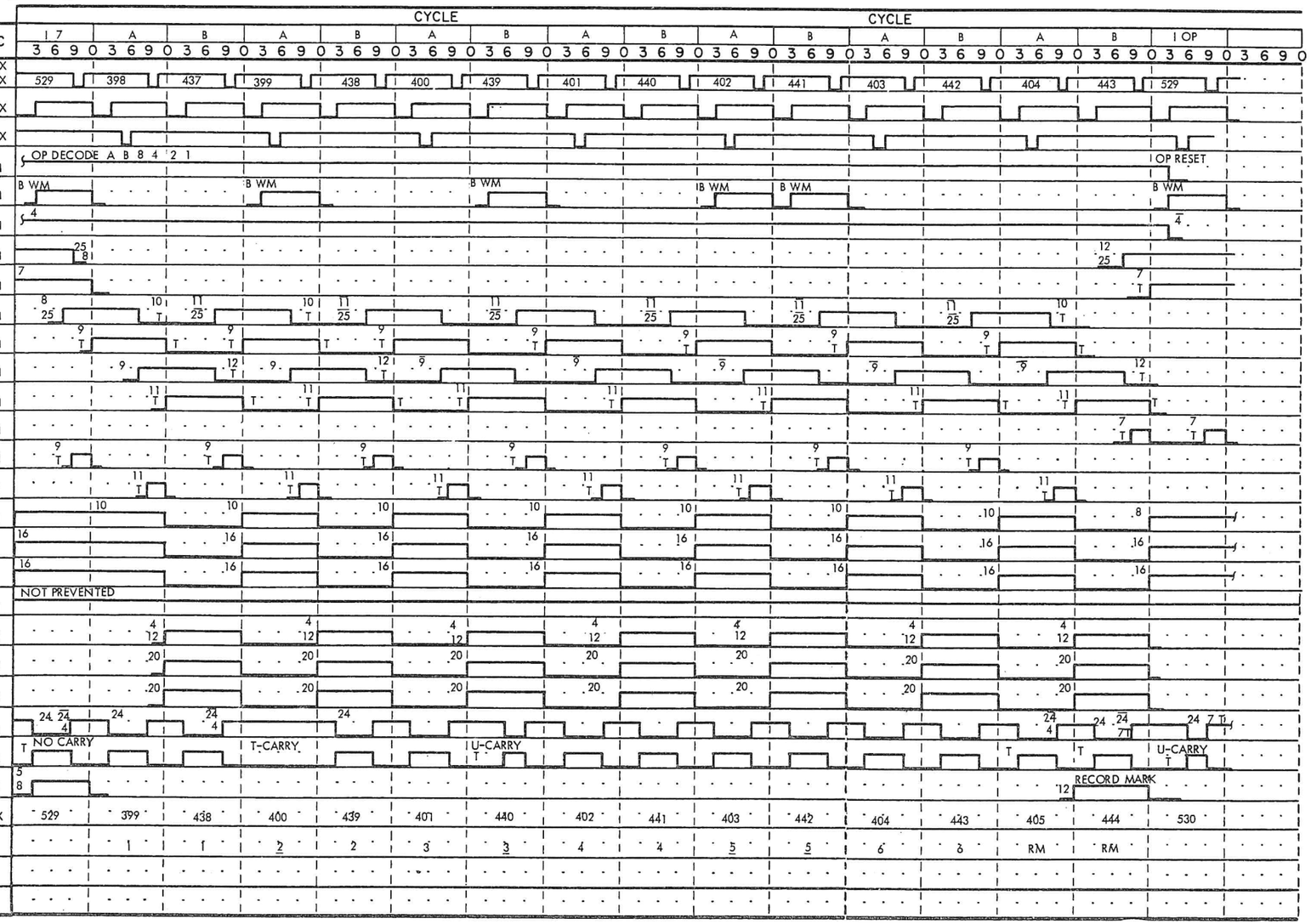


FIGURE 28. MOVE RECORD P (AAA) (BBB)

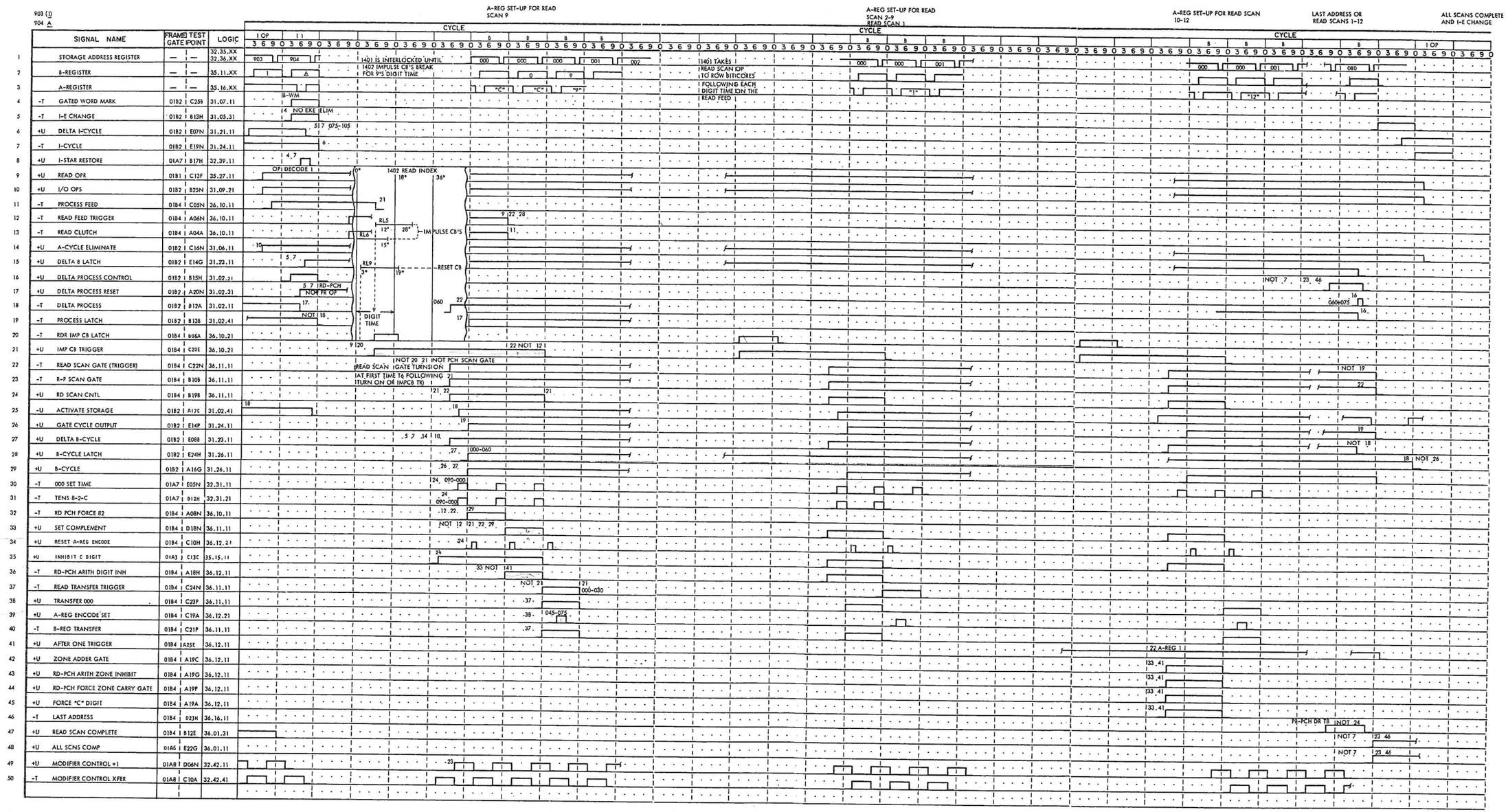


FIGURE 29. READ

903 4
904 A

	SIGNAL NAME	FRAME	TEST POINT	LOGIC
1	STORAGE ADDRESS REGISTER	—	—	32.35.XX 32.36.XX
2	B-REGISTER	—	—	35.11.XX
3	A-REGISTER	—	—	35.16.XX
4	-T GATED WM	01B2	C25B	31.07.11
5	-T I-E CHANGE	01B2	B13H	31.05.31
6	+U DELTA I-CYCLE	01B2	E07N	31.21.11
7	-T I-CYCLE	01B2	E19N	31.24.11
8	+U I-STAR RESTORE	01A7	B17H	32.39.11
9	+U PUNCH OPR	01B1	C14F	35.27.11
10	+U I/O OPS	01B2	B25N	31.09.21
11	-T PROC PUNCH	01B4	F07N	36.24.11
12	+U PUNCH FEED TRIGGER	01B4	E10E	36.24.11
13	-T PUNCH CLUTCH MAGNET	01B4	A04D	36.24.11
14	+U A-CYCLE ELIMINATE	01B2	C16N	31.06.11
15	+U DELTA B-LATCH	01B2	E14G	31.23.11
16	+U DELTA PROCESS RESET	01B2	A20N	31.02.31
17	-T DELTA PROCESS	01B2	B12A	31.02.11
18	-T PROCESS	01B2	B13B	31.02.41
19	-T PUNCH SCAN CB TRIGGER	01B4	A20N	36.21.11
20	+U PUNCH SCAN GATE	01B4	A22E	36.22.11
21	-T R-P SCAN GATE	01B4	B10B	36.11.11
22	+U PUNCH SCAN CTRL	01B4	B19N	36.22.11
23	+U GATE CYCLE OUTPUT	01B2	E14P	31.24.11
24	-U ACTIVATE STORAGE	01B2	A17C	31.02.41
25	+U DELTA B-CYCLE	01B2	E08B	31.23.11
26	+U B-CYCLE LATCH	01B2	E24H	31.26.11
27	+U B-CYCLE	01B2	A16G	31.26.11
28	-T 100 SET TIME	01A7	E01N	32.31.11
29	-T TENS 2-8-C	01A7	B12H	32.31.21
30	+U NOT SET-UP	01A7	B18C	32.31.21
31	+U PUNCH FEED RST GATE	01B4	A05N	36.10.11
32	-T RD PCH FORCE 82	01B4	A08N	36.10.11
33	+U ADD TO 100	01B4	A23H	36.22.11
34	-T A-REG SET B RD-PCH	01B4	B24N	36.12.21
35	+U ZONE ADDER GATE	01B4	A19C	36.12.11
36	+U RD-PCH FORCE ZONE CARRY	01B4	A19P	36.12.11
37	+U RD-PCH ARITH ZONE INH	01B4	A19G	36.12.11
38	+U FORCE C-DIGIT	01B4	A19A	36.12.11
39	+U PUNCH TRANSFER	01B4	A24E	36.22.11
40	+U RESET A REG ENCODE	01B4	C10H	36.12.21
41	+U A-REG ENCODE SET	01B4	C19A	36.12.21
42	-T B-REG TRANSFER	01B4	B18A	36.22.11
43	+U AFTER ZERO TRIGGER	01B4	C26A	36.12.11
44	+U FORCE DIGIT CARRY	01B4	C19N	36.12.11
45	-T FORCE C DIGIT	01B4	B20A	36.12.11
46	-T RD-PCH ARITH DIGIT INH	01B4	A18H	36.12.11
47	-T PCH DECODE SCAN	01B7	B06A	36.23.31
48	-T LAST ADDRESS	01B4	D23H	36.16.11
49	+U DELTA PROC CNTL	01B2	B15H	31.02.21
50	+U PUNCH SCAN COMPLETE	01B4	A12E	36.01.21
51	-T ALL SCANS COMPLETE	01A6	F21N	36.01.11
52	+U MODIFIER CONTROL +1	01A8	D06N	32.42.11
53	-T MODIFIER CONTROL XFER	01A8	C10A	32.42.41

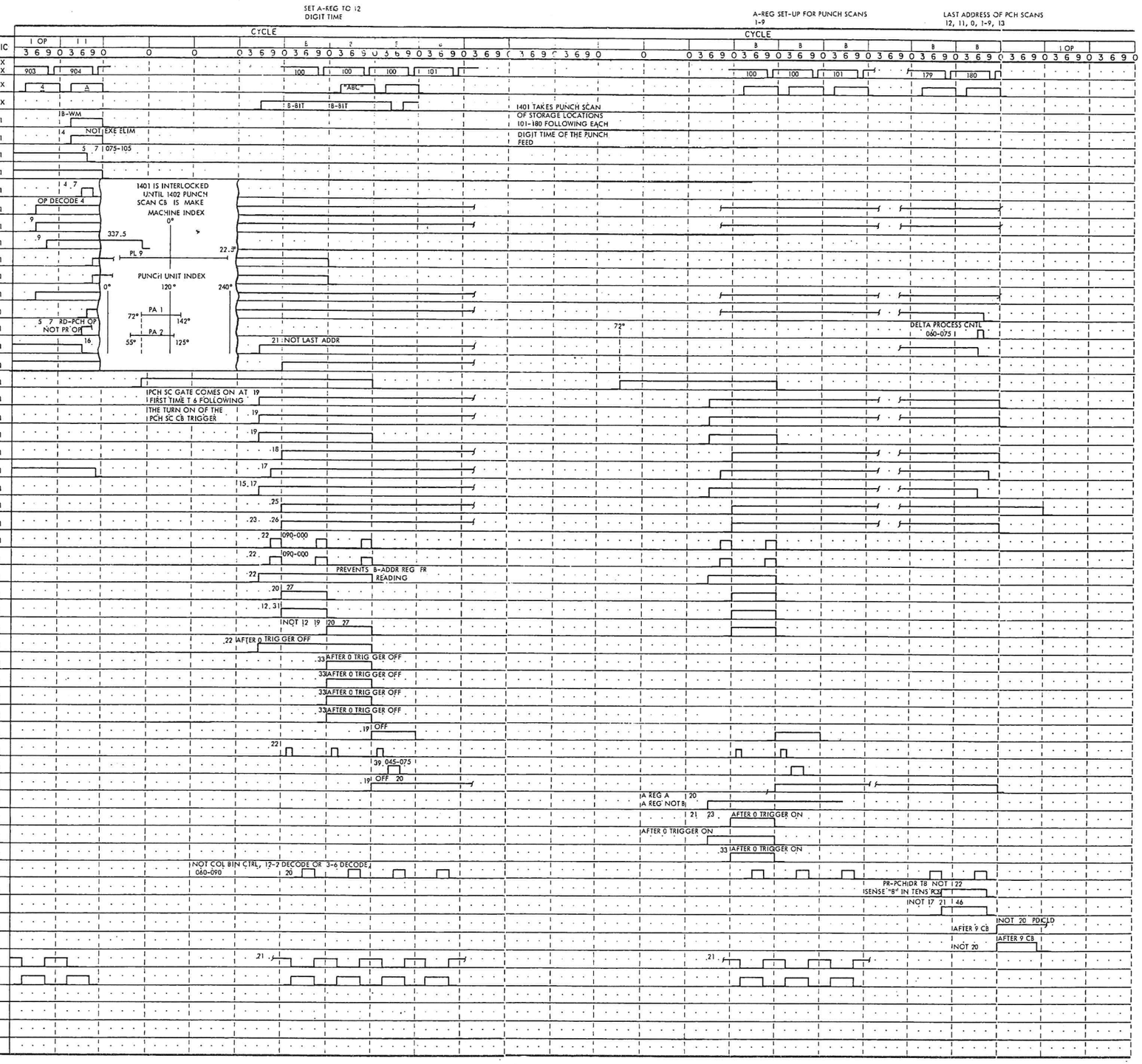


FIGURE 30. PUNCH

COLUMN BINARY - READ

	SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1	STORAGE ADDRESS REGISTER	—	—	32.35.XX
2	B-REGISTER	—	—	35.11.XX
3	A-REGISTER	—	—	35.16.XX
4	-T GATED WM	01B2	C25B	31.07.11
5	-T I/E CHANGE	01B2	B13H	31.05.31
6	+U DELTA I CYCLE	01B2	E07N	31.21.11
7	+U I-CYCLE	01B2	E17N	31.24.11
8	+U I STAR RESTORE	01A7	B17H	32.39.11
9	+U READ OPR	01B1	C13F	35.27.11
10	+U I/O OPS	01B2	B25N	31.09.21
11	-T READ FEED TRIGGER	01B4	A06N	36.10.11
12	-T READ CLUTCH	01B4	A04A	36.10.11
13	+U A CYCLE ELIMINATE	01B2	C16N	31.06.11
14	+U DELTA B LATCH	01B2	E14G	31.23.11
15	+U DELTA PROCESS RESET	01B2	A20N	31.02.31
16	-T DELTA PROCESS	01B2	B12A	31.02.11
17	-T PROCESS LATCH	01B2	B13B	31.02.41
18	-T RDR IMP CB LATCH	01B4	B06A	36.10.21
19	+U IMP CB TRIGGER	01B4	C20E	36.10.21
20	-T READ SCAN GATE (TRIGGER)	01B4	C22N	36.11.11
21	-T R P SCAN GATE	01B4	B10B	36.11.11
22	+U RD SCAN CTRL	01B4	B19B	36.11.11
23	-U ACTIVATE STORAGE	01B2	A17C	31.02.41
24	+U GATE CYCLE OUTPUT	01B2	E14P	31.24.11
25	+U DELTA B CYCLE	01B2	E08B	31.23.11
26	+U B CYCLE LATCH	01B2	E24H	31.26.11
27	+U B CYCLE	01B2	A16G	31.26.11
28	-T 000 SET TIME	01A7	E05N	32.31.11
29	-T TENS B, 2, C	01A7	B12H	32.31.21
30	-T RD PCH FORCE B2	01B4	A08N	36.10.11
31	+U SET COMPLEMENT	01B4	D18N	36.11.11
32	+U RESET A REG ENCODE	01B4	C10H	36.12.21
33				
34	-T RD-PCH ARITH DIGIT INHIBIT	01B4	A18H	36.12.11
35	-T READ TRANSFER TRIGGER	01B4	C24N	36.11.11
36	+U TRANSFER 000	01B4	C23P	36.11.11
37	+U A REG ENCODE SET	01B4	C19A	36.12.21
38	-T B REG TRANSFER	01B4	C21P	36.11.11
39	-T CONTENTS OF STOR LOC 000	—	—	—
40	+U COL BIN CTRL	02B8	F19N	41.11.21
41	+U COL BIN OPR	02B8	F11N	41.11.21
42	-T NORMAL MODE	02B8	F15A	41.11.11
43	+U COL BIN MODE	02B8	F13A	41.11.11
44	+U RD PCH TRANSFER	02B8	F08G	41.11.11
45	-T COL BIN TRANSFER STAR	02B8	F23N	41.11.31
46	-T MOD CTRL TFR	01A8	C10A	32.42.41
47	-T COL BIN MODE PLUS 1	02B8	E15A	41.11.51
48	-T MODIFIER CTRL PLUS 1	01A8	D06N	32.42.11
49	+U RD-PCH SCAN NORMAL	02B8	F07H	41.11.11
50	COL BIN 4 COL BIN 1 COL BIN C "5"	—	—	41.11.31
51	COL BIN B COL BIN 2 COL BIN C "0"	—	—	41.11.31
52	-T SENSE RD 2	01A1	D23A	42.59.11
53	+U COL BIN RD 2 LATCH	02B8	F11H	41.11.11
54	INH COL BIN - B OR A OR B OR 4 OR 2 OR 1 OR C	—	—	41.23.31
55	-T LAST ADDRESS	01B4	D23H	36.16.11
56	+U DELTA PROCESS CONTROL	01B2	B16N	31.02.21
57	+U AFTER ONE TRIGGER	01B4	A25E	36.12.11
58	+U RD SCN COMP	01B4	B12E	36.01.31
59	-T ALL SCAN COMP	01A6	F21N	36.01.11

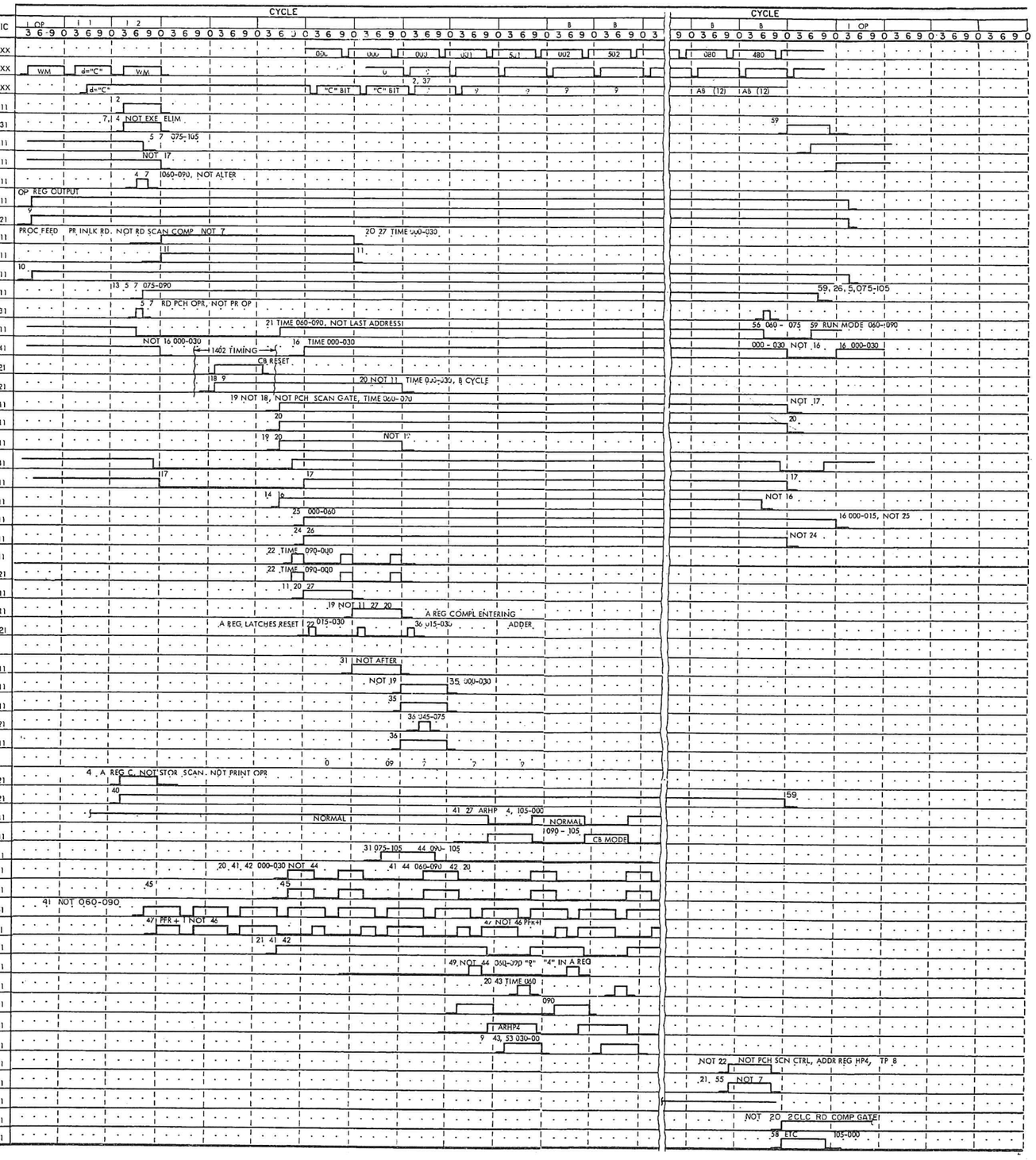


FIGURE 32. COLUMN BINARY READ SEQUENCE

COLUMN BINARY - PUNCH

		SIGNAL NAME	FRAME	TEST POINT	LOGIC
	1	STORAGE ADDRESS REGISTER	—	—	32.35.XX 32.36.XX
	2	B-REGISTER	—	—	35.11.XX
	3	A-REGISTER	—	—	35.16.XX
	4	-T GATED WM	01B2	C25B	31.07.11
	5	-T I/E CHANGE	01B2	BI3H	31.05.31
	6	+U DELTA I CYCLE	01B2	E07N	31.21.11
	7	+U I CYCLE	01B2	E17N	31.24.11
	8	+U I STAR RESTORE	01A8	B17H	32.39.11
	9	+U PUNCH OPR	01B1	C14F	35.27.11
	10	+U I/O OPS	01B2	B25N	31.09.21
	11	+U PUNCH FEED TRIGGER	01B4	E10E	36.24.11
	12	-T PUNCH CLUTCH MAGNET	01B4	A04D	36.24.11
	13	+U A CYCLE ELIMINATE	01B2	C16N	31.06.11
	14	+U DELTA B LATCH	01B2	E14G	31.23.11
	15	+U DELTA PROCESS RESET	01B2	A20N	31.02.31
	16	-T DELTA PROCESS	01B2	B12A	31.02.11
	17	-T PROCESS LATCH	01B2	BI3B	31.02.41
	18	-T PCH SCAN CB TRIGGER	01B4	A20N	36.21.11
	19	+U PUNCH SCAN GATE	01B4	B19H	36.22.11
	20	-T R-P SCAN GATE	01B4	B10B	36.11.11
	21	+U PUNCH SCAN CTRL	01B4	B19N	36.22.11
	22	+U GATE CYCLE OUTPUT	01B2	E14P	31.24.11
	23	-U ACTIVATE STORAGE	01B2	A17C	31.02.41
	24	+U DELTA B CYCLE	01B2	E08B	31.23.11
	25	+U B CYCLE LATCH	01B2	E24H	31.26.11
	26	+U B CYCLE	01B2	A16G	31.26.11
SET STAR TO 100	27	-T 100 SET TIME	01A7	E01N	32.31.11
	28	-T TENS 2 8 C	01A7	BI2H	32.31.21
	29	+U NOT SET UP	01A7	B18C	32.31.21
0 SET IN 100	30	+U PCH FEED RST GATE	01B4	A05N	36.10.11
	31	-T RD PCH FORCE 82	01B4	A08N	36.10.11
COND ZONE ADDR TO PROD ABC AT 12 PCH TIME	32	+U ADD TO 100	01B4	A23H	36.22.11
	33	-T A REG SET B RD PCH	01B4	B24N	36.12.21
	34	+U ZONE ADDER GATE	01B4	A19C	36.12.11
	35	+U RD PCH FORCE ZONE CARRY	01B4	A19P	36.12.11
	36	+U RD PCH ARITH ZONE INH	01B4	A19G	36.12.11
	37	+U FORCE C DIGIT	01B4	A19A	36.12.11
	38	+U PUNCH TRANS	01B4	A24E	36.22.11
A REG SET TO SAME CHAR AS IN B REG	39	+U RESET A REG ENCODE	01B4	C10H	36.12.21
	40	+U A REG ENCODE SET	01B4	C19A	36.12.21
TRANSFER B REG CHAR TO LOC 100 ON 3RD B CYCLE	41	-T B REG TRANSFER	01B4	BI8A	36.22.11
	42	CONTENTS OF STORAGE LOC 100	—	—	—
	43	+U COLUMN BINARY OPERATION	02B8	F11N	41.11.21
	44	-T NORMAL MODE	02B8	F15A	41.11.11
	45	+U COLUMN BINARY MODE	02B8	F13A	41.11.11
	46	+U RD PCH TRANSFER	02B8	F08G	41.11.11
	47	-T COL BIN TRANSFER STAR	02B8	F23N	41.11.31
	48	-T MOD CTRL TFR	01A8	C10A	32.42.41
	49	-T COL BIN MODE PLUS 1	02B8	E15A	41.11.51
	50	-T MODIFIER CTRL PLUS 1	01A8	D06N	32.42.11
	51	+U RD PCH SCAN NORMAL	02B8	F07H	41.11.11
	52	COL BINARY "4"	—	—	41.11.31
	53	COL BINARY "1"	—	—	41.11.31
	54	-T COL BIN PCH DECODE	02B8	F20H	41.23.21
	55	+U COL BIN PCH CHECK DECODE	02B8	F08P	41.23.21
	56	+U COL BIN LAST ADDRESS	02A8	F18P	41.11.11
	57	-T LAST ADDRESS	01B4	D23H	36.16.11
	58	+U DELTA PROCESS CONTROL	01B2	B16N	31.02.21

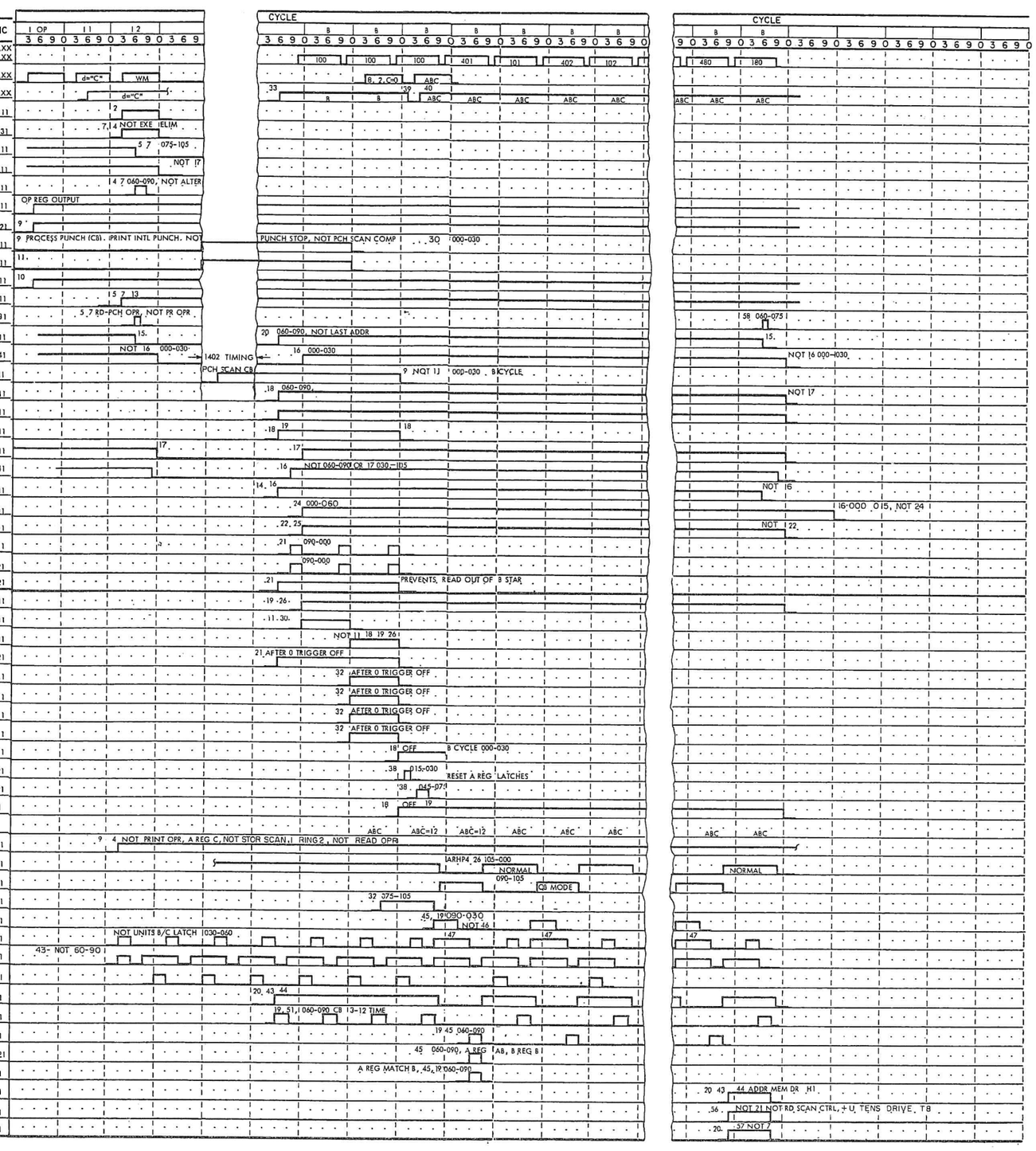


FIGURE 33. COLUMN BINARY PUNCH SEQUENCE

M 503 909 A 1 C ASSUME WM IN 401

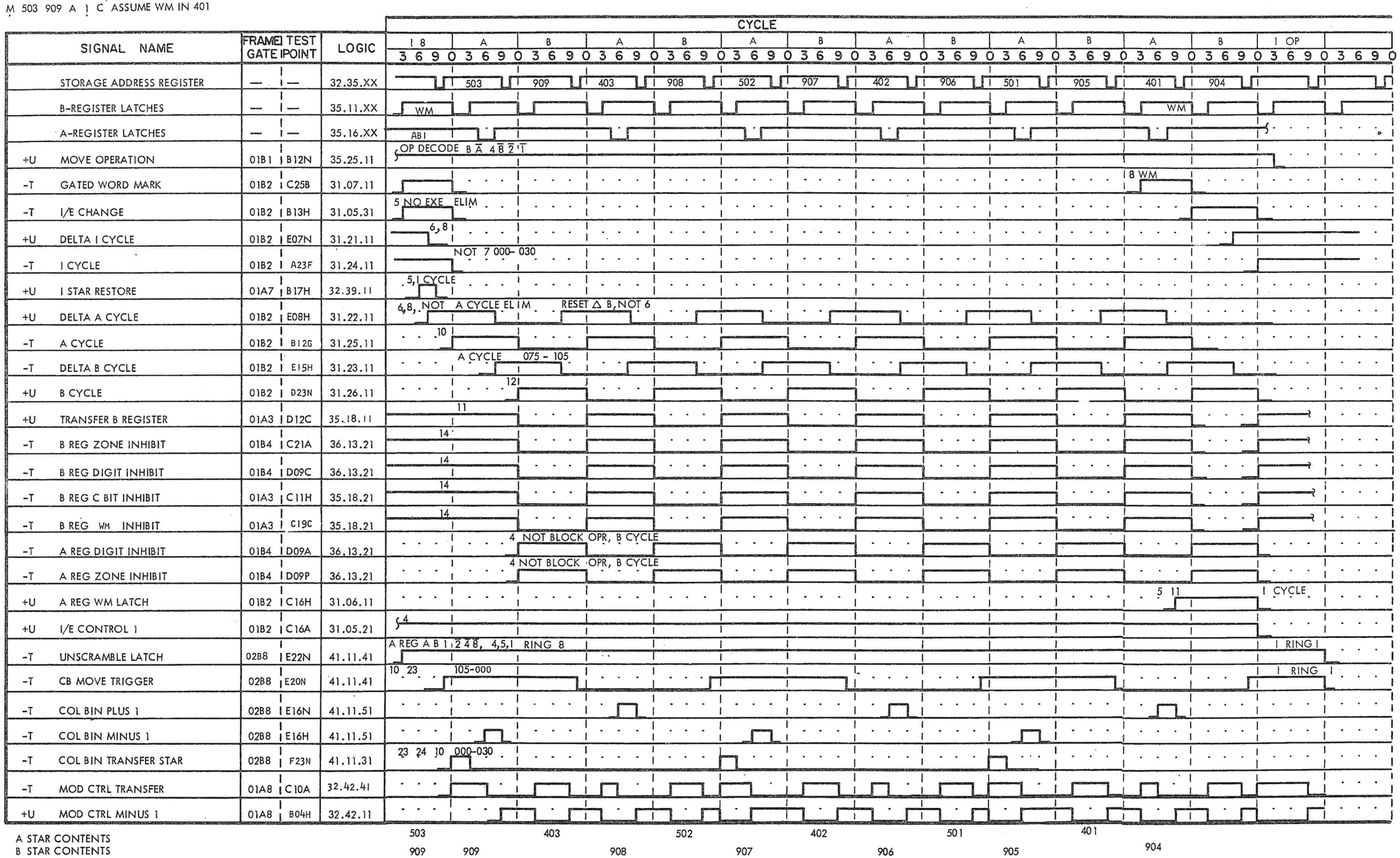
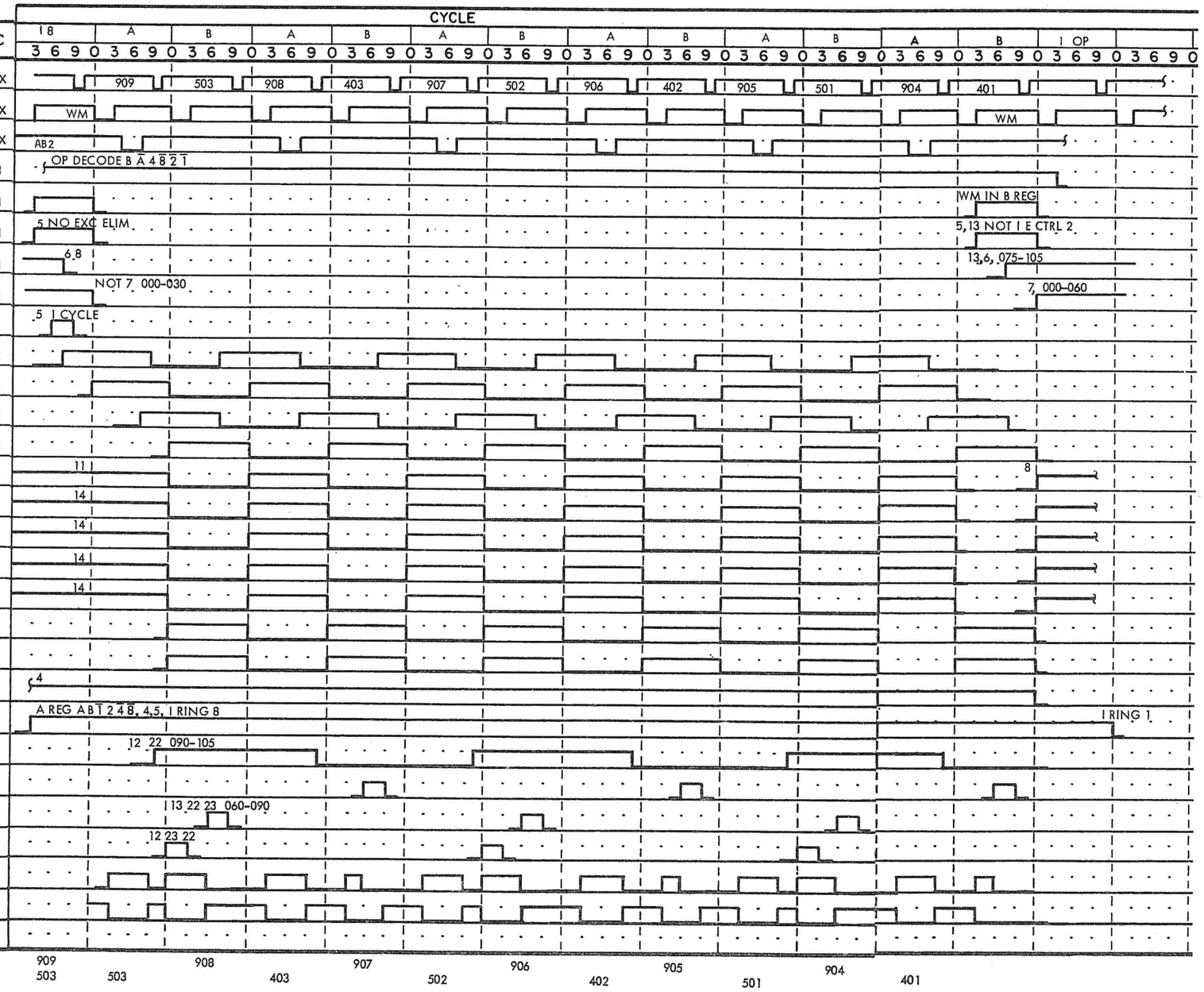


FIGURE 34. MOVE AND UNSCRAMBLE COLUMN BINARY SEQUENCE

M 909 503 B

		SIGNAL NAME	FRAME	TEST GATE POINT	LOGIC
1		STORAGE ADDRESS REGISTER	—	—	32.35.XX
2		B-REGISTER LATCHES	—	—	35.11.XX
3		A-REGISTER LATCHES	—	—	35.12.XX
4	+U	MOVE OPERATION	01B1	B12N	35.25.11
5	-T	GATED WORD MARK	01B2	C25B	31.07.11
6	-T	I/E CHANGE	01B2	B13H	31.05.31
7	+U	DELTA I CYCLE	01B2	E07N	31.21.11
8	-T	I CYCLE	01B2	A23F	31.24.11
9	+U	I STAR RESTORE	01A7	B17H	32.39.11
10	+U	DELTA A CYCLE	01B2	E08H	31.22.11
11	-T	A CYCLE	01B2	B12G	31.25.11
12	-T	DELTA B CYCLE	01B2	E15H	31.23.11
13	+U	B CYCLE	01B2	D23N	31.26.11
14	+U	TRANSFER B REGISTER	01A3	D12C	35.18.11
15	-T	B REG ZONE INHIBIT	01B4	C21A	36.13.21
16	-T	B REG DIGIT INHIBIT	01B4	D09C	36.13.21
17	-T	B REG C BIT INHIBIT	01A3	C11H	35.18.21
18	-T	B REG WM INHIBIT	01A3	C19C	35.18.21
19	-T	A REG DIGIT INHIBIT	01B4	D09A	36.13.21
20	-T	A REG ZONE INHIBIT	01B4	D09P	36.13.21
21	+U	I/E CONTROL I	01B2	C16A	31.05.21
22	-T	SCRAMBLE LATCH	02B8	E22P	41.11.41
23	-T	CB MOVE TRIGGER	02B8	E20N	41.11.41
24	-T	COL BIN PLUS 1	02B8	E16N	41.11.51
25	-T	COL BIN MINUS 1	02B8	E16H	41.11.51
26	-T	COL BIN TRANS STAR	02B8	F23N	41.11.31
27	-T	MOD CTRL TRANSFER	01A8	C10A	32.42.41
28	+U	MOD CTRL MINUS 1	01A8	B04H	32.42.11



A STAR CONTENTS 909 503 908 907 906 905 904
B STAR CONTENTS 503 403 502 402 501 401

FIGURE 35. MOVE AND SCRAMBLE COLUMN BINARY SEQUENCE

	SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1	STORAGE ADDRESS REGISTER	—	—	32.35.XX 32.36.XX
2	B-REGISTER	—	—	35.11.XX
3	A-REGISTER	—	—	35.16.XX
4	-T GATED WM	01B2	C25B	31.07.11
5	-T I/E CHANGE	01B2	B13H	31.05.31
6	+U DELTA I CYCLE	01B2	E07N	31.21.11
7	+U I CYCLE	01B2	E17N	31.24.11
8	+U PUNCH OPR	01B1	C14 F	35.27.11
9	+U I/O OPS	01B2	B25N	31.09.21
10	+U PFR OPR	01B7	D11G	56.15.11
11	-T PROC PUNCH	01B4	F07N	36.24.11
12	+U PUNCH FEED TRIGGER	01B4	E10E	36.24.11
13	+U TRANSFER READ BRUSHES	01B7	F25H	56.15.11
14	+U PCH SCAN CB OR AFTER 9 CAM	01B4	E09A	36.21.11
15	+U IMP CB SET	01B4	F22A	36.10.21
16	+U IMPULSE CB TRIGGER	01B4	C20E	36.10.21
17	-T READ SCAN GATE	01B4	B26N	36.11.11
18	-T R-P SCAN GATE	01B4	B10B	36.11.11
19	-T DELTA PROCESS	01B2	B12A	31.02.11
20	-T PROCESS LATCH	01B2	B13B	31.02.41
21	-T LAST ADDRESS	01B4	D23H	36.16.11
22	-T PCH SCAN CB TRIGGER	01B4	A20N	36.21.11
23	+U PCH SCN TRIGGER	01B4	A22N	36.22.11
24	-T AFTER 9 CB	01B4	C06G	36.21.11
25	-T XFR SCAN	01B7	F04C	56.12.11
26	+U ADDR SET (PFR GEN 001)	01B7	D06A	56.12.11
27	+U (ALTERNATE CYCLE TRIGGER) ADDRESS RD AREA	01B7	D12N	56.12.11
28	-T PFR TRANSFER STAR	01B7	D14H	56.12.11
29	+U PFR FORCE 1	01B7	D13P	56.12.11
30	-T PFR FORCE HUNDREDS C 82	01B7	D15H	56.12.11
31	-T MOD CTRL TRAN	01A8	C10A	32.42.41
32	+U MOD CTRL PLUS 1	01A8	D06N	32.42.11
33	-T PFR CHECK PLANE REG RESET	01B7	A07G	56.10.91
34	-T UPPER TRANS REG	01B7	D23G	56.10.91
35	+U INHIBIT XU 11	01B7	D25N	56.17.41
36	+U PUNCH COMPLETE TRIGGER	01B4	A12E	36.01.21
37	-T ALL SCANS COMPLETE	01A6	F21N	36.01.11

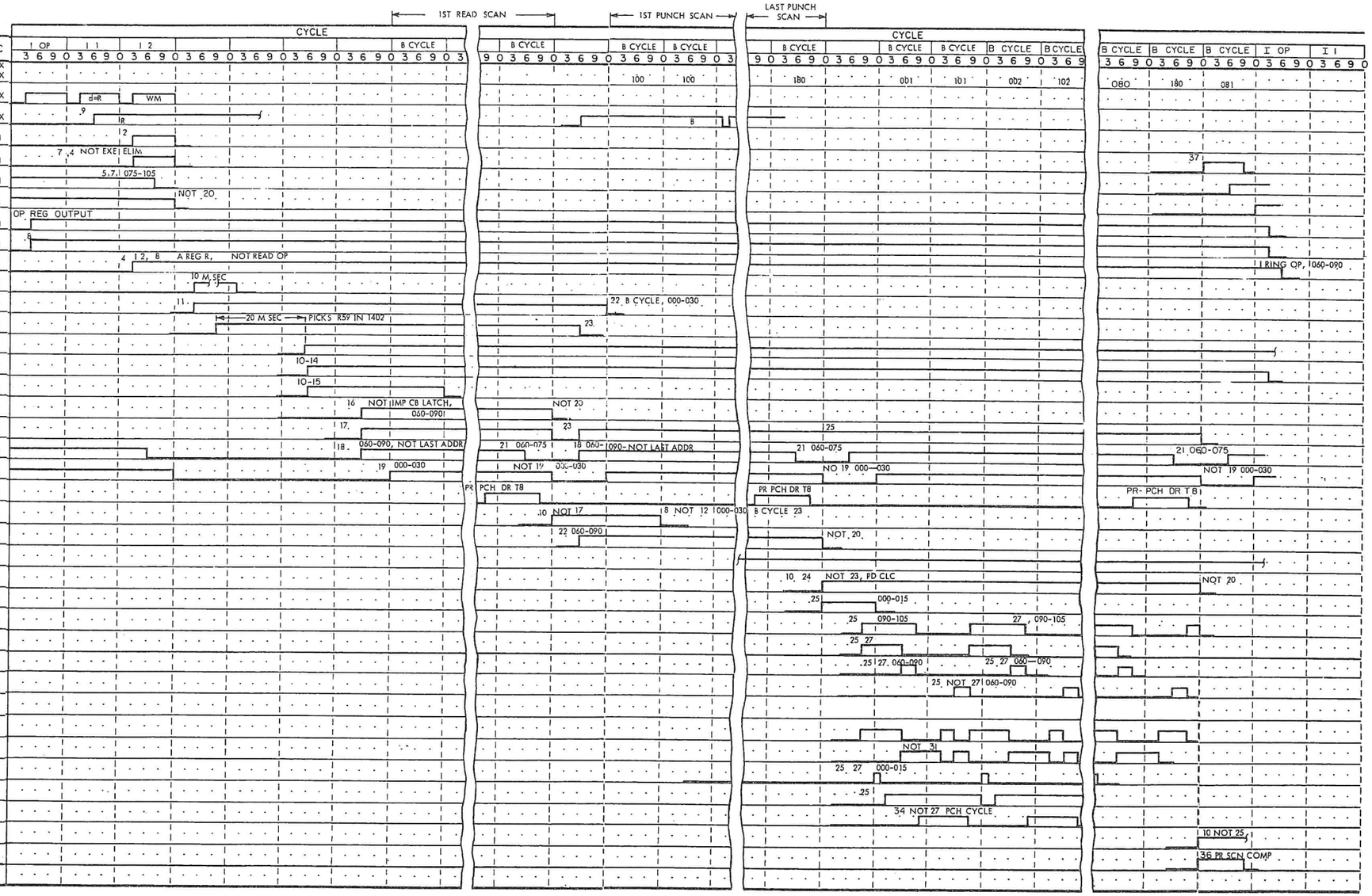


FIGURE 36. PUNCH FEED READ SEQUENCE

FIGURE 36 PUNCH FEED READ SEQUENCE

903 K (d) 905 S 903 K (701) d 908 S 701 M

	SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC	12 / 1 OP (3 6 9 0 3 6 9 0 3)	CYCLE: 15 / 1 OP (9 0 3 6 9 0 3 6 9 0 3 6 9 0)
1	STORAGE ADDRESS REGISTER	—	—	32.35.XX' 32.36.XX	905 905	908 701
2	B-REGISTER	—	—	35.11.XX	S S	S M
3	A-REGISTER	—	—	35.10.XX	d	d
4	+U STACK SEL OPR	01B1	B11N	35.25.11	OP DECODE B·Ā·2·8̄·4̄·1̄	B Ā 2 8̄ 4̄ 1̄
5	-T GATED WM	01B2	C25B	31.07.11	BWM SUPPRESSED BY I-OP	BWM
6	-T I/E CHANGE	01B2	B13H	31.05.31	SUPPRESSED BY 10	
7	+U DELTA I-CYCLE	01B2	E07N	31.21.11	6	
8	-T I-CYCLE	01B2	E19N	31.24.11	7	
9	+U I-STAR RESTORE	01A7	B17H	32.39.11	5 8	
10	+U EXE ELIM	01B2	C08H	31.05.11	4	
11	-T PROGRAM SKIP	01B2	C23A	31.08.11		4 I-RING 5 5
12	+U I-A STAR GATE	01B2	D05C	31.08.11		11
13	+U SET I-RING OP	01B2	F15A	31.30.11		11
14	-T A-STAR GATE OUT	01A7	B16B	32.32.21		7 12 NOT SET-UP
15	-T I-RING OP	01B6	E20N	31.31.31	13 7 015-030 NOT I-B MAR 1	7 13 015-030 NOT I-B MAR 1
16	+U STACKER SELECT d CHAR 1-	01B4	F08A	36.50.11	A-REG 1 OR 2 OR 4 OR 8 4 5 8	
	2-	01B4	F08D			
	4-	01B4	F09H			
	8-	01B4	F08F			
17	+U MODIFIER CONTROL +1	01A8	D06N	32.42.11		
18	-T MODIFIER CONTROL XFER	01A8	C10A	32.42.41		
19	MODIFIER OUTPUT ON BUS LINES	—	—	32.43.XX	906 906	909 702
20	DATA ON INH DRIVE LINES	—	—	—	S S	S M
	I STAR AT END OF CYCLE				905 906	908 702

FIGURE 37. STACKER SELECT K AND STACKER SELECT BRANCH

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1		B-REGISTER (WM) B4 (M)	—	—	35.21.11
2			—	—	
3	+U	MOVE OPERATION	01B1	B12N	35.25.11
4		B REGISTER (WM) CB21 (L)	—	—	35.21.11
5			—	—	
6	+U	LOAD OPERATION	01B1	B11F	35.25.11
7		A REGISTER A84 (%)	—	—	70.11.21
8	+U	UNIT SELECT LATCH, UNIT SELECT	02A2	A06C	70.11.21
9	-T	TAPE +1 MODE	02A	A09D	70.11.21
10					
11	+U	I/O OPS	01B2	B25N	31.09.21
12	+U	A CYCLE ELIMINATION	01B2	C16N	31.06.11
13		A REGISTER BA 2 (B) (ODD REDUNDANCY)	—	—	70.61.31
14	-T	REDUNDANCY LATCH	02A2	B10G	70.61.31
15	+U	UNIT SELECT GATE	02A2	A04N	70.11.21
16		A REGISTER 1, 2, 3, 4, 5, OR 6	—	—	71.11.11 71.11.31
17	+U	SELECT TAPE UNIT (TAPE UNIT LAT 1, 2, 3, 4, 5, OR 6)	02A1	—	71.11.11 71.11.31
18					
19	+U	B REGISTER WORD MARK	01B2	C20E	31.07.11
20	+U	GATED WORD MARK	01B2	B25F	31.07.11
21	+U	I CYCLE	01B2	E17N	31.24.11
22					
23	-T	I/E CHANGE	01B2	B13H	31.05.31
24					
25					
26	+U	DELTA B-CYCLE	01B2	E15H	31.23.11
27					
28	-T	B CYCLE	01B2	D24N	31.26.11
29		A REGISTER B 81 (R)	—	—	70.11.21
30	+U	READ CALL	02A2	A22H	70.11.21
31	+U	CLOCK START CONTROL	02A1	B22Q	71.31.21
32	-T	TAPE CLOCK	02A1	B09N	71.31.21
33	+U	CHECK CHARACTER	02A1	A17E	71.71.21
34	-T	GROUP MARK	02A1	C07A	71.71.21
35	-T	FORCED GROUP MARK	02A2	A19C	70.61.31
36		FORCE GROUP MARK INTO A REGISTER	02A2	A10H	70.61.21
37	-T	FORCED I/E CHANGE	02A2	A13A	70.11.41
38	+U	SET TO I RING OP	01B2	E15A	31.30.11
39					
40	-T	DELTA I CYCLE	01B2	D13A	31.21.11
41	+U	DELTA PROCESS	01B2	A18N	31.02.11 31.31.11
42	+U	UNIT RESET	02A2	B11H	70.11.21

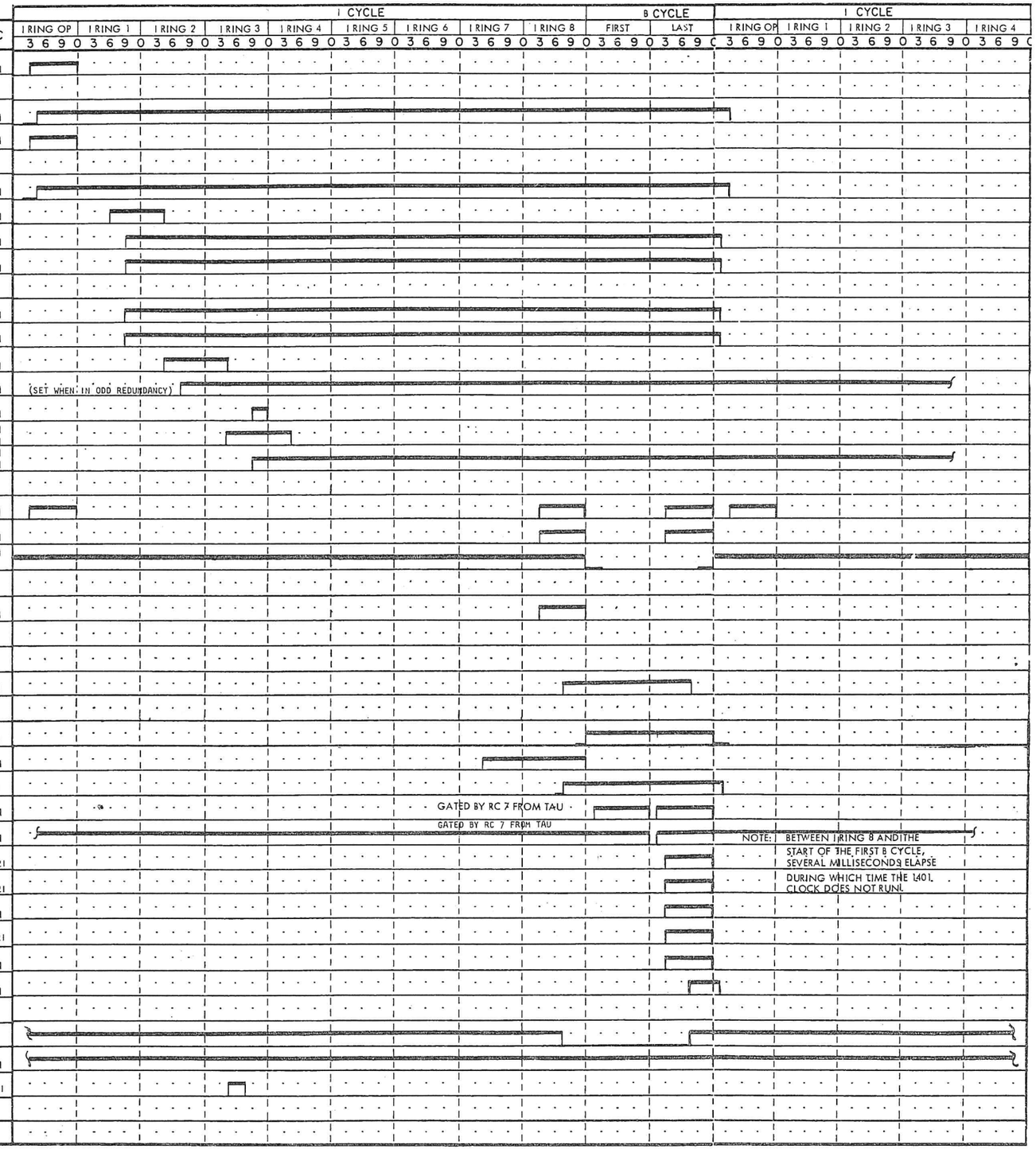


FIGURE 38. MOVE (LOAD) TAPE READ OPERATION

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1		B-REGISTER (WM) B4 (M)	—	—	35.21.11
			—	—	
3	+U	MOVE OPERATION	01B1	B12N	35.25.11
4		B REGISTER (WM) C B21 (L)	—	—	35.21.11
			—	—	
6	+U	LOAD OPERATION	01B1	B11F	35.25.11
7		A REGISTER A84 (%)	—	—	70.11.21
8	+U -T	UNIT SELECT LATCH, UNIT SELECT	02A2	A06C	70.11.21
9	-T	TAPE +1 MODE	02A2	A09D	70.11.21
11	+U	I/O OPS	01B2	B25N	31.09.21
12	+U	A CYCLE ELIMINATION	01B2	C16N	31.06.11
13		A REGISTER BA2 (B) (ODD REDUNDANCY)	—	—	70.61.31
14	-T	REDUNDANCY LATCH	02A2	B10G	70.61.31
15	+U	UNIT SELECT GATE	02A2	A04N	70.11.21
16		A REGISTER 1, 2, 3, 4, 5, OR 6	—	—	71.11.11 71.11.31
17	+U	SELECT TAPE UNIT (TAPE UNIT LATCH 1, 2, 3, 4, 5, OR 6)	02A1	—	71.11.11 71.11.31
18	+U	GATE B REGISTER CONTENTS INTO THE B ADDRESS REGISTER	—	—	—
19	+U	B REGISTER WORD MARK	01B2	C20E	31.07.11
20	+U	GATED WORD MARK	01B2	C25B	31.07.11
21	+U	I CYCLE	01B2	E17N	31.05.31
23	-T	I/E CHANGE	01B2	B13H	31.05.31
26	+U	DELTA B CYCLE	01B2	E15H	31.23.11
28	-T	B CYCLE	01B2	D24N	31.26.11
29		A REGISTER A42 (W)	—	—	70.11.21
30	+U	WRITE CALL	02A2	B20H	70.11.21
31	-T	CLOCK START CONTROL LATCH	02A1	B22Q	71.31.21
32	-T	TAPE CLOCK	02A1	B09N	71.31.21
33	+U	CHECK CHARACTER (FROM TAU)	02A1	A17E	71.71.21
35	-T	FORCED GROUP MARK	02A2	A19C	70.61.31
36	-T	UNIT WRITE GATE	02A2	B10A	70.51.31
37	-T	FORCED I/E CHANGE	02A2	A13A	70.11.41
38	+U	SET TO I RING OP	01B2	E15A	31.30.11
40	+U	DELTA I CYCLE	01B2	D13A	31.31.11
41	+U	DELTA PROCESS	01B2	A18N	31.62.11
42	+U	UNIT RESET	02A2	B11H	70.11.21
43	+U +P	DISCONNECT / DISCONNECT CALL TO TAU	02A2 / 02A2	B17N / B17P	70.51.21

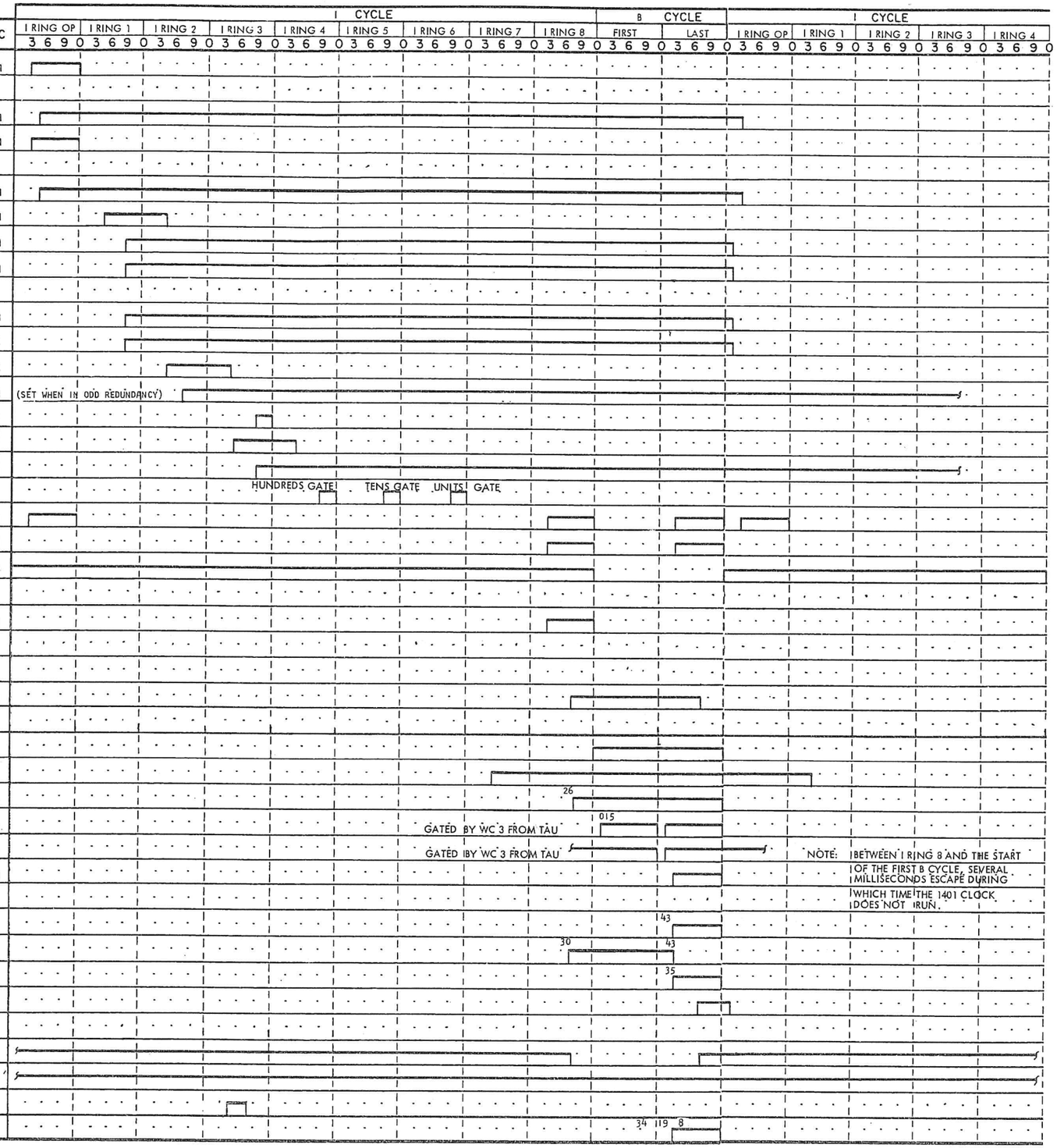


FIGURE 39. MOVE (LOAD) WRITE OPERATION

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1	-T	DELTA B CYCLE LATCH	01B2	E09E	31.23.11
2	+U	DELTA B CYCLE	01B2	E15H	31.23.11
3	-T	B CYCLE	01B2	D24H	31.26.11
4	+U	LOAD OPERATION	01B1	B11F	35.25.11
5		DATA FROM TAPE	—	—	70.61.21
6		C REGISTER A841 (WS CHAR)	—	—	70.61.21
7	-T	WS READ	02A2	A01H	70.61.31
8	+U	TAPE READDRESS	02A2	B20A	70.51.31
9	-T	READDRESS LATCH (CY CONTROL)	01B2	C09N	31.04.11
10	-T	NOT READDRESS LATCH	02A2	A17H	70.51.31
11	+U	INHIBIT WORD MARK	02A2	A10A	70.61.31
12			—	—	
13			—	—	
14		RESET B ADDRESS REGISTER	—	—	32.33.11 32.33.21
15		GATE INTO B ADDRESS REGISTER FROM MODIFIER	—	—	32.33.11 32.33.21
16		GATE OUT THE B ADDRESS REGISTER	01A7	B21G	32.33.31
17	-T	NOT ADDRESS REGISTER RESET	01B2	F08P	31.04.11
18		GATE ADDRESS REG CONTENTS INTO MOD	—	—	32.39.21

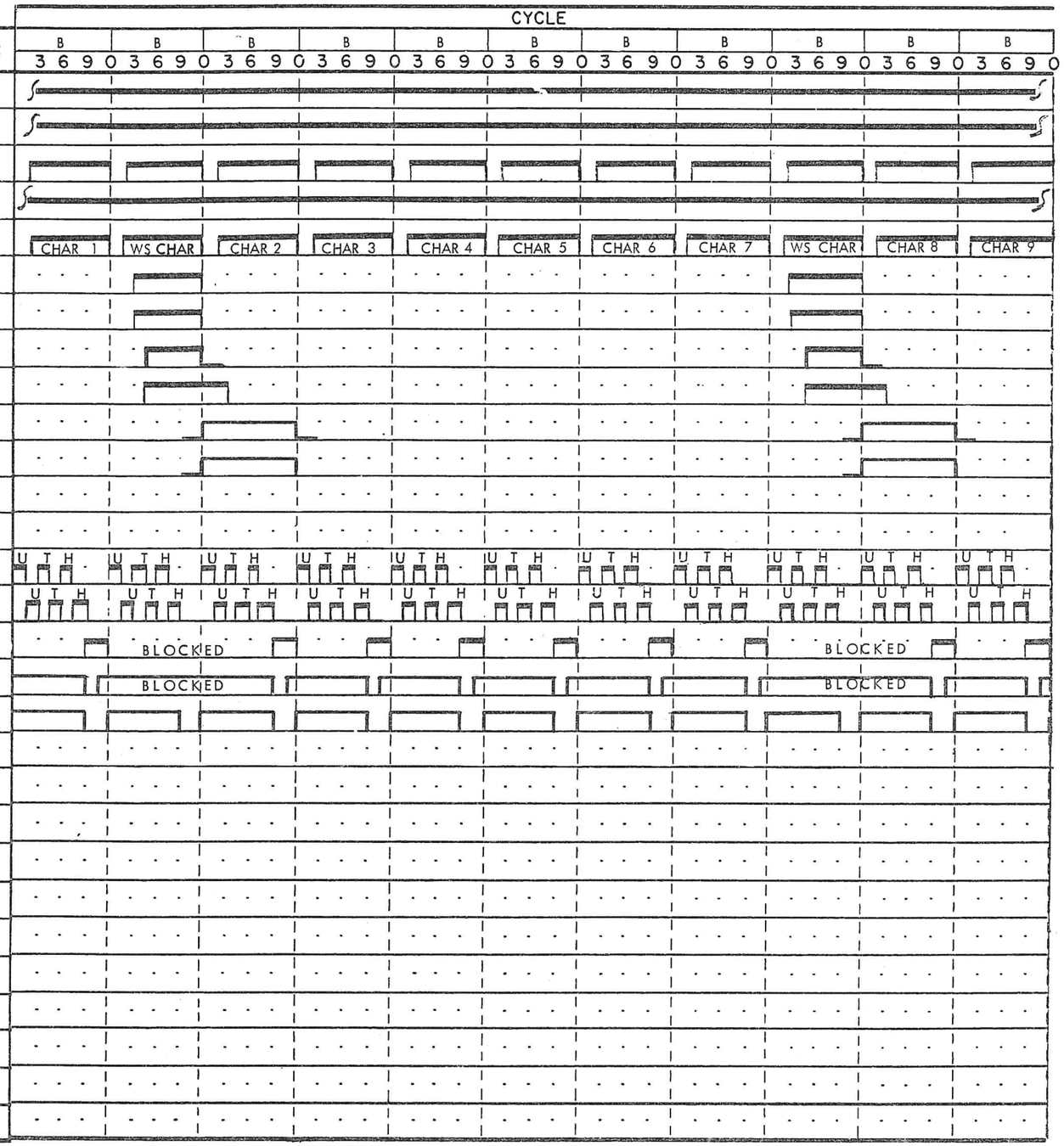


FIGURE 40. LOAD TAPE AND READ A WORD SEPARATOR CHARACTER

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1	-T	DELTA B CYCLE LATCH	01B2	F09F	31.23.11
2	+U	DELTA B CYCLE	01B2	E15H	31.23.11
3	-T	B CYCLE	01B2	D24N	31.26.11
4		DATA READ FROM STORAGE	—	—	70.51.21
5	+U	LOAD OPERATION	01B1	B11F	35.25.11
6	-T	WRITE CALL	02A2	A03B	70.11.21
7	-T	B REGISTER WORD MARK	02A2	B10B	70.51.21
8	-T	READDRESS LATCH	02A2	A17E	70.51.31
9	+T	NOT READDRESS LATCH	02A2	A17H	70.51.31
10	+U	TAPE READDRESS	02A2	B20A	70.51.31
11	-T	READDRESS LATCH (CY CONTROL)	01B2	C09N	31.04.11
12	-T	WS ON TAPE	02A2	B12B	70.51.31
13		FORCE LINES A, 8, 4, 1 TO TAU	—	—	70.51.21
14			—	—	
15		RESET B ADDRESS REGISTER	—	—	32.33.11
16		GATE INTO B ADDRESS REGISTER FROM MODIFIER	—	—	32.33.11
17	-T	GATE OUT THE B ADDRESS REGISTER	01A7	B21G	32.33.31
18	-T NOT	ADDRESS REGISTER RESET	01B2	F08P	31.04.11
19			—	—	
20		GATE ADDRESS REG CONTENTS INTO MOD AND INTO STORAGE	—	—	—

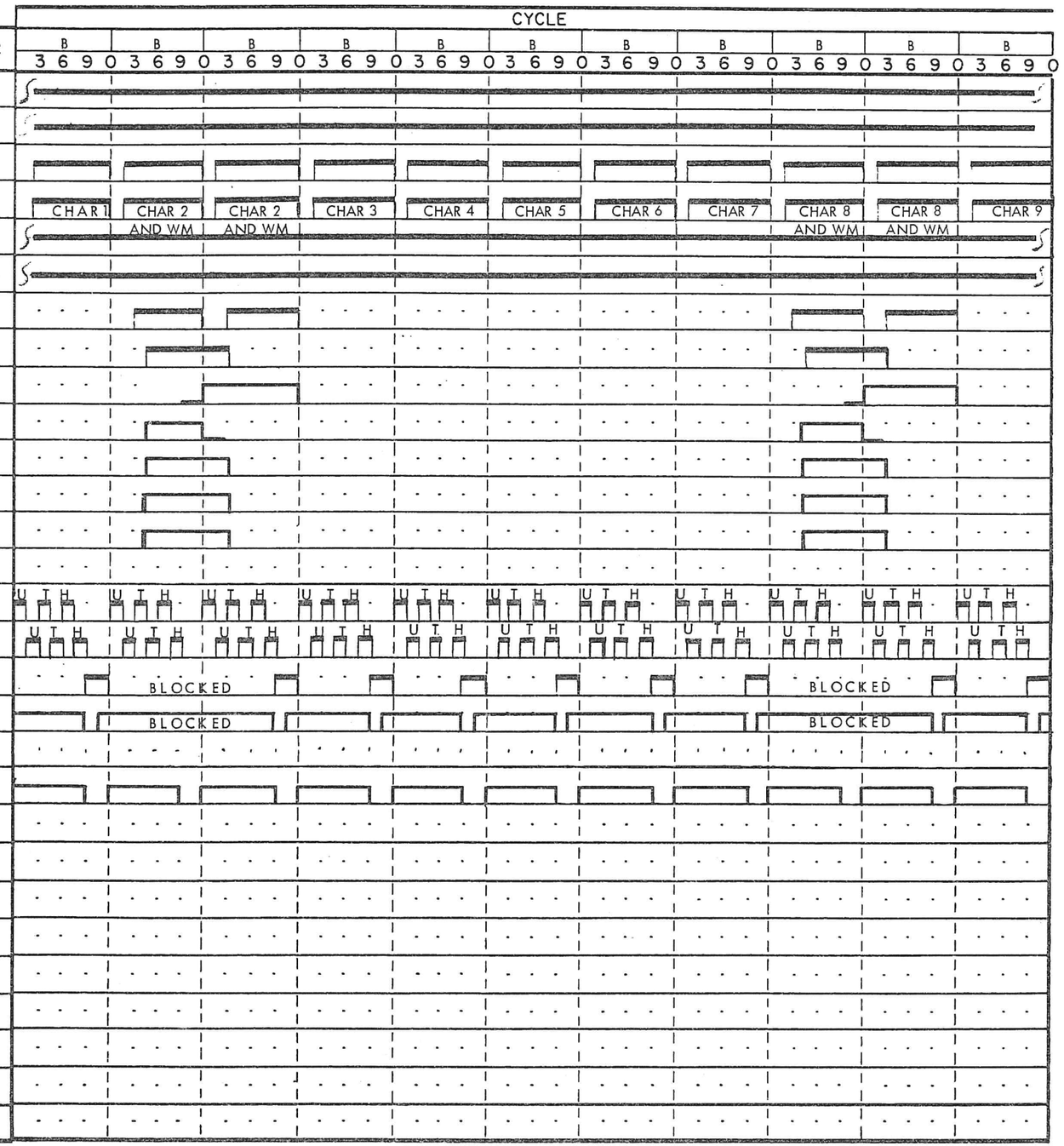


FIGURE 41. LOAD TAPE AND WRITE A WORD SEPARATOR CHARACTER

U% U1 (d) B d = B

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1	-T	DELTA I CYCLE	01B2	B12H	31.21.11
2		B-REGISTER (WM) A4 (U)	—	—	35.21.11
3		OP DECODE (WM) A4 (U)	—	—	35.26.11
4	+U	U OP CODE	01B2	C12F	35.26.11
5	+U	EXECUTE ELIMINATE	01B2	C08H	31.05.11
6		A-REGISTER A 84 (%)	—	—	70.11.21
7	-T	UNIT SELECT LATCH, UNIT SELECT	02A2	B05N	70.11.21
8	-T	TAPE +1 MODE	02A2	A09D	70.11.21
9	+U	I/O OPERATE	01B2	B25N	31.09.21
10	+U	A CYCLE ELIMIN^TION	01B2	C16N	31.06.11
11					
12					
13	+U	UNIT SELECT GATE	02A2	A04N	70.11.21
14		A REGISTER 1	—	—	71.11.11
15	+U	SELECT TAPE UNIT (TAPE UNIT LATCH 1)	—	—	71.11.11
16	+U	B REGISTER WORD MARK	01B2	C20E	31.07.11
17	+U	U OP CODE GATE	02A1	A04N	71.11.21
18		A REGISTER BA 2 (B)	—	—	71.11.21
19	+P	BACKSPACE TO TAU	02A1	B23B	71.11.21
20	+U	GATED WORD MARK	01B2	B25F	31.07.11
21	+U	SET I OP LATCH	01B2	D21B	31.30.11
22	-T	TAPE CLOCK	02A1	B09N	71.31.21
23					
24	+U	UNIT RESET	02A2	B11H	70.11.21

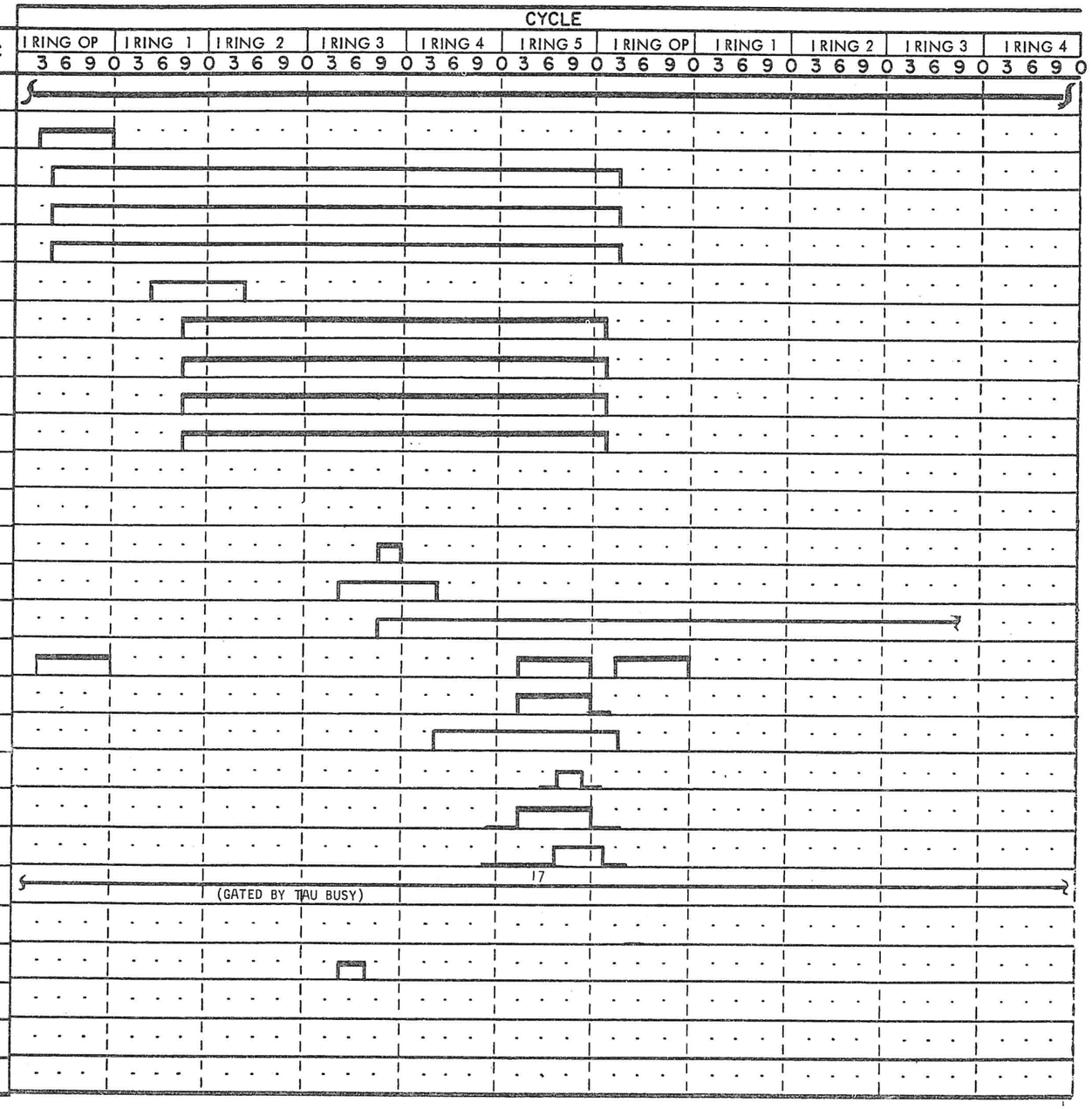


FIGURE 42. BACKSPACE TAPE OPERATION

U% UI (d) B d= E

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1	-T	DELTA I CYCLE	01B2	B12H	31.21.11
2		B-REGISTER (WM) A4 (U)	—	—	35.21.11
3		OP DECODE (WM) A4 (U)	—	—	35.26.11
4	+U	U OP CODE	01B2	C12F	35.26.11
5	+U	EXECUTE ELIMINATE	01B2	C08H	31.05.11
6		A-REGISTER A84 (%)	—	—	70.11.21
7	-T	UNIT SELECT LATCH, UNIT SELECT	02A2	B05N	70.11.21
8	-T	TAPE +1 MODE	02A2	A09D	70.11.21
9	+U	I/O OPS	01B2	B25N	31.09.21
10	+U	A CYCLE ELIMINATION	01B2	C16N	31.06.11
11					
12					
13	+U	UNIT SELECT GATE	02A2	A04N	70.11.21
14		A REGISTER I	—	—	71.11.11
15	+U	SELECT TAPE UNIT (TAPE UNIT LATCH I)	—	—	71.11.11
16	+U	B-REGISTER WORD MARK	01B2	C20E	31.07.11
17	+U	U OP CODE GATE	02A2	A05B	70.11.21
18		A-REGISTER CBA41 (E)	—	—	71.11.21
19	-T	ERASE CALL TO TAU	02A1	B18H	71.11.21
20	+U	GATED WORD MARK	01B2	B25F	31.07.11
21	+U	SET I OP LATCH	01B2	D21B	31.30.11
22	-T	TAPE CLOCK	02A1	C10P	71.31.21
23					
24	+U	UNIT RESET	02A2	B11H	70.11.21

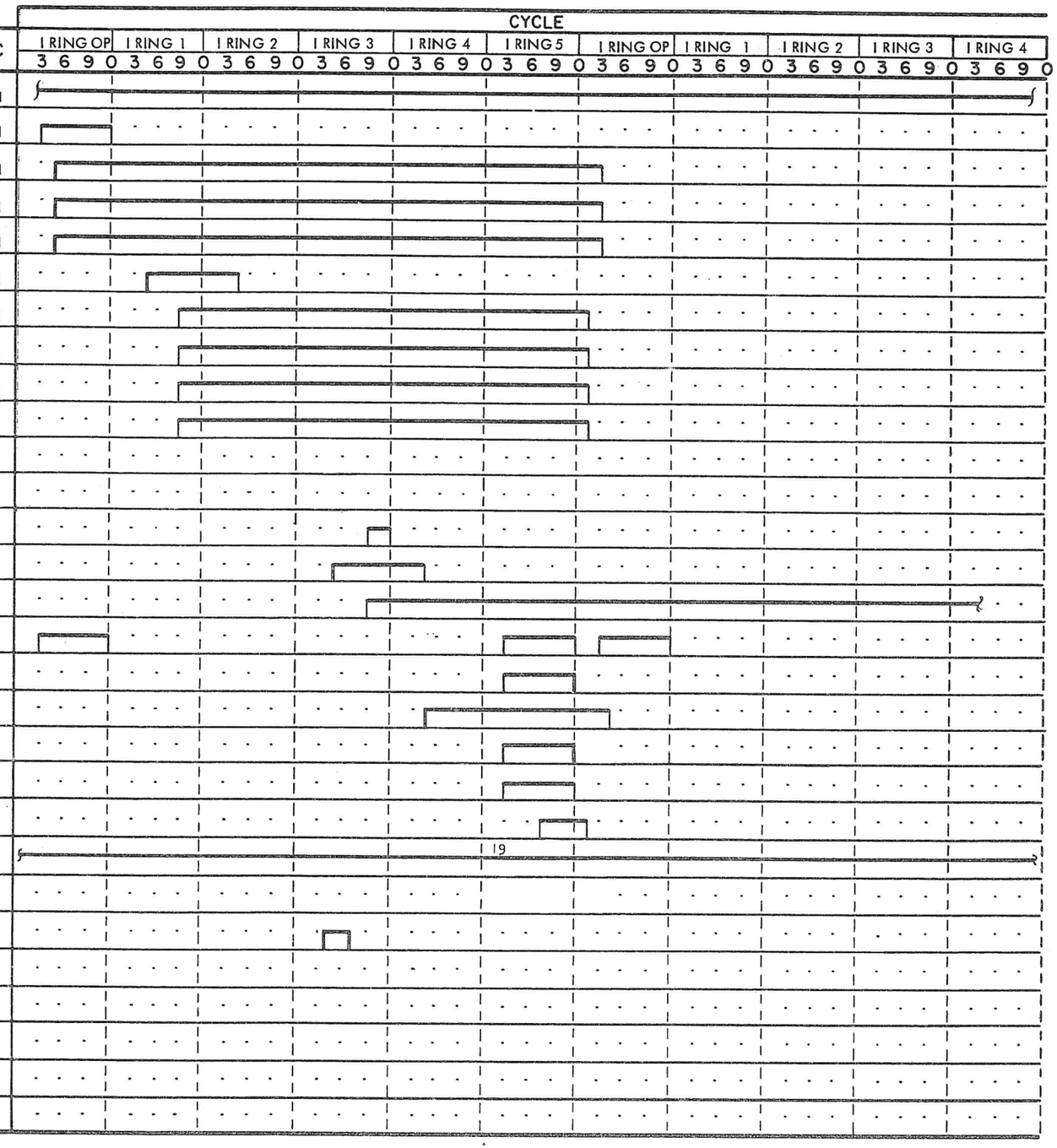


FIGURE 43. ERASE TAPE OPERATION

U % U I M B

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1	-T	DELTA I-CYCLE	01B2	B12H	31.21.11
2		B-REGISTER (WM) A4 (U)	—	—	35.21.11
3		OP DECODE (WM) A4 (U)	—	—	35.26.11
4	+U	U OP CODE	01B2	C12F	35.26.11
5	+U	EXECUTE ELIMINATE	01B2	C08H	31.05.11
6		A REGISTER A84 (%)	—	—	70.11.21
7	-T	UNIT SELECT LATCH, UNIT SELECT	02A2	B05N	70.11.21
8	-T	TAPE +1 MODE	02A2	A09D	70.11.21
9	+U	I/O OPS	01B2	B25N	31.09.21
10	+U	A CYCLE ELIMINATION	01B2	C16N	31.06.11
11			—	—	
12					
13	+U	UNIT SELECT GATE	02A2	A04N	70.11.21
14		A REGISTER 1	—	—	71.11.11
15	-T	SELECT TAPE UNIT (TAPE UNIT LATCH 1)	02A1	B01E	71.11.11
16	+U	B-REGISTER WORD MARK	01B2	C20E	31.07.11
17	+U	U OP CODE GATE	02A2	A05B	70.11.21
18		A-REGISTER CA4 (M)	—	—	71.11.21
19	-T	WRITE TAPE MARK CALL	02A2	C05N	70.11.41
20	+U	GATED WORD MARK	01B2	B25F	31.07.11
21	+U	SET I OP LATCH	01B2	D21B	31.30.11
22	-T	TAPE CLOCK	02A1	B09N	71.31.21
23					
24	+U	UNIT RESET	02A2	B11H	70.11.21

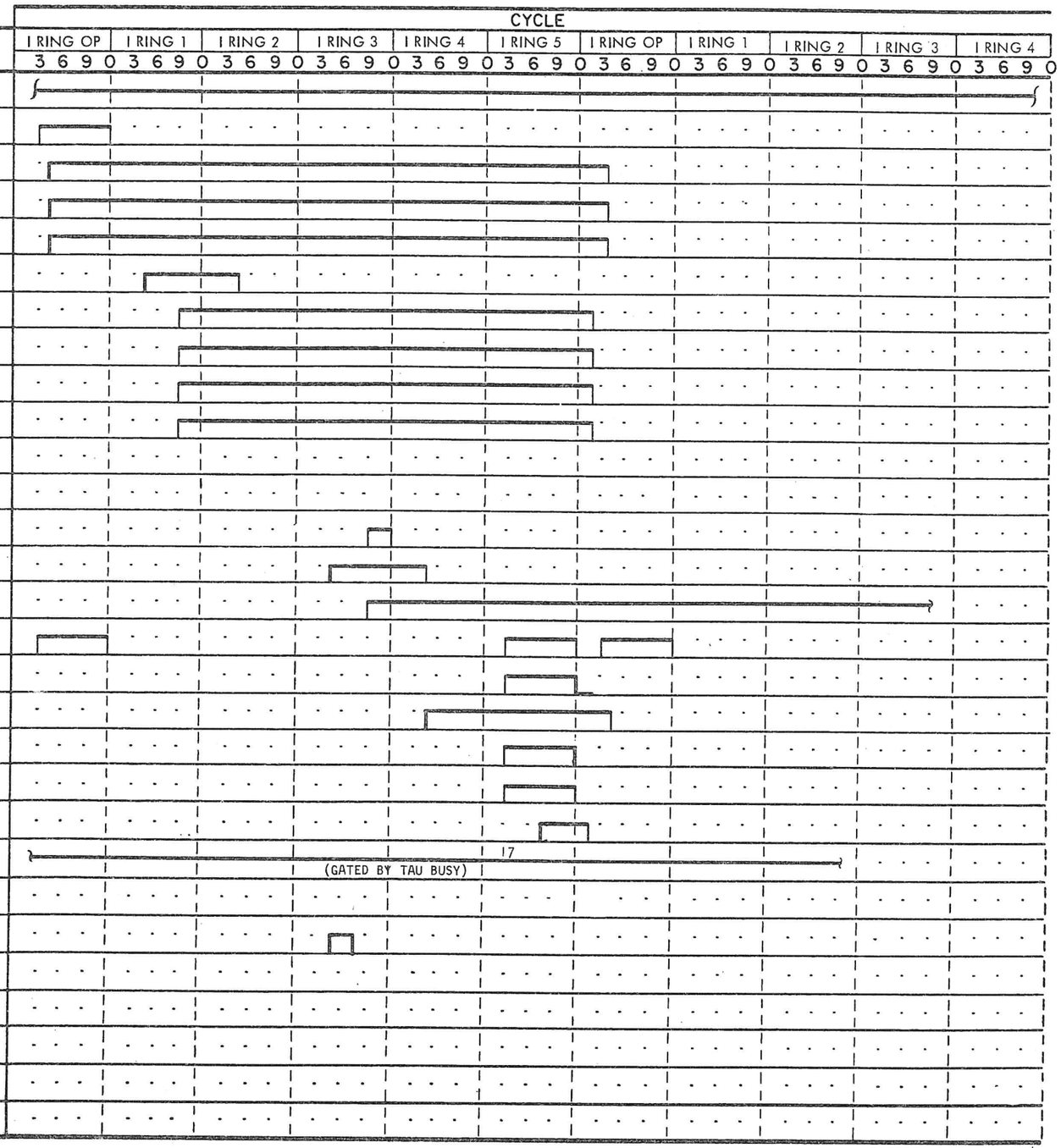


FIGURE 44. WRITE TAPE MARK

U % U I R B

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1	-T	DELTA I CYCLE	01B2	B12H	31.21.11
2		B-REGISTER (WM) A4 (U)	—	—	35.21.11
3		OP DECODE (WM) A4 (U)	—	—	35.26.11
4	+U	U OP CODE	01B2	C12F	35.26.11
5	+U	EXECUTE ELIMINATE	01B2	C08H	31.05.11
6		A REGISTER A84 (%)	—	—	70.11.21
7	-T	UNIT SELECT LATCH, UNIT SELECT	02A^	B05N	70.11.21
8	-T	TAPE +1 MODE	02A2	A09D	70.11.21
9	+U	I/O OPS	01B2	B25N	31.09.21
10	+U	A CYCLE ELIMINATION	01B2	C16N	31.06.11
11			—	—	
12					
13	+U	UNIT SELECT GATE	02A2	A04N	70.11.21
14		A-REGISTER 1	—	—	71.11.11
15	-T	SELECT TAPE UNIT (TAPE UNIT SELECT 1)	02A1	B01E	71.11.11
16	+U	B REGISTER WORD MARK	01B2	C20E	70.11.21 31.07.11
17	+U	U OP CODE GATE	02A2	A05N	70.11.21
18		A REGISTER B81 (R)	—	—	71.11.21
19	-T	REWIND	02A1	B18N	71.11.21
20	+U	GATED WORD MARK	01B2	B25B	31.07.11
21	+U	SET I OP LATCH	01B2	E14A E20H	31.30.11
22	-T	TAPE CLOCK	02A1	B09N	71.31.21
23					
24	+U	UNIT RESET	02A2	B11H	70.11.21

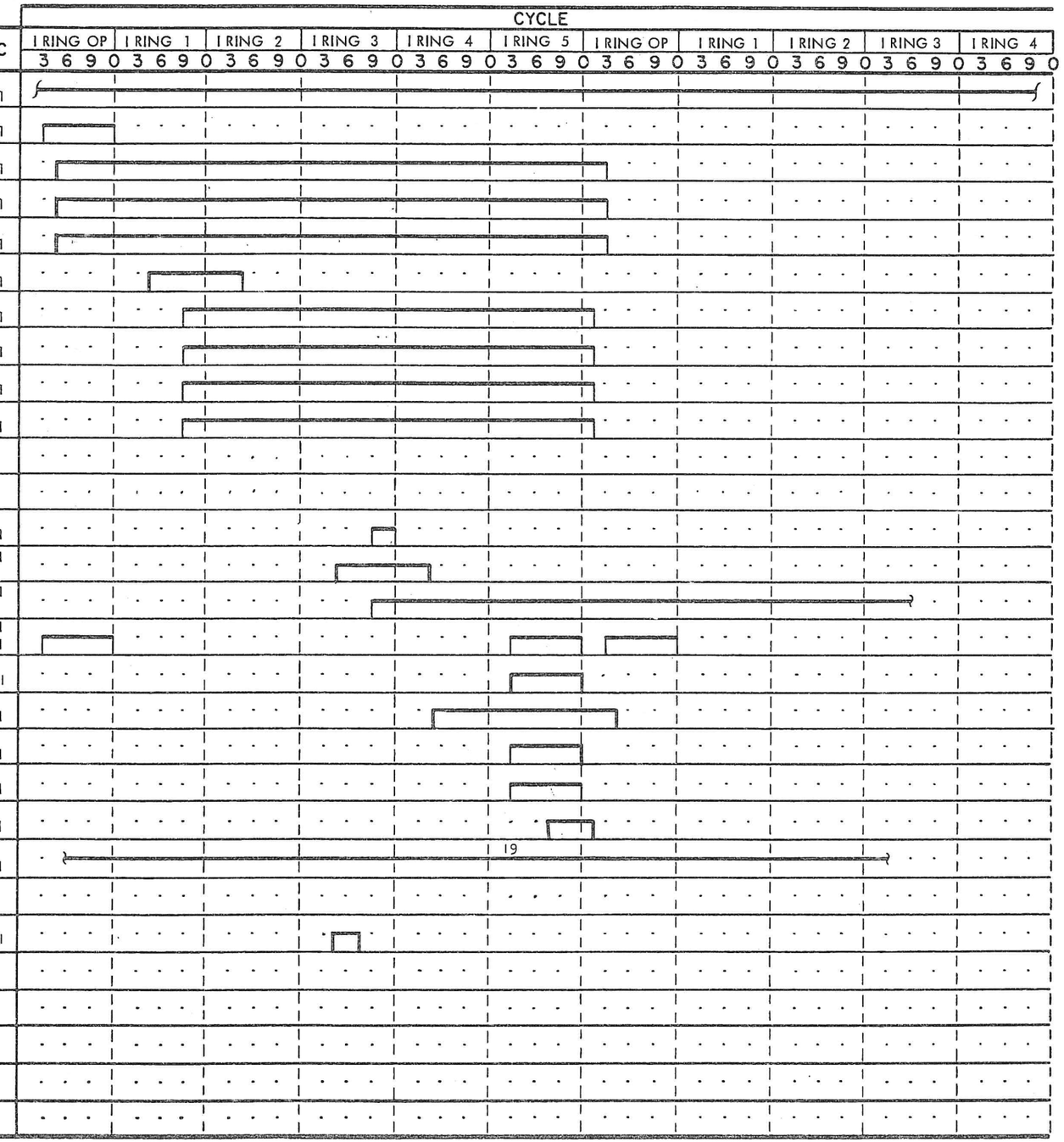


FIGURE 45. REWIND TAPE OPERATION

U % U I (d) B d = U

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1	-T	DELTA I CYCLE	01B2	B12H	31.21.11
2		B-REGISTER (WM) A4 (U)	—	—	35.21.11
3		OP DECODE (WM) A4 (U)	—	—	35.26.11
4	+U	U OP CODE	01B2	C12F	35.26.11
5	+U	EXECUTE ELIMINATE	01B2	C08H	31.05.11
6		A REGISTER A84 (%)	—	—	70.11.21
7	+U -T	UNIT SELECT LATCH, UNIT SELECT	02A2	B05N	70.11.21
8	-T	TAPE +1 MODE	02A2	A09D	70.11.21
9	+U	I/O OPS	01B2	B25N	31.09.21
10	+U	A CYCLE ELIMINATION	01B2	C16N	31.06.11
11					
12					
13	+U	UNIT SELECT GATE	02A2	A04N	70.11.21
14		A REGISTER 1	—	—	71.11.11
15	+U	SELECT TAPE UNIT (TAPE UNIT LATCH 1)	—	—	71.11.11
16	-T	B REGISTER WORD MARK	01B2	C20E	70.11.21 31.07.11
17	+U	U OP CODE GATE	02A2	A05B	70.11.21
18		A REGISTER CA4 (U)	—	—	71.11.21
19	+N	REWIND UNLOAD TO TAU	02A1	B17P	71.11.21
20	+U	GATED WORD MARK	01B2	B25F	31.07.11
21	+U	SET I OP LATCH	01B2	D21B	31.30.11
22	-T	TAPE CLOCK	02A1	B09N	71.31.21
23					
24	+U	UNIT RESET	02A2	B11H	70.11.21

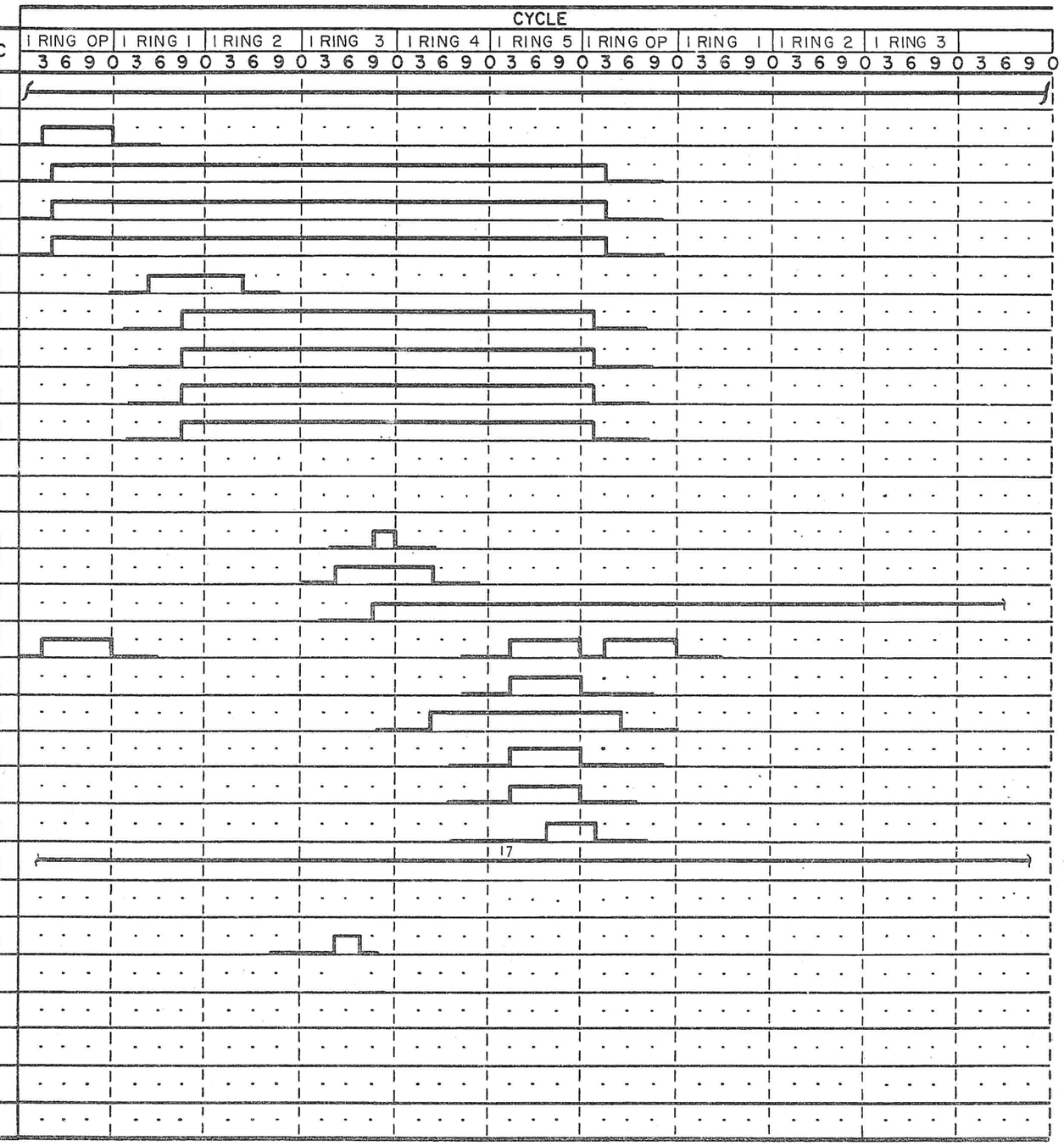


FIGURE 46. REWIND AND UNLOAD TAPE

B (AAA)(d) B

d = K (END OF FILE) OR L (TAPE ERROR)
AAA - S

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1	-T	DELTA I CYCLE	01B2	B12H	31.21.11
2		B REGISTER	—	—	35.21.11
3		OP DECODE (WM) CBA 2 (B)	—	—	35.26.11
4	-T	BRANCH OPERATION	02A1	A05G	70.11.41
5		GATE B REGISTER CONTENTS INTO A ADDRESS REG (DIGIT BY DIGIT)	—	—	32.42.11
6	+U	EXECUTE ELIMINATE	01B2	C08H	31.05.11
7		A REGISTER CB2 (K) OR A REGISTER B21 (L)	—	—	70.11.41 71.11.11
9	-T	B REGISTER WORD MARK	02A2	A15E	70.51.31
10	+U	GATED WORD MARK	01B2	B25F	31.07.11
11	+U	TAU ERROR OR	02A2	A25K	70.11.41
12	+U	SEL +TI ON	02A2	A25N	70.11.41
14	+U	TAPE PROGRAM SKIP	02A2	C04C	70.11.41
15	-T	PROGRAM SKIP LATCH	01B2	C23A	31.08.11
16	+U	SET TO I RING OP LATCH	01B2	E14A	31.30.11
17	-T	A ADDRESS REGISTER GATE OUT	01A7	B16B	32.32.21

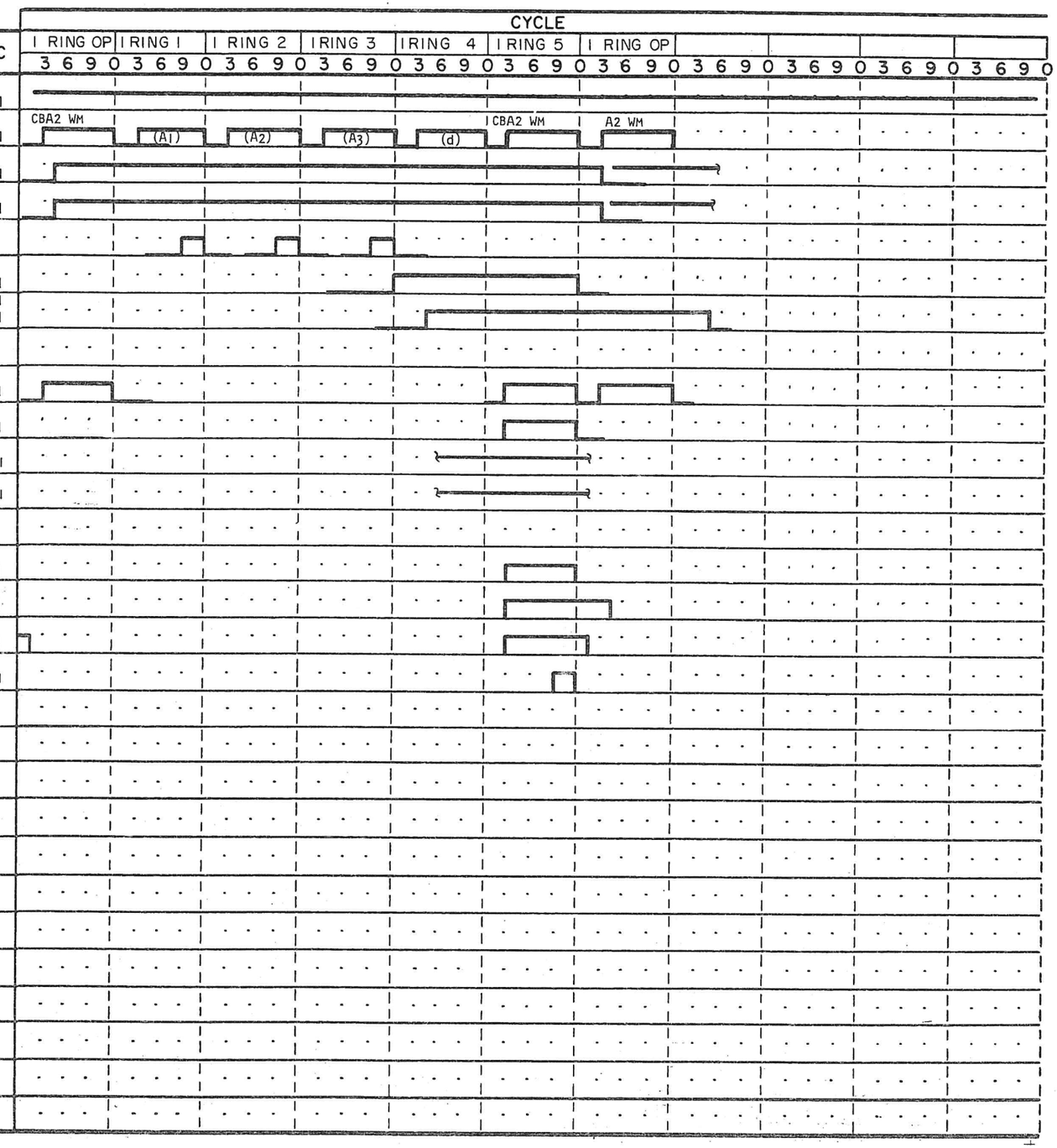


FIGURE 47. TAPE END OF FILE INDICATOR TEST AND TAPE TRANSMISSION ERROR TEST

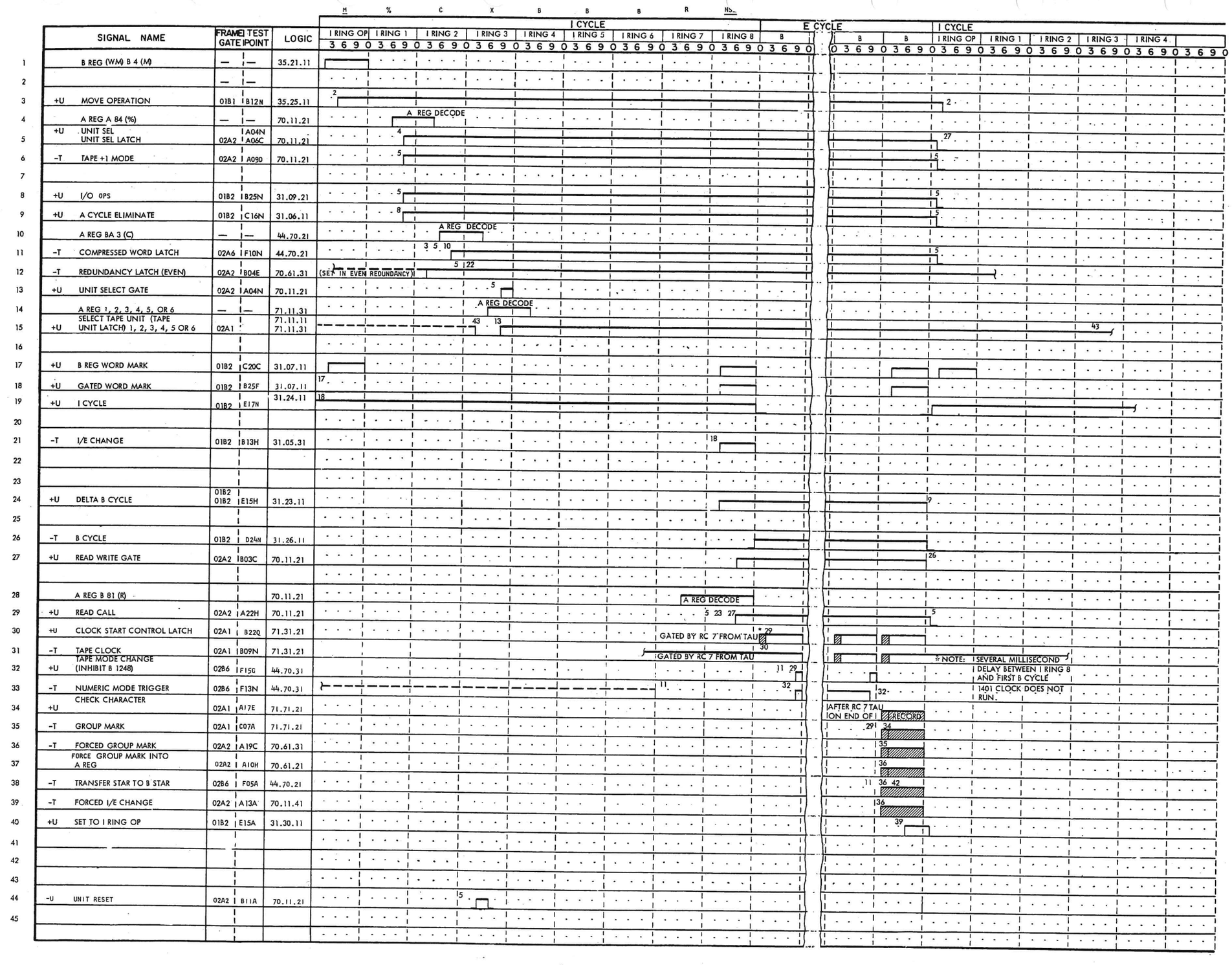


FIGURE 48. MOVE COMPRESSED TAPE READ OPERATION

399 GM
040 X 412 714
047 M

A-FIELD DATA GM Δ20985ΔDRAKE GM
B-FIELD DATA b bbbbbb b bb b bb b

RESULTANT A-FIELD (AFTER MOVE ZERO INSERT) Δ20985ΔDRAKE GM
RESULTANT B-FIELD (AFTER MOVE ZERO INSERT) GM Δ 0020985Δ DRAKE GM

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1		STORAGE ADDRESS REGISTER	—	—	32.35.XX 32.36.XX
2		B-REGISTER	—	—	35.11.XX
3		A-REGISTER	—	—	35.16.XX
4	-T	INDEX PREVENT GATED WM	02B6	F05N	44.70.21
5		EXPAND OP X (A 124)	01B1	A21H	44.70.11
6	-T	GATED WM	01B2	C25B	31.07.11
7	-T	I/E CHANGE	01B2	B13H	31.05.31
8	+U	DELTA I-CYCLE	01B2	E07N	31.21.11
9	-T	I-CYCLE	01B2	A23F	31.24.11
23	+U	FIRST B BIT	02B6	F25E	44.70.41
10	+U	DELTA A-CYCLE	01B2	E09N	31.22.11
11	-T	A-CYCLE	01B2	B12G	31.25.11
12	-T	DELTA B-CYCLE	01B2	E09E	31.23.11
13	+U	B-CYCLE	01B2	D23N	31.26.11
14	-T	B-REG ZONE INHIBIT	01A3	D18P	35.18.21
15	-T	B-REG DIGIT INHIBIT	01A3	D16A	35.18.31
16	-T	B-REG C-BIT INHIBIT	01A3	C11H	35.18.21
17	+U	INHIBIT WM	01A3	E15D	35.14.51
18	+U	XFER A REG DIGIT ZONE	02B6	F26G	44.70.21
19	-T	A-REG ZONE INHIBIT	01A3	F20H	35.18.41
20	-T	A-REG DIGIT INHIBIT	01A3	B13H	35.18.41
21	+U	DELTA CHARACTER	02B6	F19N	44.70.31
22	-T	NUMERIC MODE	02B6	F13N	44.70.31
24		2ND A-REG B BIT	02B6	F23H	44.70.41
25	+U	2ND B-BIT TRIGGER	02B6	F24N	44.70.41
26	+U	A-CYCLE ELIMINATE	02B6	F06D	44.70.21
27	-T	INHIBIT 82 CD CZ	02B6	F07H	44.70.21
28	-T	STORE I-E CHANGE	02B6	F12N	44.70.31
29		WRITE PULSE AND DATA ON INHIBIT DRIVE LINES	01A1		42.58.11

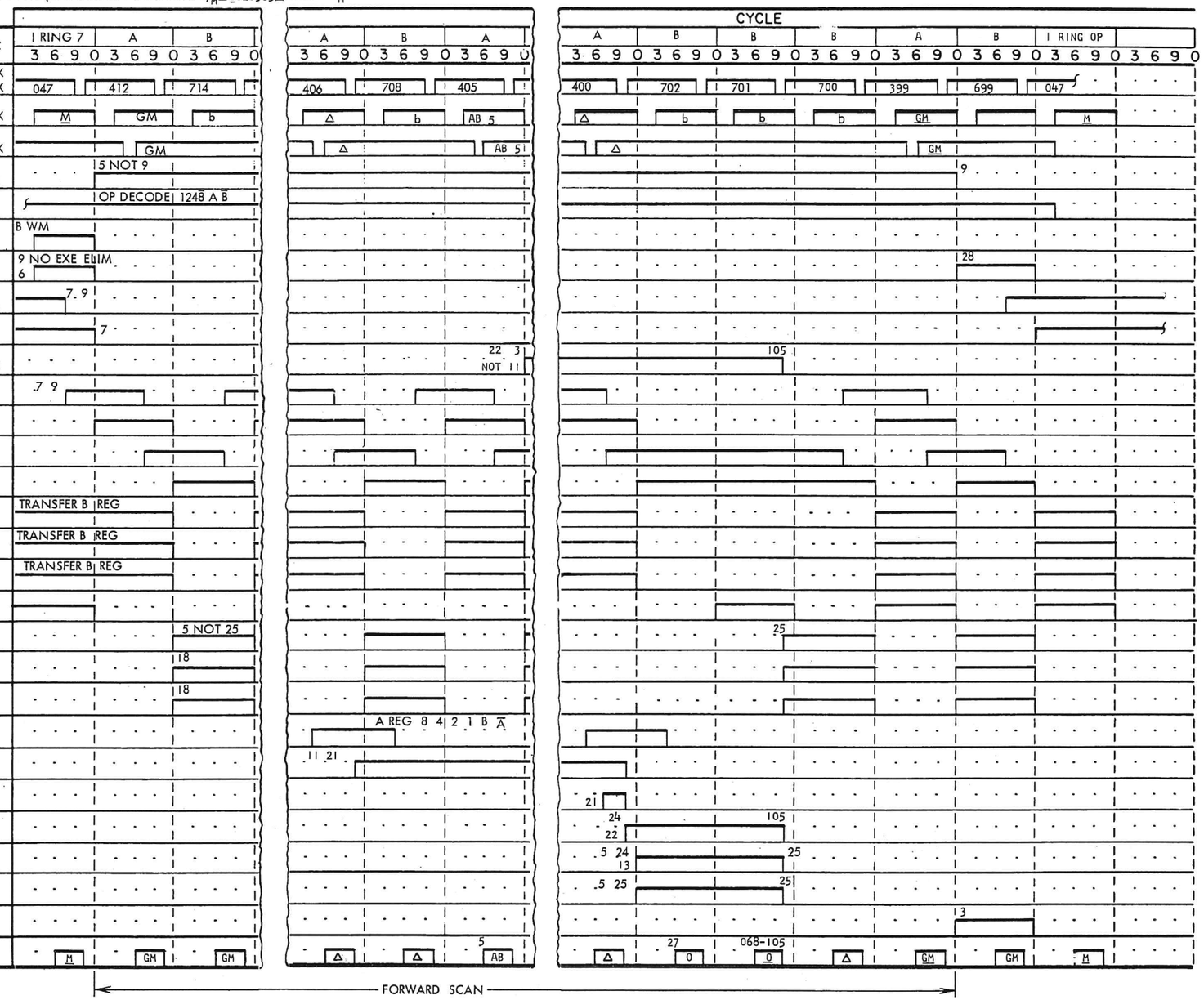


FIGURE 49. MOVE WITH ZERO INSERTION X (AAA) (BBB)

(807) # (898) (257)
(814) X

ORIG A-FIELD
ORIG B-FIELD

N 2X
N ~~2X~~ = (6527)
H T W = (7836 + A-TAG)

RESULTANT B-FIELD LWC = (14363 + A-TAG)

CYCLE: 14 OR 7 | A | B | A | B | A | B | B/1 OP * | B | 1 OP

		SIGNAL NAME	FRAME GATE	TEST POINT	LOGIC
1		STORAGE ADDRESS REGISTER	—	—	32.3X.XX.2
2		B-REGISTER	—	—	35.1X.XX.2
3		A-REGISTER	—	—	35.1X.XX.2
4	+U	MODIFY (#) OP	01B1	B26H	44.62.02.2
5	-T	DELTA 1 CYCLE LATCH	01B2	C11N	31.21.11.2
6	-T	1 CYCLE LATCH	01B2	E19N	31.24.11.2
7	-T	DELTA A CYCLE LATCH	01B2	E09N	31.22.11.2
8	-T	A CYCLE LATCH	06B4	F02P	42.65.01.2
9	-T	DELTA B CYCLE LATCH	06B4	F02N	42.65.01.2
10	-T	B CYCLE LATCH	01B2	E23H	31.26.11.2
11	+U	CYCLE TR 1	06B4	F05E	42.65.01.2
12	+U	CYCLE TR 2	06B4	F06E	42.65.01.2
13	+U	CYCLE TR 3	06B4	F07E	42.65.01.2
14	+U	A CYCLE ELIMINATE	06B4	F22P	42.65.01.2
15	+U	TRANSFER B-REGISTER	06B4	F22A	42.65.02.2
16	-T	ARITH ZONE	05B4	F09H	42.65.02.2
17	-T	ARITH DIGIT	06B4	E07P	42.65.02.2
18	-T	MOD OP BLOCK NU CARRY	06B4	F09N	42.65.02.2
19	-T	B-REG ZONE INHIBIT	06B4	F10H	42.65.02.2
20	+U	RESET A-REGISTER	06B4	F15A	42.65.02.2
21	+U	A-REG SET A (FOR CARRY)	06B4	F15H	42.65.02.2
22	-T	ADDER CARRY	06B4	E01E	42.65.03.2
23	-T	ZONE ADDER CARRY	06B4	F14A	42.65.03.2
24	+U	ADDRESS MOD I-E CHANGE	06B4	F18N	42.65.02.2
25	+U	MODIFIER CONTROL -1	01A8	B04H	32.42.11.2
26	-T	MODIFIER CONTROL +3	06B4	F13H	42.65.02.2
27	-T	MODIFIER CONTROL XFER	01A8	C10A	32.42.41.2
28		MODIFIER OUTPUT ON BUS	—	—	32.43.XX.2
29		DATA ON INHIBIT DRIVE	—	—	35.1X.XX.2

N 2 X
+ H T W
L W C

6 5 2 7
+ 7 8 3 6
14 3 6 3 + A Tag

FIGURE 50. ADDRESS MODIFY TIMING # (AAA) (BBB)

MULTIPLY OPERATION

A-FIELD ADDRESS			457	458
A-FIELD BEFORE OPERATION			3	B6
A-FIELD AFTER OPERATION			3	B6

INSTRUKTIONS: (900) L 783 678
(907) @ 458 678
(914) B 900

B-FIELD ADDRESS			673	674	675	676	677	678
B-FIELD BEFORE OPERATION			2	0	3	3	2	1
B-FIELD AFTER CLEAR OPER.					1	0	0	0
B-FIELD AFTER ADD 2A OPER.					0	0	7	B2
B-FIELD AFTER ADD A OPER.			0	0	0	1	0	B8
B-FIELD AFTER ADD 2A OPER.			0	0	7	3	0	B8

	SCOPE POINT	LEVEL	I	A	B	A	B	A	B	B	B	AUX A	AUX B	A	B	B	B	AUX A	AUX B	A	B	B	B	AUX B	B	AUX B	B	AUX A	AUX B	A	B	B	B	I
M-STAR			914	458	678	458	678	457	677	676	675	458	678	457	677	676	675	458	678	457	677	676	675	678	674	677	673	458	676	457	675	674	673	914
A-STAR			458	458		457		456				457		456				457		456								457		456				
B-STAR			678		678		677		676	675	674		677		676	675	674		677		676	675	674		673		672		675		674	673	672	
A-AUX-STAR				458								458						458																
B-AUX-STAR					678							458	678					458	678					677		676			676					
B-REGISTER			2	B6	1	B6	0	3	2	3	3	B6	0	3	0	0	1	BB	B2	3	7	0	0	B8	0	0	2	B6	1	3	0	0	0	B
A-REGISTER			8	B6		B6		3		C	C	B6		3		C	C	B6		3		C	C	C	C	C	C	B6		3		C	C	0
TO INHIBIT			2	B6	0	B6	0	3	0	0	1	B6	B2	3	7	0	0	B6	B8	3	0	1	0	B8	0	0	0	B6	3	3	7	0	0	B
B-CYCLE	44.14.01. 02B 7B16 C	T																																
B-AUX STAR R1 UNITS	44.16.11. 02A 7C09 H																																	
AUX STAR SET LATCH	44.11.01 02B 7B17 N	T																																
B-AUX STAR GATE OUT	44.16.01 02A 7C10 B	T																																
TRANSFER B-REG.	35.40.11. 01A 3B01 H	U																																
CLEAR B-FIELD LATCH	44.11.41 02B 7D21 G	T																																
FORCE B2C	44.11.41 02B 7A16 N	T																																
SIGN TRIGGER	44.11.31 02B 7A05 P	T																																
SET. PROD. SIGN LATCH	44.11.41 02B 7B11 H	T																																
X-POSITION LATCH	44.11.21 02B 7C17 B	T							020			000																						
MULTIPLIER LATCH	44.11.21 02B 7C17 H	T															015	000																
A-CYCLE ELEMINATE LATCH	44.11.11. 02B 7C17 A	T							060		045																							
2A LATCH	44.12.11. 02B 7A20 H	T									30						015																	
A LATCH	44.12.11. 02B 7A20 N	T															030						015											
A-AUX LATCH	44.14.11. 02B 7B07 H	U																																
B-AUX LATCH	44.14.31. 02B 7B06 H	U																																
ARITH. DIGIT GATE	44.13.21. 02B 7C09 A	T																																
COMPLEMENT FROM CALC	44.13.11. 02B 7C07 A	U																																
DOUBLER CARRY TRIG.	44.18.21 02A 7C22 A	U			105																													
ADDER CARRY	34.33.11. 01B 3C24 C	T																																
CARRY TRIGGER	34.38.11 01B 3E16 N	T																																
A REG NOT 1 FROM CALC		T																																
A REG Q0 CALC		U																																
A REG Q2 CALC		U																																
I/E CHANGE	44.13.01. 02B 7A24 N	T																																
			I	A	B	A	B	A	B	B	B	AUX A	AUX B	A	B	B	B	AUX A	AUX B	A	B	B	B	AUX B	B	AUX B	B	AUX A	AUX B	A	B	B	B	I

SET | TEST UNITS | TEST UNITS | TEST UNITS | SHIFT | TEST TENS | SHIFT | TEST HUNDS | TEST HUNDS | E/T

A-FIELD BEFORE OPERATION			2	1				
A-FIELD AFTER OPERATION			2	7^B				

INSTRUCTIONS: (900) $\underline{0}^{+}$ T83 678
(907) % 458 676
(914) $\underline{B}$ 900

B-FIELD BEFORE OPERATION			0	0		3	4	0
B-F. AFTER DIVIDE - COMPARE			0	1	0	3	4	0^B
B-F. AFTER DIVIDE - COMPARE			0	1	0	3	4	0^B
B-F. AFTER SUBT. A & DIV. COMP.			0	1	0	0	7	0^B
B-F. AFTER DIVIDE - COMPARE			0	1	2^{AB}	0	7	0^B
B-F. AFTER SUBT. 2A & DIV. COMP.			0	1	2^{AB}	0	1	6^B

4 A Aux
6 B Aux

SCOPE TRIGGER POINT	02 B7 B17 N AUX STAR SET LATCH	I_7	A	B	A	B	A	B	B	B	AUX B	AUX A	AUX B	A	B	B	B	AUX A	AUX B	A	B	B	B	AUX B	AUX A	AUX B	A	B	B	B	AUX A	AUX B	A	B	B	B	I_{op}
M - STAR		914	458	676	458	676	457	675	674	673	676	458	677	457	676	675	674	458	677	457	676	675	674	677	458	678	457	677	676	675	458	678	457	677	676	675	914
A - STAR		458	458		457		456					457		456				457		456					457		456				457		456				
B - STAR		676		676		675		674	673	672	677		676		675	674	673		676		675	674	673	678		677		676	675	674		677		676	675	674	
A - AUX - STAR			458																																	
B - AUX - STAR				676							677													678													
B - REGISTER		2	7^B	3	7^B	3	2	0	0	0	3	7^B	4	2	3	0	0	7^B	4	2	3	0	1	7	7^B	0^B	2	7	0	0	7^B	0^B	2	7	0	2^{AB}	B
A - REGISTER		8	7^B	7^B	7^B	[illegible]	2	2	C	C	C	7^B		2		C	C	7^B		2		C	C	C	7^B		2		C	C	7^B		2		C	C	0
TO INHIBIT		2	7^B	3	7^B	3	2	0	0	0	3	7^B	4	2	3	0	1	7^B	7	2	0	0	1	7	7^B	0^B	2	7	0	2^{AB}	7^B	0^B	2	1	0	2^{AB}	B
B - CYCLE	44.11.01 02 B 7 B16C																																			
B-AUX STAR RE. UNITS	44.16.01 02 A 7 C09 H																																			
AUX STAR SET LATCH	44.11.01. 02 B7 B17 N																																			
B-AUX-STAR GATE OUT	44.16.01 02 A 7 C10 B																																			
TRANSFER B-REG	35.40.11. 01 A 3 B 01 H																																			
SET A-REG C-BIT	44.11.11. 02 B 7 D03 A															030 - 049																				
X POS. LATCH	44.11.21. 02 B 7 C17 B								030																											
A ÷ ELIM. LATCH	44.11.11. 02 B 7 C17 A							060							060		045																			
SIGN TRIGGER	44.11.31. 02 B 7 A05 P		060																							060										
SET SIGN GATE	44.13.01 02 B 7 D08 D																																			
QUOT. TRIGGER	44.12.01 02 B 7 A13 N																																			
COMPARE GATE	44.13.01 02 B 7 A22 N																																			
A LATCH	44.12.11 02 B 7 C08 P																045						015													
2A LATCH	44.12.11. 02 B 7 C08 A																													045						15
B<A LATCH	44.19.21. 02 A 7 E12 N																																			
B< 2A. LATCH	44.19.31. 02 A 7 E15 N														07																					
COMPLEMENT GATE	44.18.11. 02 B 7 B03 N																																			
SUBT. A LATCH	44.18.21. 02 A 7 E12 H														07				07																	
SUBT. 2 A LATCH	44.18.31. 02 A 7 E15 H													07																						
END DIVIDE LATCH	44.12.01. 02 B 7 B11 F																																			
FORCE B 0	44.18.31 02 A 7 D03 H																																			
FORCE B 1	44.18.21. 02 A 7 C24 D																																			
FORCE Q 0	44.18.31 02 A 7 D03 N																																			
FORCE Q 2	44.18.21 02 A 7 D10 P																																			
MOD. CONTR. +1	32.44.11. 01 A E F 20 N																																			
CARRY	34.38.11. 01 B 3 E 16 N																																			
		I_7	A	B	A	B	A	B	B	B	AUX B	AUX A	AUX B	A	B	B	B	AUX A	AUX B	A	B	B	B	AUX B	AUX A	AUX B	A	B	B	B	AUX A	AUX B	A	B	B	B	I_{op}
			SET AUX-STARS	COMP. OPERATION						SET QUOT. DIGIT	SHIFT D'END FIELD	COMP. OPERATION				SET QUOT. DIGIT	SUBT. + COMP. OPER.				SET QUOT. DIGIT	SHIFT D'END FIELD	COMP. OPERATION				SET QUOT. DIGIT	SUBT. + COMP. OPER.				SET QUOT. DIGIT		

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Console Indicators
37, 20, 11

1401 INTERMEDIATE LEVEL DIAGRAMS

1-4	CLOCKING AND STORAGE
10-22	DATA FLOW AND CONTROLS
25-34	ARITHMETIC OPERATIONS (ADD, SUBT, MULT, DIV)
35-40	MOVE AND LOAD (MOVE, LOAD, CLEAR, EDIT, COMPARE)
41-44	ADVANCE PROGRAMMING (Q OPR, STORE)
45-52	LOGIC OPERATIONS (BRANCH, NO OP, STOP)
53-58	1406 EXPANDED STORAGE
60-79	INPUT/OUTPUT (READ, PRINT, PUNCH AND OPTIONS)
80-89	MAGNETIC TAPE

CLOCKING AND STORAGE

1 CLOCK CONTROL AND CLOCK PULSES
2 STORAGE DECODE SWITCHES
3 CURRENT SWITCHES, INHIBIT DRIVERS
4 PRESENSE AND SENSE AMPLIFIERS

DATA FLOW AND CONTROLS

10 DATA FLOW A, B Reg
11 DATA FLOW CONTROLS
12 INHIBIT CHECK AND A AND B CHECK
13 CYCLE CONTROL
14 ADDRESS STOP, I RING, PROG SKIP
15 OP REGISTER, OP CODE DEVELOPMENT
16 OP CODE AND OP CHECK
17 A STAR AND B STAR
18 I STAR, AUTO SCAN, STAR MANUAL SET
19 STAR MODIFIER AND CONTROLS
20 MODIFIER
21 MODIFIER AND ADDRESS VALIDITY CHECK

ARITHMETIC OPERATIONS

25 ADD SUBT AND ADDER CONTROL
26 ADD SUBT AND ADDER CONTROLS
27 A AUX STAR AND GATE CONTROLS
28 B AUX STAR AND GATE CONTROLS
29 MULTIPLY AND DIVIDE CONTROLS
30 MULTIPLY AND DIVIDE CONTROLS
31 MULTIPLY AND DIVIDE CONTROLS
32 MULTIPLY AND DIVIDE CONTROLS

MOVE AND LOAD

35 MOVE, LOAD, CLEAR, AND COMPARE
36 COMPARE
37 HI LO EQUAL COMPARE
38 ZONE TEST AND WORD MARK SET
39 EDIT AND EXPANDED EDIT
40 EXPANDED EDIT ASTERISK AND DECIMAL OPTION

ADVANCE PROGRAMMING

41 ADVANCE PROGRAMMING Q OPR, STORE LOGIC OPERATIONS
42 ADVANCE PROGRAMMING CONTROLS

LOGIC OPERATIONS

45 BRANCH, NO OP AND STOP OPR
50 RAMAC AND INQUIRY
51 RAMAC AND INQUIRY
52 51 COLUMN FEED

1406 EXPANDED STORAGE

53 MODIFY OP AND STORAGE CONTROL PULSES
54 STORAGE DECODE SWITCHES 4 TO 12K
55 CORE STORAGE DRIVE CKTS AND SENSE CKTS 4 TO 12K
56 STORAGE DECODE SWITCHES 12 TO 16K
57 CORE STORAGE DRIVE CKTS AND SENSE CKTS 12 TO 16K
58 FULL STORAGE PRINT OUT

INPUT/OUTPUT

60 DATA FLOW AND READ CONTROLS
61 PUNCH DATA FLOW
62 PUNCH CONTROLS AND PFR OPTION
63 READER AND PUNCH CHECK CIRCUITS
64 PFR DATA FLOW, CHECKING AND CONTROLS
65 PFR PUNCH CONTROLS
66 PFR READ PUNCH CONTROLS
67 COLUMN BINARY READ CONTROLS AND DATA FLOW
68 MOVE COLUMN BINARY CONTROLS
69 PRINT DATA FLOW
70 PRINT COUNTERS
71 PRINT RINGS
72 PRINT CONTROLS
73 PRINT BUFFER STORAGE AND DATA FLOW
74 PRINT BUFFER RINGS AND CONTROLS
75 PRINT BUFFER COUNTER
76 PRINT BUFFER CONTROLS
77 PRINT BUFFER CONTROLS
78 CARRIAGE CONTROLS
79 DUAL SPEED CARRIAGE CONTROLS

MAGNETIC TAPE

80 READ AND WRITE TAPE
81 READ AND WRITE TAPE WITH WORD MARKS
82 TAPE CONTROL CODES
83 TAPE BRANCH CODES
84 READ COMPRESSED TAPE
85 MANUAL TAPE OPERATION, RESET AND LOAD
86 EXPANDED TAPE
87 I/O BRANCH
88 I/O SELECT

Consoles Indicators
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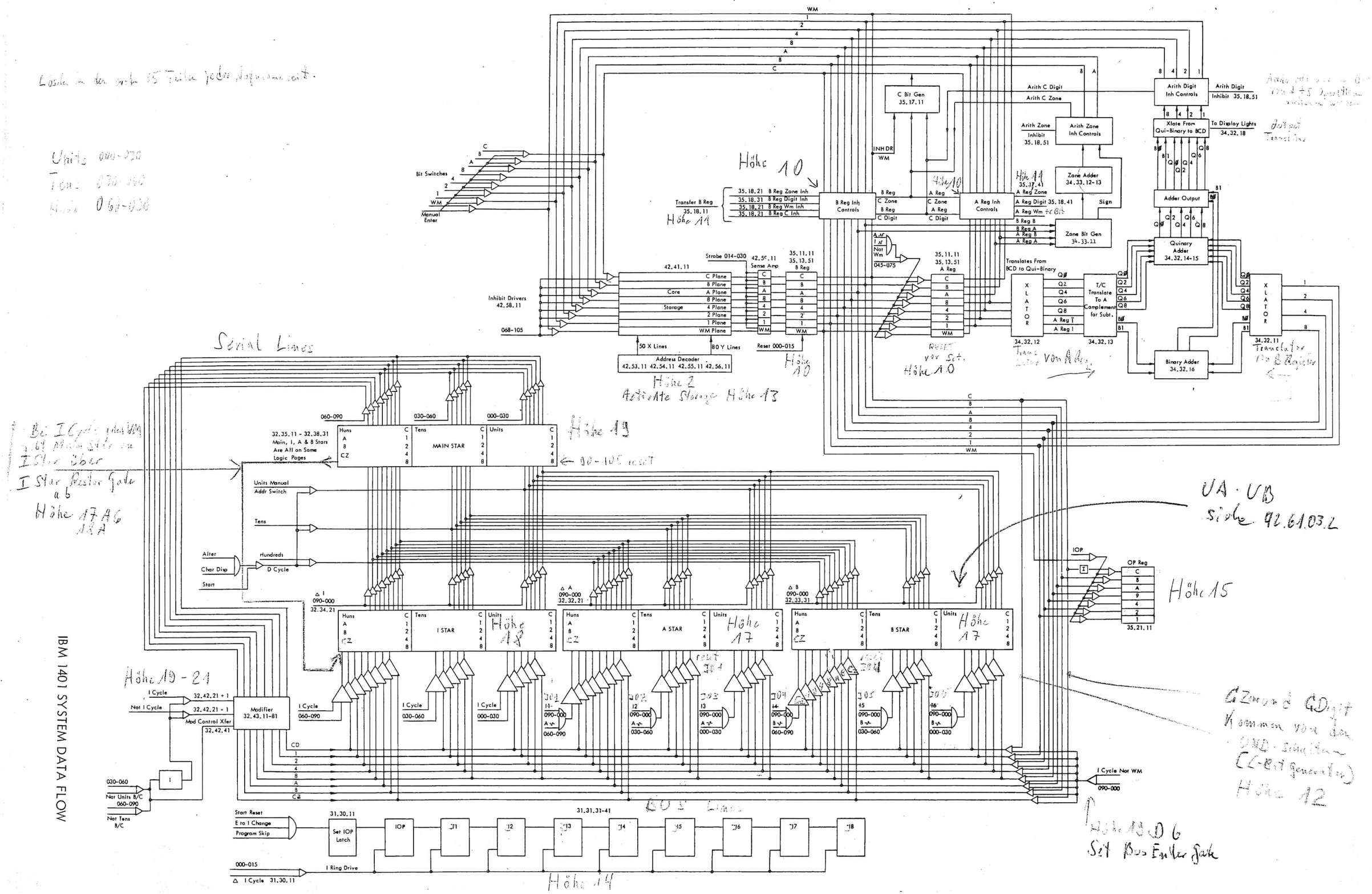

IBM 1401 SYSTEM DATA FLOW