U.D.C. 621.382.333

Transistor Abnormalities as Revealed by Current-Voltage Characteristics

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Summary: The examination of a suspect transistor to determine its mode of degradation or failure always includes, at an early stage, checks on its junction and transistor characteristics, usually with the aid of a visual display on a curve tracer. This paper discusses the diagnostic significance of some of the abnormalities which may be observed on such displays.

1. Introduction

The object of this paper is to collect together a number of published explanations of abnormal current-voltage characteristics of transistors as a guide to the interpretation of results obtained from degraded specimens submitted for failure analysis.

The detailed physical causes of the problems will be discussed only very briefly since they have been treated in numerous publications and conferences over the past few years[1] and in some cases there is still doubt about the physical and metallurgical processes involved. We are here primarily concerned with the diagnostic information which can be gleaned from a close study of the current-voltage characteristics, as displayed at d.c. or low frequency on a transistor curve tracer. Some of the conclusions are inevitably ambiguous unless supported by other evidence. Indications of what other factors to look for are provided in a diagnostic table (Table 1).

Over a period of some years, the theory of transistor operation has been developed to the stage where the characteristics of an ideal transistor are understood in detail, and the behaviour of some real configurations is also qualitatively accounted for.[2, 3] It must be recognized that some of the effects described in this paper as abnormalities may be inherent in the design of certain transistor types, and thus not necessarily detrimental to performance within the specified ranges. A defective transistor characteristic can therefore only be defined with reference to the normal behaviour of the type.

2. Bulk Junction Effects

The majority of problems arising in the bulk of the junction areas are concerned with the ease of carrier transport through the base region. Whether the transistor is prepared by diffusion or alloying, careful control is necessary to ensure that the two junctions are at exactly the right spacing over the desired area. If the base region is too thick the carrier transport across it is reduced by recombination during the increased transit time, so that h_{FB} and h_{FE} both start to fall off at lower frequencies and the cut-off frequencies are correspondingly reduced.

Since collector-emitter avalanche depends on $M\gamma\alpha_T$ approaching unity (where M is the avalanche multiplication factor, γ the emitter efficiency and α_T the base transport factor), the reduction in α_T produced by a thick base or low carrier lifetime in the emitter-base junction depletion region means that a higher value of M, and hence a higher collector voltage, must be attained for avalanche. When the avalanche has started, the rapid increase of emitter current brings about a corresponding increase of emitter efficiency, so that M no longer needs to be so high. The sustaining voltage is therefore less than the breakdown voltage and a 'snapback' is therefore exhibited by devices with thick bases or high recombination rates in the region of the emitter-base junction.

Obviously, excessive base thickness can result from an abnormally shallow emitter junction and, in planar structures, from an excessively deep collector junction. Apart from inadequate control on the processes of forming the junctions there is the possibility that an undetected impurity abnormality, either extensive or localized, in the starting material can give rise to an incorrect base thickness, or to excessive carrier recombination in the junction region.

An unexpected complication in the planar process was the discovery of the effect variously known as 'emitter dip' or 'push-out'.[4] This is the tendency of the already-formed collector junction to become deeper immediately below the subsequent emitter diffusion. The cause appears to lie in the introduction of lattice defects by the latter diffusion, and the extent of the effect depends on factors such as the actual impurity elements, diffusion temperatures, and cooling rates. The result is to upset the uniformity of thickness of the base region, giving in extreme cases a lateral path from emitter to edge of 'dipped' collector junction which is significantly shorter than the normal path. The effect is more serious in high-frequency transistors with their necessarily thin base layers.

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'Punch-through' (or reach-through) is the phenomenon where the space-charge region of a junction widens under steadily-increasing bias to the point where it meets a discontinuity which can provide additional carriers, such as another junction, a contact, or a boundary with another region of high doping (e.g. that between an n-type epitaxial layer and its n+ substrate). A number of situations can be envisaged for planar transistors, in addition to the simple punch-through between emitter and collector junctions which is liable to take place in any type of transistor. Two significant modes are the linking-up of the collector junction with the epitaxial interface beneath it and the spread of the collector junction space-charge layer at the surface towards the base contact. Punch-through effects due to reverse voltage applied to the emitter junctions of planar transistors are unlikely, in view of the much higher doping levels and the consequently thinner space-charge layer of this junction.

The most common form of punch-through, between collector and emitter, is less likely in diffused transistors, with their fairly high base doping level, than in alloy devices, where the base material is the most pure. Consequently, most planar transistors subjected to collector-emitter voltage attain the avalanche breakdown voltage before the punch-through level is reached.

However, if there is a very small patch of abnormally thin base region, because of some local impurity anomaly, such as a cluster of impurity atoms in the starting material, or a diffusion 'pipe' due to a structural defect, local punch-through can take place. The series resistance of such a small patch may be high enough for the effect on the current-voltage characteristic to be no more than formation of a 'knee' at the local punch-through voltage, followed by a resistive region up to the collector-emitter breakdown voltage of the normal parts of the device.

When we consider the effect of applying collector-base voltage to a transistor (with open emitter) which is liable to punch-through, it can be seen that as soon as the collector junction space-charge region extends beyond the emitter junction into the floating emitter, the latter begins to rise above its normal floating potential and remains at a constant level (the punch-through voltage V_{PT}) with respect to the collector. This results in a reverse bias appearing between emitter and base. When this junction breaks down, a collector-base path is established via the emitter junction and the space-charge region. Thus the effective collector-base breakdown voltage is $V_{(BR)CBO} = V_{PT} + V_{(BR)EBO} = V_{(BR)CEO} + V_{(BR)EBO}$. In these circumstances, short-circuiting emitter to base makes $V_{(BR)CES}$ equal to V_{PT}, which is thus less than $V_{(BR)CBO}$, as contrasted with the normal transistor in which these two breakdown voltages are equal.

The other important bulk mechanism in planar devices is reach-through from the collector junction, through the lightly-doped epitaxial collector layer, to the more heavily-doped substrate, again causing an artificially low breakdown voltage, since the expansion of the space-charge layer with voltage is interrupted and the field increases rapidly. There is a corresponding abrupt change in the rate of increase of collector-junction capacitance.

The avalanche process is accompanied by the emission of light from the immediate regions where the generation-recombination processes occur. Observations of the uniformity of this radiation give an effective guide to the distribution of the avalanching regions. The light is emitted from silicon devices in the visible and near infra-red ranges, and can be viewed with an ordinary microscope in a darkroom, or more easily with an image convertor which accepts the infra-red radiation as well. The intensities are such that photography may require several minutes' exposure. Absorption and scattering of the light within the semiconductor result in the deeper parts of the junctions being less amenable to observation than edges and shallow regions, so that emitter junctions of planar silicon transistors are the most rewarding for study by this technique.

3. Surface Effects

Punch-through from the collector junction to the base contact can occur in planar transistors with lightly-doped bases or with base contacts too close to the collector junction (either the true metallurgical junction or the effective position as modified by surface effects to be described below). The result is to reduce the peak collector-base voltage below the theoretical avalanche breakdown voltage.

Since both junctions in a transistor necessarily come to the surface, their uniformity is liable to be affected in this region by the presence of surface impurities, passivating layers, and often by the geometrical configuration. The field across the junctions gives rise to fringing effects at the edges, which can result in migration of ionized impurities on the surface of the semiconductor or thin passivating layer, and also within the latter layers if any mobile ions exist. Grown junctions which are cut from uniform slices of expitaxial material, and mesa devices with vertical edges, have no geometrical factors, but planar devices are characterized by the cylindrical nature of their junction edges, coupled with the fact that the edges of the second and subsequent diffusions reach the surface through a region of rapidly changing impurity content. Built-in surface effects also appear in mesa-type devices with edges oblique to the junctions, this being a design feature of many thyristors and similar devices.

3.1. *Accumulation, Depletion and Inversion layers*

The most important surface factor affecting an active semiconductor device is the departure of the surface conductivity from the bulk value (or the extrapolated value, in the case of a device with graded impurity content). Even a clean, undamaged slab of semiconductor has surface states which cause the band structure to be distorted close to the surface: any charges due to surface impurities will induce equal and opposite charges within the semiconductor and accentuate the effect. We can define three states of the surface:

(a) Accumulated—the surface is unchanged from the bulk conductivity type but behaves as if more heavily doped.

(b) Depleted—the surface is nearer intrinsic conductivity than the bulk, or completely intrinsic.

(c) Inverted—the surface is of opposite conductivity type to the bulk.

The configuration and thickness of most p-n junction space-charge regions will be modified by one of these effects at the surface, altering both junction breakdown voltage and internal leakage current. External leakage currents through the charged layers are a separate problem which may or may not arise.

The possible changes can be illustrated by exploring the results of applying increasing p- or n-type character to the surface of a p^+-n junction (Fig. 1). In the idealized situation of this figure, the breakdown voltage is determined mainly by the extent of the space-charge layer on the high resistivity n side of the junction, and the leakage current consists of a diffusion component, controlled by carriers from beyond the space-charge region, and a recombination component, involving carriers generated and recombining within the space-charge region. Both the absolute and relative magnitudes of these components alter with the volume of the space charge.

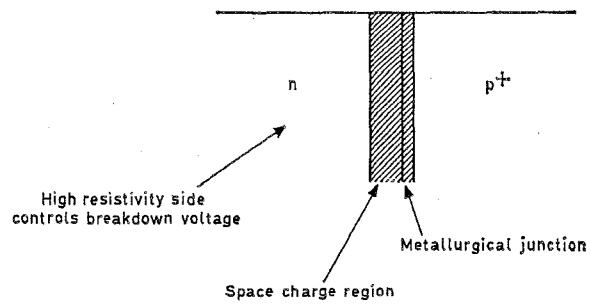
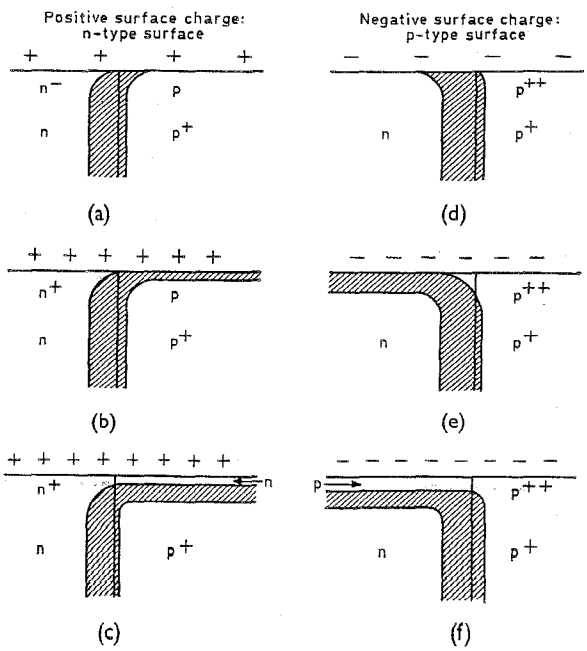


Fig. 1. p^+-n junction with no surface abnormalities.

In simple structures with no impurity gradation, the former component is independent of the width of the space-charge layer, while the latter component is directly proportional to the width, so their ratio is readily calculated. However, when bulk impurities are graded, and surface space-charges are also involved, both the absolute and relative magnitudes of these components alter with the volume of the space-charge.

Figure 2 shows, in the left-hand column, the effect of an increasing positive surface charge inducing an n-type tendency in the surface. This has initially more effect on the lightly-doped n-side than on the p^+ side,



(a) Space-charge layer narrowed at surface. Breakdown voltage reduced.

(b) Surface recombination component in space charge layer added to junction leakage current.

(c) Permanent channel across p^+ region, increasing effective junction area, but now only involving bulk recombination. Channel breakdown may occur at low voltage.

(d) Space-charge layer widened at surface. Breakdown voltage increased if previously controlled by surface.

(e) Space-charge layer narrowed at surface, reducing breakdown voltage. Leakage current increased by surface recombination.

(f) Permanent channel across n^+ region, increasing effective junction area, but now only involving bulk recombination. Channel breakdown may occur at low voltage.

Fig. 2. Effect of increasing surface charge on p^+-n junction (charge increasing from top to bottom).

so that the space-charge region is narrowed and breakdown voltage reduced. As the p^+ surface depletes, it links up with the junction depletion (space-charge) layer, increasing the latter's area and volume, giving rise to increased leakage currents, especially since the (often high) surface recombination is now added to the bulk recombination. Further increase in charge converts the p^+ surface completely to an n-type inversion layer or surface channel, so that there is now a field-induced junction, no longer following the original 'metallurgical' junction close to the surface. The depletion region of this field-induced junction no longer contains the surface, with its recombination centres, so the recombination component of leakage current drops to the level determined by bulk recombination alone.[5]

The right-hand column gives the corresponding diagrams for a p-type surface swing. Here, in the early stages, the depletion layer is thickened at the surface, so that if the original junction voltage has previously been surface-limited, it will increase towards the true bulk level, until depletion of the n-type surface alters the geometry and thins the depletion region at the 'corner', again reducing the breakdown voltage. The depletion depth below the surface is greater, for a given surface charge, because of the lower doping level of the n-type side.

The increased volume and area of depletion does not, in fact, fully account for experimental observations of leakage current or channelled p-n junctions. Fitzgerald and Grove[6] performed some calculations with reasonable surface recombination velocities for silicon planar device surfaces and found that this simple view often gave leakage currents orders of magnitude less than those actually observed. Two suggestions were put forward to explain the discrepancy, with experimental evidence in support of both. First was that larger channel currents are generated when the inversion layers extend to regions of abnormally high recombination rate—e.g. scribe lines, dielectric defects or even device edges. Secondly, if the field-induced junction defining a channel has a much lower breakdown voltage than the bulk junction (e.g. if it lies in a heavily-doped surface region), its contribution to the total junction current will appear at low voltages but will thereafter be limited by current saturation in the channel.

Two mechanisms which can produce a current-saturating form of characteristic have been recognized.[7] If the surface mobility is high, and the recombination-generation centre is small, carriers will be swept out as soon as they are generated, and further increase in bias will have no effect. Alternatively, if the centre is large and gives a substantial current flow along the thin channel, an appreciable voltage drop will appear along its length. There will thus be a point where the field induced junction has zero bias, and this will move away from the parent junction with increasing bias. At some stage, the depletion region of the field induced junction will reach the silicon surface and 'pinch off' the channel, after which no further increase in current or channel length with voltage occurs.[8]

The two mechanisms are distinguished by their temperature sensitivity—the carrier exhaustion process has a high coefficient, since it depends on the carrier generation rate, while the pinch-off mechanism is controlled by the low sensitivity of channel conductance. The former, being dominated by the generation centre, is also less sensitive to surface changes.

An important diagnostic feature for channels connected to junctions is the slope of the forward current-voltage characteristic at low voltages. The forward current of a good junction is given by the sum of two components, diffusion and recombination, with exponential dependences on qV/kT and $qV/2kT$ respectively. Channels appear to introduce a third component with a dependence between $qV/3kT$ and $qV/4kT$. If the coefficient of this term is large, it dominates the low-voltage forward current, so that a logarithmic current-voltage plot will indicate whether a significant channel exists (Fig. 3).

3.2. *Unpassivated Devices*

The effect of surface impurities on unprotected devices was of considerable importance in early semiconductor studies. The term 'surface impurities' should be extended to include ambient gases, since exposure to different gases and washing treatments can leave the surface in a variety of different states, from strongly p-type to strongly n-type, thus permitting the whole gamut of accumulation, depletion, and inversion effects to occur on any semiconductor surface. Any ionic impurities which become mobile in the

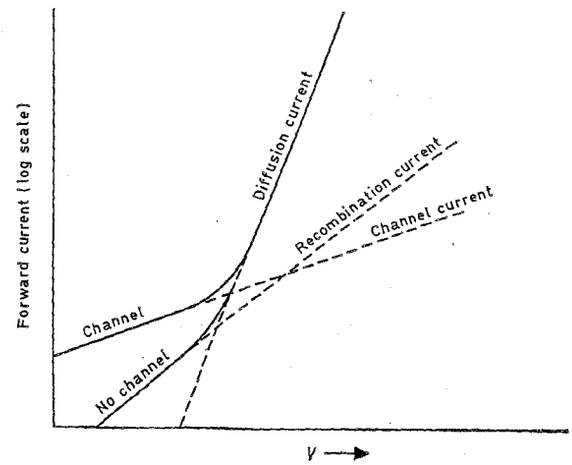


Fig. 3. Forward characteristics of p-n junctions.

presence of moisture or other chemical agents constitute a potential source of leakage currents along the surface of the semiconductor. This was the main reason for the development of passivation treatments for surfaces of transistors, which ultimately showed the way to the planar process.

A further effect of surface condition of a bare semiconductor is the difference in surface recombination velocity produced by various treatments. Since this factor is involved in the equations for current flow near the surface, it can easily dominate the behaviour of unpassivated transistors. A reasonable simplification is to say that strongly p- or n-type surfaces have low recombination velocities, and that a variety of treatments are known to achieve these aims.[9]

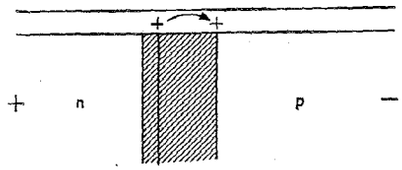
The processes of manufacture often result in the exposure of bare semiconductor at the surfaces of devices which are mainly passivated. This may happen by design—e.g. where the oxide of planar devices is removed along lines which are to be scribed for dice separation—or by accident—e.g. where an oversized contact window or an undersized metal contact leaves a gap. The effects of such exposed areas have not been adequately explored, but some possibilities will be put forward here. It is obvious that surface impurities will often provide recombination centres in their own right, in addition to the effect on lifetime through changes in carrier concentration which may be observed even when an insulating layer separates the impurities from the semiconductor. The important point here is that surface impurities can produce channel effects in both cases, so that, for example, two channels under separate areas of planar oxide can be linked by an area of bare silicon. If, at the same time, the impurities introduce a high surface recombination rate, the situation can be far worse than if no bare semiconductor surface was present.

3.3. *Passivated Devices*

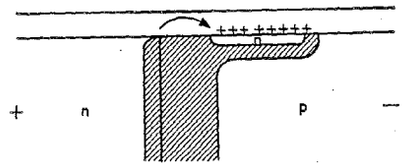
On passivated surfaces, and in particular on the oxide-covered surfaces of planar silicon devices, surface impurities can still produce induced accumulation depletion, and inversion layers, even though they may no longer be able to generate leakage paths across surfaces. The most important mechanism involving surface-mobile impurities is the charge separation which can occur in the fringing field of the junction, acting through the thin dielectric layer.[8] Positive ions accumulate over the negative (p-type) side of a junction and negative ions over the positive (n-type) side under reverse bias. Since each induces a charge of opposite sign in the underlying semiconductor, a tendency towards depletion appears on both sides, to the obvious detriment of junction behaviour. Since one side of the junction is normally more heavily doped than the other, the usual effect is to move towards inversion of the lightly-doped side, and the production of a channel. Channels formed by this mechanism can usually be removed by the simple process of baking the device and thus eliminating the charge separation by randomizing the mobile ions.

A more complicated situation arises when mobile charges exist within the passivating layer. This is a problem which particularly concerns planar devices with thermally-grown oxide, since the normal result of this process is to produce a positive charge in the oxide and consequently an n-type swing on the underlying silicon. The mechanisms by which this can occur have been the subject of extensive debate and experiment, and it seems probable that several different factors contribute to varying degrees, according to the details of the oxidation process. For our purposes, however, it is sufficient to discuss the effects of two factors regardless of their physical origin: fixed charges (including fixed centres whose charge can be varied) and mobile ions. Their behaviour may be quite different according to whether the fields in which they lie are entirely lateral fringing fields or a component normal to the oxide-silicon interface is introduced by the presence of a metal on the top surface of the oxide, such as an expanded contact or an integrated circuit interconnection. If there is a field normal to the interface, charge redistribution takes place at elevated temperatures but not symmetrically with respect to field direction. With metal positive and semiconductor negative, the positive charge builds up close to the latter, producing an n-type tendency. The reverse effect is much harder to achieve. Lateral fields produce charge separation within the oxide, and reversed fields and elevated temperatures are needed to eliminate the resulting channel effects. When channels are formed by lateral migration in connection with strongly reverse-biased junctions, they may become isolated when the space-charge region contracts on removal of the voltage (Fig. 4), and only become reconnected when the voltage is raised to a threshold level.[6, 10] Thus junction leakage currents may be negligible up to this level and then increase by orders of magnitude when the channels start to conduct.

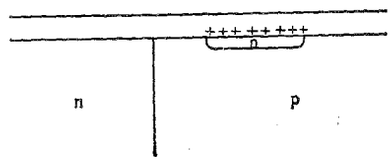
The effects of surfaces on transistor behaviour are best illustrated in terms of the usual n-type tendencies on the surfaces of planar p-n-p and n-p-n transistors, remembering that the collectors are of low, fairly uniform impurity content, and bases have higher, graded content. The effects of emitter depletion and inversion layers are not so obvious because the doping levels are usually such that the normal levels of surface charge in silicon devices are insufficient to produce the full sequence of events shown in Fig. 2. However, when the surface concentration is greater than about 4×10^{18} cm^{-3}, the inversion layer becomes so thin that there is an appreciable probability of tunnelling



(a) Reverse voltage applied.



(b) Channel formed by positive ion migration in oxide to far side of space-charge region.

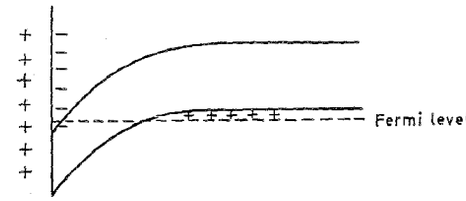


(c) Voltage removed, isolated channel remains.

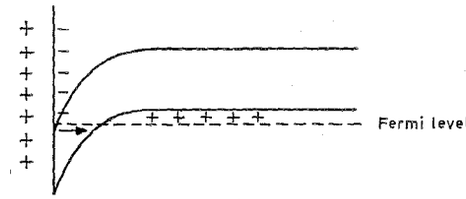
Fig. 4. Formation of an isolated channel by ion migration in the fringing field of a junction.

between valence and conduction bands (or intermediate impurity levels)[11] as shown in Fig. 5. This gives an excess leakage current in what would otherwise behave as a normal one-sided step junction. Although most devices have emitter surface concentrations so high that this effect cannot occur over the majority of the emitter surface (i.e. greater than about 8×10^{18} cm^{-3}), there will always be a region near the junction where the net impurity concentration goes through the critical range for tunnelling, so that there will always be a critical degree of inversion which will produce excess leakage from the emitter side of the junction. The significance of the effect is least in junctions where steep impurity gradients minimize the width of the critical surface region. It should be noted that tunnelling can also occur on the base side of the junction when the appropriate degree of inversion is attained on specimens with heavily-doped bases.

Recalling that the breakdown voltage of a p-n junction depends primarily on the impurity concentration on the lightly-doped side, it is easy to see that with the doping system of the planar transistor, the state of the collector surface normally determines the tendency to surface breakdown of collector junctions and the base surface usually controls emitter junction breakdown. In an n-p-n planar transistor, the n^+



(a) Moderate doping, inversion layer too thick for tunnelling.



(b) Heavy doping, tunnelling across thin inversion layer.

Fig. 5. Surface band structures, illustrating tunnelling on inversion of heavily-doped surfaces.

shift of the collector surface reduces the collector junction breakdown voltage (Fig. 2), while in a p-n-p device, with only a light depletion layer over its collector, the collector breakdown voltage is increased, although heavy depletion or inversion reverses the effect.

The well-known 'walk-out' effect, often seen on curve-tracer displays, in which the breakdown voltage increases rapidly after reverse bias is applied, can usually be attributed to surface impurity or charge changes resulting from the application of the electric field or (less frequently) to rise in surface temperature due to the power input. If the surface is close to the inversion point, the depletion layer configuration of the junction is very susceptible to such changes, so that the diminished breakdown voltage and high leakage current resulting from a thin channel are progressively removed.

In a p-n-p device, base surface accumulation and reduction of the emitter breakdown voltage are produced by swings towards n-type which are insufficient to produce inversion and channelling over the p-type regions. Similarly, n-p-n planar transistors can sometimes have increased emitter breakdown voltages when the p-type surface is depleted. Thus the change of breakdown voltage at the surface of a deteriorating transistor often sets in before any increase in leakage current due to depletion or inversion, and the diagnosis of a leakage current as due to a channel should always be considered in relation to abnormalities in breakdown voltage. Conversely, considerable changes in gain and leakage *without* breakdown voltage changes point to bulk, rather than surface phenomena.

The most common problems of planar devices can now be summarized:

(a) p-n-p devices with collector channels. High collector-base and collector-emitter leakage currents, either saturating or non-saturating and (like collector junction capacitance) greatly increased when the active area of the channel reaches the exposed edge of the device. Collector breakdown voltages are usually reduced, (though in some cases slight depletion can cause an increase) and the gain is lessened by the contribution of the leakage effects to the base current.

(b) n-p-n devices with base channels. These may have channels right across the base (or, in annular geometries, in the oxide-covered parts adjacent to emitter and collector, connected by the metallized base ring), or only on the more lightly-doped collector side of the base. The former can produce either a saturating collector-emitter leakage current, with very thin layers, or an ohmic leakage path, with strong channels, or anything between these extremes. A phenomenon which has been seen at low current levels in some n-p-n planar devices, in which the geometry permits the formation of base channels from emitter to collector without reaching the base contact, has been termed 'ultra-high gain'. Rosenbaum and Loro[12] explained this as due to the base channel functioning at low levels as a field-effect transistor, with the bulk of the base acting as the gate. The collector-base currents are normal, and ln I_c versus V_{BE} has less than the ideal slope of q/kT ($40V^{-1}$), in devices of this sort. h_{FE} falls to normal levels when the collector current is raised well above the channel pinch-off level.

The effect of a base channel on the collector-base characteristic depends on whether the base metallization is in contact with the channel (or acts as a bridge between two channelled regions) or not. In the former configuration, there may once again be anything between a small saturated leakage and an ohmic shunt path across the junction, while in the latter, the effect is similar to that of an external collector-emitter shunt path, namely that the linked collector-emitter junction will breakdown at about $V_{(BR)EBO}$ into either a saturated leakage or an ohmic resistance. In this situation, shorting base to emitter will give $I_{CBS} > I_{CBO} > I_D$ (the base current in the shorted I_{CBS} condition), whereas in an unchannelled device these three currents are nearly equal.[13] Channels on the collector side of the base do not affect the emitter junction, but their effect on collector-base leakages and breakdown voltages results in their influence on I_{CBO} being still considerable. The other likely possibility is inversion of the base surface close to the emitter, where it is *heavily doped*, which may produce tunnelling, giving reduced $V_{(BR)EBO}$ and increased I_{EBO}. Since the latter shunts some of the base input, the result is once again a loss of gain. Reddi[11] has shown, experimentally, that inversion of *lightly uniformly-doped* bases can have the opposite effect, since they acquire field-induced junctions which, because of the lower doping, are highly efficient extensions of the emitter area, despite the greater base thickness under them. Thus, although I_{EBO} is increased, giving a higher I_B, the increased injection gives a more than proportionate effect on collector current. The result is an *increase* in h_{FE}.

(c) p-n-p devices with base accumulation layers. The emitter reverse breakdown voltage is reduced, as described above, so that the detrimental effects of exceeding it (such as drift of h_{FE}) may be initiated by the tests of the sharpness of this breakdown which are sometimes used as screening process for transistors.

(d) n-p-n devices with collector accumulation layers. As already described, collector breakdown voltage is reduced, though except in bad cases the effect will be indistinguishable from other junction edge breakdown phenomena.

(e) p-n-p devices with emitter inversion. Tunnelling can increase I_{EBO}, with consequent reduction of gain, and reduce $V_{(BR)EBO}$ if the surface charge is enough to invert the surface in the critically doped region. Otherwise, the area of inversion is very small, and the excess current, containing no tunnelling component, is likewise small.

In the unlikely event of a p-type surface swing on a planar device, or the more likely event of such a swing on a transistor made in some other way, the above remarks can be applied by reversing the p- and n-type references, and at the same time remembering that transistors other than planar do not necessarily have the same relative impurity levels in their three regions.

The accepted way of limiting the effect of channels is to surround the appropriate side of the junction with an annular guard ring or 'channel-stopper'[8] consisting of a heavily-doped surface layer diffused into the surface at a distance from the junction just beyond the normal extent of the bulk depletion layer at maximum designed reverse voltage. This prevents any inversion of the surface near to the junction. Another expedient, which also helps to avoid stability problems due to migration of ions within the oxide of planar devices, is the 'field relief electrode'. Here a metal layer, connected to an annular guard ring, is extended across the surface of the passivating layer as far as the junction,

thus removing fields in the oxide and ensuring constancy of surface potential.[14] The normal n-type tendency is thus counteracted by expanding the base contacts of n-p-n devices and the collector guard rings of p-n-p devices across the oxide to the collector junction (i.e. the negative contact is expanded in each case).

3.4. *Effects of Moisture and Other Conducting Surface Contaminants*

The presence of condensed moisture often assists in the redistribution of the surface contaminants which cause channels, as well as contributing actual (often ohmic) conducting paths across junctions. Freezing and evaporation cause fairly abrupt changes in the surface leakages due to moisture, so that moisture-induced effects can be distinguished from other leakages by temperature cycling. Leakage currents which are only significant from a little below 0°C to somewhere in the region of 100°C are easily recognizable. I_{CBO} is the parameter most obviously affected by condensed moisture, since it is ideally very small. It is possible for large droplets of moisture to give rise to intermittent high leakage as random shocks move them from point to point. Removal of the transistor can does not necessarily remove moisture-induced leakage instantly and vacuum baking may be required to ensure that all moisture is removed from the surface. Unlike some leakages due to ionic separation, these moisture-induced leakages are not re-established by subsequent operation of the device under dry conditions.

Other conducting surface contaminants may not be removed even by vacuum baking, and must be suspected in cases where ohmic junction leakage current persists.

3.5. *The Effects of External Leakage Currents on Transistor Behaviour*

The inherent bulk leakage currents, which are functions of carrier diffusion and recombination in the junction region, must be distinguished from external leakages whose effects are introduced at the contacts, sufficiently remote from the active regions to have little influence on the inherent leakage currents. Thus we can consider a transistor as a 'black box' with currents I_C, I_B and I_E, measured at the terminals, made up of the internal currents I'_C, I'_B and I'_E through the transistor proper, plus currents through shunting resistors representing possible sources of external leakage, such as surface contamination and header faults (Fig. 6). Calling these resistors R_{CE}, R_{CB} and R_{BE}, we can write the measured currents in terms of the internal currents:

$$I_C = I'_C + V_{CE}/R_{CE} + V_{CB}/R_{CB}$$
$$I_B = I'_B - V_{CB}/R_{CB} + V_{BE}/R_{BE}$$
$$I_E = I'_E + V_{CE}/R_{CE} + V_{BE}/R_{BE}$$

In many practical cases only one or two of these leakages may exist. For example, with collector-emitter leakage alone, the effective small-signal gain $h_{fe} = (\Delta I_C/\Delta I_B)_{V_{CE}=\text{const}}$ is essentially the same as the 'internal' gain in the absence of leakage (Fig. 7(b)), though the parallel shunt path makes measurements of the d.c. gain, $h_{FE} = I_C/I_B$, meaningless, and may pass an intolerable standing current.

Emitter-base leakage (Fig. 7(c)) upsets performance at all levels. At $I_B = 0$, the internal I'_B is negative, so I_{CEO} is reduced, and a certain amount of base drive must be applied to overcome this reverse emitter bias and lift the device above cut-off. Reverse emitter bias also causes the collector breakdown voltage to exceed $V_{(BR)CEO}$, so there is a snap-back to normal levels

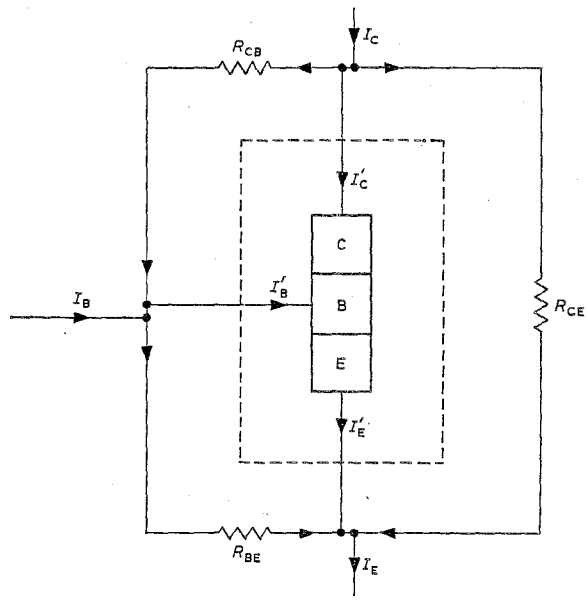


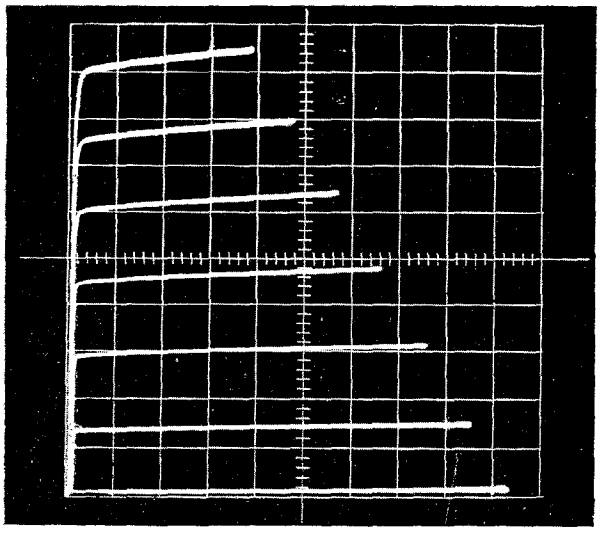
Fig. 6. External leakage paths related to the observed currents in a transistor.

when the bias changes to normal polarity and the collector current rises. Above cut-off the leakage reduces h_{fe} by shunting part of the base current I_B direct to the emitter contact, the effect being most marked when the base input is low, and the incremental forward resistance of the emitter-base junction is high.

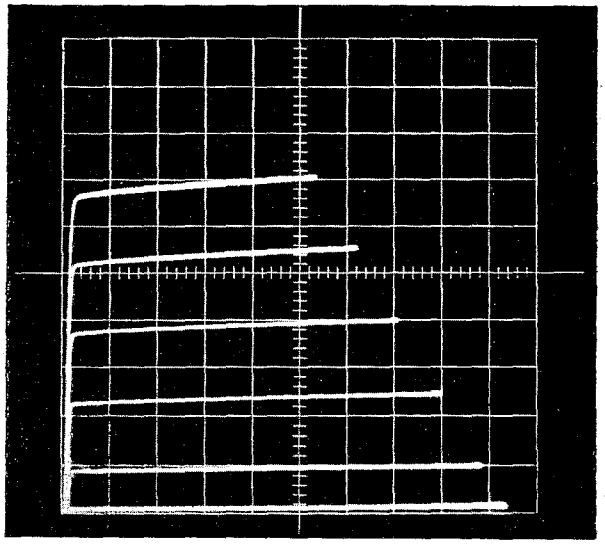
Collector-base leakage means that with no external base current, the transistor still receives an input determined by the collector voltage (Fig. 7(d)). Current gain takes effect and the excess collector-emitter current for a given leakage resistance is much greater than when the same resistance acts as R_{CE}. When an external base-emitter voltage is applied with V_{CE} kept constant there is a corresponding reduction in the collector-base voltage, so the leakage current

contribution to the base input is reduced. As the driving voltage is increased, the leakage provides an ever-decreasing proportion of the base input, so that h_{FE} is not so seriously affected by collector-base leakage at higher input levels. However, the standing current may be intolerable for many applications.

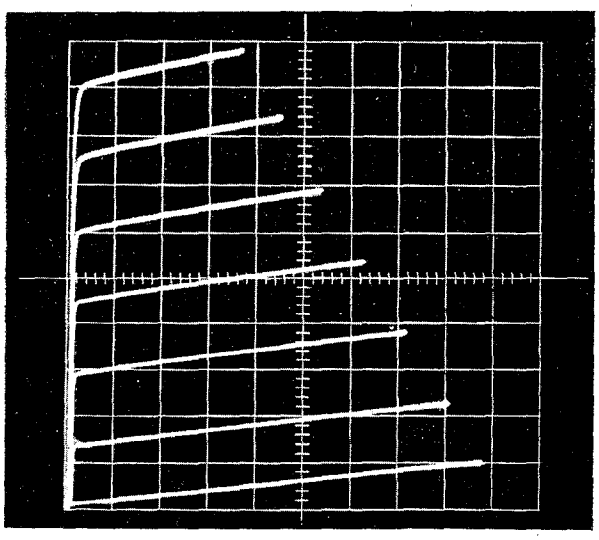
A combination of collector-base and emitter-base leakages of comparable resistance acts as a potential divider (Fig. 7(f)), partially shielding the transistor from the effects of base drive, so that the current gain is reduced and the collector-emitter current at $I_B = 0$ consists of both direct leakage through the resistances



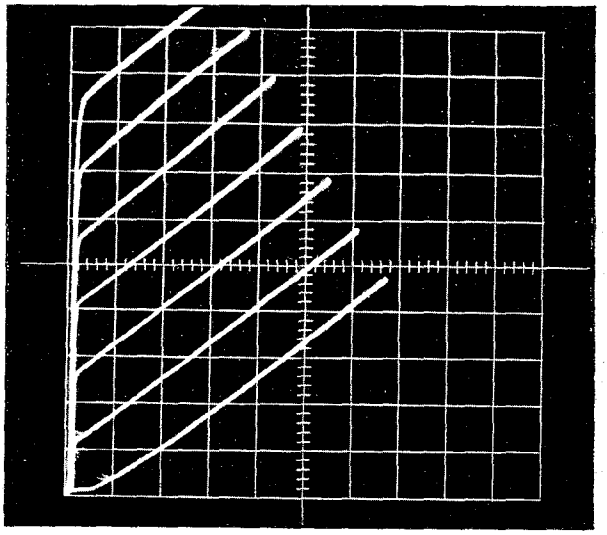
(a) Normal collector characteristics.
horizontal V_{CE} 2 V/div,
vertical I_C 2 mA/div,
base steps I_B 50 μA/step, h_{FE} 54–68



(b) 10 kΩ collector to emitter
h_{FE} 54–68

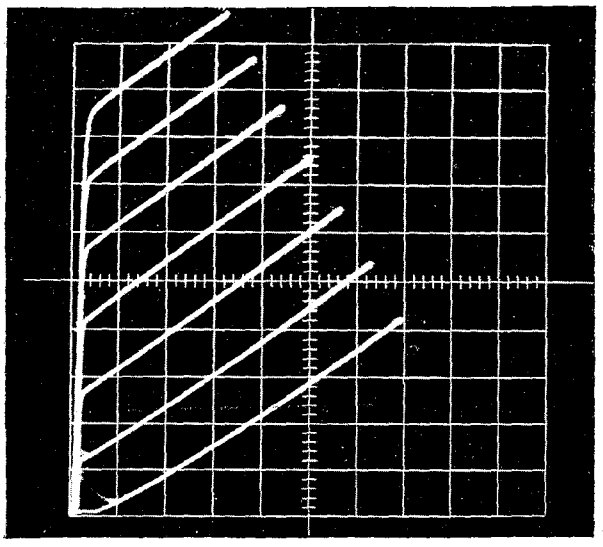


(c) 10 kΩ base to emitter
$I_B = 0$ and $I_B = 50$ μA
steps coincide
h_{FE} 52–64
(except where cut-off at low levels).

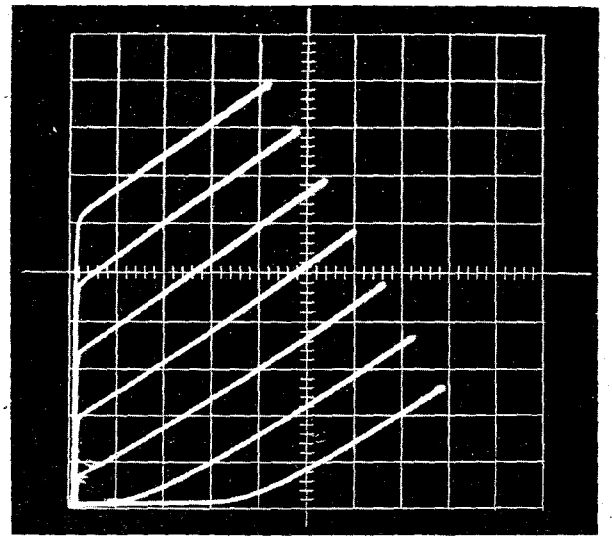


(d) 100 kΩ collector to base
Collector slope 1·4 kΩ
h_{FE} 52–64

Fig. 7. Collector characteristics.



(e) 100 kΩ collector to base
10 kΩ collector to emitter
Collector slope 1·3 kΩ
h_{FE} 52–64



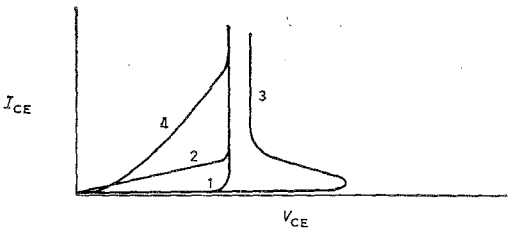
(f) 100 kΩ collector to base
10 kΩ base to emitter
$I_B = 0$ curve 'turns on' at 6 V, where V_{BE} 0·64 V
Collector slope 1·4 kΩ
h_{FE} 52–60

Fig. 7 (*contd.*) Collector characteristics.

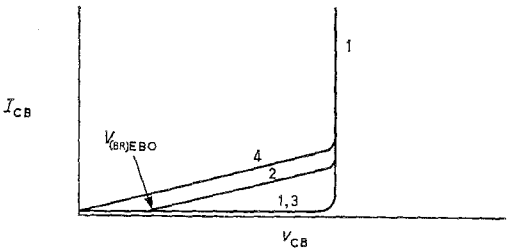
and a larger contribution which comes into play at a threshold V_{CE} where the voltage applied by the potential divider starts to forward-bias the emitter and thereby produces an input which is amplified by the current gain. At higher levels of base input, this excess current sets in at progressively lower collector voltages until the threshold vanishes. Combinations of comparable collector-base and collector-emitter leakage resistances (Fig. 7(e)) are dominated by the former, for reasons already explained.

These remarks on the form of the characteristics can be taken to apply also to those internal (i.e. channel) leakages which act over a wide voltage range as if they were independent paths parallel to the junctions themselves. Reservations apply, of course in cases where the internal resistances are comparable with the external ones, and also where the breakdown characteristics of the channels are intimately involved in the low-level current-voltage relationships of the transistor junctions. The lines of current flow in the bulk of the device are then altered by the presence of the leakage paths, to the extent that they can no longer be considered as independent parallel paths.

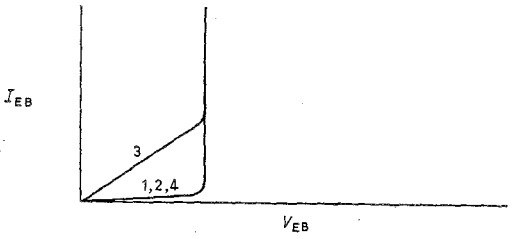
The effects of external leakage paths on breakdown voltages (and also the effects of channels in the rare cases where the channel breakdowns do not complicate the issue) are easily derived (Fig. 8). Collector-emitter leakage does not affect the actual voltage levels significantly, though a subsidiary break-point is seen in the collector-base characteristic at $V_{(BR)EBO}$, beyond which R_{CE} and the emitter junction provide a



(a) Collector-emitter characteristics.



(b) Collector-base characteristics.



(c) Base-emitter characteristics.

Fig. 8. Breakdown characteristics.

Key: 1. Normal
2. With external collector-emitter leakage
3. With external emitter-base leakage
4. With external collector-base leakage.

shunt path. Emitter-base leakage produces its greatest effect on $V_{(BR)CEO}$, by producing a $V_{(BR)CER}$ condition, with snapback. Collector-base leakage, as already explained, produces a large increase in collector-emitter current, so that overheating and softening of the characteristic may occur before the avalanche voltage, which is still determined by the criterion $\gamma\alpha_T M \rightarrow 1$, is attained.

3.6. *Externally-induced Surface Effects*

Two important factors which can affect transistors, especially when operated unencapsulated, in the laboratory, are the effects of illumination and of external capacitances. Illumination increases the generation-recombination rate, and can add to leakage currents, while external means of altering surface potentials can have the same effects as surface charges. An illustration of the latter point was given by Card,[15] who studied the effects of setting up fields between transistors and insulated cans. He showed that with a collector-emitter channel present, +1000V on the can had the same effect on collector leakage current as +0·04V applied to the base, and increased h_{FE}. The converse effect was found with negative voltages. It was concluded that if the can potential affected only the emitter or collector junction characteristic, and not the collector-emitter leakage, a local channel at the relevant junction was indicated. Sensitivity of exposed devices to the presence of nearby objects thus indicates the presence of channels.

Photo-effects may be photo-voltaic or photo-conductive in nature, and while general illumination will somewhat enhance the leakage of a good transistor, the leakage of a channelled device is much more seriously affected, because of the greater area of sensitive surface. Mathews *et al.*,[10] using a scanning light spot, showed how various channel configurations affected local photo-response most where the space-charge region met the surface, and much less where the channel extended deep enough for the space-charge layer not to extend upwards to the surface. Scanning light spots are now widely used for plotting the locations and extent of channels in faulty devices.

4. Thermal Effects

4.1. *Second Breakdown*

Undoubtedly the most important thermal effect in transistors is the 'second breakdown' phenomenon. This has been the subject of extensive study in a number of centres, and although some of the details of the mechanism are still hotly debated, the general pattern of events in the more common designs of transistor is quite well established. An up-to-date review has been given by Schafft.[16]

When a transistor operates under power conditions, it inevitably warms up. It has already been seen that the lines of current flow can become concentrated in certain parts of the device from purely geometrical considerations, and if we allow for additional factors such as junction inhomogeneities, it is readily understandable that some patches of the active region will become hotter than others. Their carrier concentration thus increases, and the current for a given input voltage rises, giving a 'thermal runaway' effect. It has been suggested that the critical temperature for runaway can be equated to that where the highest resistivity semiconductor layer becomes intrinsically conducting, but this would not be easy to prove. Whether or not the runaway immediately destroys the transistor depends mainly on the associated circuit limitations, and on the contact metal used, since the actual mode of failure is usually the alloying-in of the metals at points where the appropriate temperature is reached.[17] Even if the current is restricted, prolonged operation may ultimately result in degradation (especially of h_{FE} and $V_{(BR)CEO}$) to the point of failure. The repetitive voltage sweep of the transistor tester is ideally suited to producing such gradual failures, since the current is externally limited and immediate catastrophe is avoided.

Since it is basically a thermal effect, involving excess carrier generation, second breakdown is a slow phenomenon compared with many of the switching applications of transistors. Delay times in the range from microseconds to milliseconds and transition times of microseconds are typical, so that in switching and class C amplification applications, where the current is turned off in less than these times, second breakdown is less likely to occur than in d.c. circuits and class A amplification, where the heating effects build up rapidly.

A form of second breakdown effect can be observed in some individual p-n junction diodes, but in transistors there is an additional complication of the presence of the base and its input, if any. Not much heating is necessary to produce enough current generation in the base to make the transistor largely independent of any external source. Schafft points out that if the collector current is held constant in the second breakdown region, reverse base drive tends to increase current crowding into the 'pinch' region, thus decreasing V_{CE}, while forward base drive conversely increases V_{CE} (Fig. 9). (This is the opposite effect to that found in thermal runaway involving overheating of the whole active area.) In fact, the current constriction may sometimes be reduced, by increasing the forward base drive, to the extent that the device moves out of second breakdown while maintaining a high collector current.

The shape of a second breakdown transistor characteristic is similar to that of the normal open base characteristic up to a level which may be well

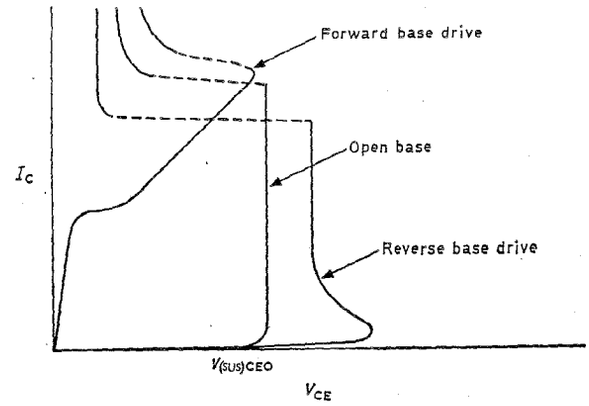


Fig. 9. Effect of base drive on collector-emitter second breakdown characteristics.

into the avalanche breakdown region. At the critical current level (which is not necessarily the same at d.c. or high frequencies as that shown by a low-frequency curve tracer display) a negative resistance region leads sharply to a lower voltage in the stable state of second breakdown, which, according to the transistor design and thermal conditions, may lie between V_{CE} = constant (for good heat sinking) and $V_{CE}I_C$ = constant. To this must be added the effect of any series resistance due to the test gear.

There have been a number of reports of symptoms associated with a tendency to second breakdown. Switchback on the I_{CEO} characteristic is one such feature, while a 'ballooning' of the collector characteristics on the curve tracer with open or forward base bias shows that thermal trouble is imminent. The onset of current crowding causes a distortion of the collector family due to decrease in gain, and it has been noticed that triple-diffused and epitaxial transistors sometimes show a sharp increase in V_{CE} before second breakdown. In the common base configuration, the thermally generated current causes a drop in V_{CB} after an emitter pulse, by partially discharging the collector-base capacitance. Yet another report suggests that reach-through from the collector junction to the collector contact (or substrate in epitaxial devices) induces second breakdown.

All these apparently disconnected features indicate the complexity of the second breakdown and its dependence on details of transistor design. The methods of avoiding second breakdown appear to have much in common with the means of ensuring linearity of current gain, since both involve minimizing natural tendencies to current crowding by maximizing emitter periphery, and minimizing base resistivity and width.

4.2. *Overheating and Thermal Runaway*

The incidence of general, rather than localized, thermal runaway is now rare in silicon transistors, though it can still happen with junctions capable of supporting more than their specified current inputs without breakdown. Obviously, high ambient temperatures or inadequate heat sinking encourage runaway, and in the latter context it must be remembered that the bonding of the transistor to its support is the first link in the thermal resistance chain. If inadequate dice bonding is the cause of thermal runaway, it will introduce other recognizable symptoms, which are described in Section 5 below.

The higher intrinsic carrier concentration of germanium, giving a lower temperature for onset of intrinsic conduction, makes germanium transistors more susceptible to runaway.

5. Mechanical and Header Effects

In this Section we will consider types of misbehaviour which can be attributed to factors outside the semiconductor: the contacts, leads, and header, as well as factors related to mechanical stresses or damage to the transistor chip.

5.1. *Contact Defects*

A high-resistance contact decreases the slope of the forward characteristic of the junction to which it leads, and it often adds a finite resistance beyond avalanche breakdown. In the common-emitter mode, collector resistance, which usually results from a poor die-to-header bond, is recognizable in the abnormal saturation characteristic: $V_{CE(Sat)}$ is high but still linear with respect to current while the corresponding V_{BE} is normal. The effect of base or emitter resistance is also seen in V_{BE} and in the I_{CES} characteristic, which shows something of the 'switchback' normally associated with the I_{CER} mode.

In addition to these obvious resistive effects, substandard bonds to contact areas are liable to produce hot-spots immediately underneath, which can ultimately lead to failure. Young and Elkins[18] have shown that gold ball bonds to planar devices may melt locally, so that gold alloy penetrates the junctions. The onset of this type of fault at the emitter is often marked by a softening of the reverse characteristic of the junction, as well as by excessive noise from the device in operation and a loss of gain due to decreased emitter efficiency.

Faults in the mounting of devices—base contact tabs of alloy transistors, and collector substrate to header bonds of planar devices—introduce thermal resistance as well as the electrical resistance already noted. A device with such problems will suffer from overheating effects, which increase leakage currents and sometimes soften the avalanche characteristics, as well as making second breakdown and thermal runaway more likely to occur.

5.2. *Cracks*

A fault which occasionally results from bonding pressure errors, or may originate from the cutting or cracking stage of separating the semiconductor chips, is a crack across the active region (including of course, any channels which may exist). By introducing a discontinuity in the field distribution, a crack usually reduces the breakdown voltage for the junction in much the same way as the intersection with a surface. Reliable experimental reports of the effects of such faults, uncluttered by associated defects, are rare, but a 2-volt step-back of an otherwise linear collector-base avalanche characteristic has been associated in one report with a crack under the gold ball bond to the base.

The ingress of impurities into cracks, either during processing or subsequently, causes drift of junction leakage currents, as well as noisy instabilities both in the leakage currents and the breakdown characteristics of junctions affected. If the collector-base junction alone is cracked, h_{FE} will hardly be affected, and I_{CES} and floating emitter potential will be normal, so that only the collector-base and collector-emitter characteristics will be upset. On the other hand a crack affecting the emitter junction produces a high floating potential and I_{CES} much greater than I_{CBO}, while the high emitter junction leakage degrades the low current h_{FE}. If both junctions are cracked, the effect is as if a base channel were present in addition to the combined effects on the separate junctions.

5.3. *Header Leakage Currents*

One important external factor which can affect the electrical characteristics is leakage currents across the header, usually attributable to surface contamination or occasionally to insufficient insulation around the leads. If it is on the outside surface some form of washing will usually remove the offending material, but identification of other header leakages are more of a problem. Baking may help, but in the last resort, opening the can and severing the leads inside is the only answer. Leakages of this type can thus be simulated by external resistances on a good transistor, as described above.

6. Diagnosis of Faults from Abnormal Electrical Characteristics

The diagnosis of faults from the current-voltage characteristics of transistors is always a qualitative process: it is usually necessary to look for additional evidence to determine where the fault is located and what it consists of. For example, a short-circuit is readily diagnosed, but its identification as due to an internal effect, a surface effect, or an extraneous metallic object may often be a matter of painstaking study. A further difficulty is that because the measurements which show unusual characteristics may be made under different conditions, some faults may show up much better on some tests than on others. An example of this is emitter junction problems, which may show up in h_{FE} or in I_{EBO} tests, but very often not both, because the former is a forward-bias test and the latter is done at reverse bias, so that the significant part of the junction is not the same in the two cases.

Table 1 approaches the diagnosis problem by taking each abnormality in turn, recording as many interpretations as possible, and then, for each of these, indicating other electrical or other tests which might confirm the verdict. It will be assumed that where not otherwise stated, remarks about 'excessive leakage current' imply 'for a given voltage, as compared with a perfect sample', and so on. The lists can obviously not be exhaustive: circumstances may sometimes give unexpected combinations or cancellations of effects, which can only be interpreted if additional evidence becomes available from visual or other observations.

The interpretations given in this Table must not be applied mechanically to the results given by many automatic testing methods, in which current levels at fixed voltages or, more commonly, voltage levels at fixed currents are recorded. For example, an automatic test for junction breakdown voltage might be to measure the voltage which produces 1mA avalanche current. However, if a shunt path existed, this amount of current might be recorded well below the true breakdown voltage, so that the record would show high leakage *and* low breakdown, where the true verdict should be high leakage alone. Similarly a collector-emitter shunt path will upset the d.c. ratio I_C/I_B used to measure gain at low collector currents, even though the high current and small-signal gains are normal.

A visual display of the characteristics on a curve tracer is essential.

7. Progressive Changes in Properties

The majority of devices presented to a failure analyst have little or no record of previous history attached, so that the levels of leakage currents and breakdown voltages can only be judged by comparison with a device which fulfils the normal specifications. However, it will by now be obvious that, apart from catastrophic failures, a large proportion of detrimental effects are progressive in nature, so that information such as whether the leakage currents are rising or falling can provide valuable aids to the choice between the possible explanations of a spot check result.

The value of continuous monitoring of changes in breakdown voltage which often precede large changes in leakage current has already been noted. The voltage changes often lie within the specified range for good

Table 1
Diagnostic Table

Primary indications	Additional indications	Interpretations and suggestions for further action
	Two-terminal characteristics	
Emitter-base junction		
High I_{EBO} (and low-level gain reduced)	(a) $V_{(BR)EBO}$ normal, ohmic current	External leakage path, or strong channel, base contact to emitter.
	(b) $V_{(BR)EBO}$ low, I_{CBO} normal	Channel on base side of junction (especially n-p-n planar).
	(c) as (b), but little temperature dependence	Emitter inversion, giving tunnelling (especially p-n-p planar).
	(d) with instabilities of current and $V_{(BR)EBO}$	Crack across emitter junction.
Soft breakdown	(a) with high I_{EBO} at lower levels	Device overheated, giving large diffusion current.
	(b) with excessive noise	Hot-spots under defective bond. Examine cross-section.
	(c) with entirely abnormal emitter behaviour (e.g. strong dependence of I_{EBO} on bias)	Emitter abnormalities such as precipitate particles producing microplasmas. Examine cross-section after looking for light emission below breakdown.
Resistive forward characteristic		High-resistance emitter or base contact.
Low slope to logarithmic low-level forward characteristic		Channel on base side of junction (especially n-p-n planar) or tunnelling due to emitter inversion (especially p-n-p planar).
Collector-base junction		
High I_{CBO}, ohmic	(a) temporarily reduced below 0°C or above 100°C. May be unstable and/or noisy	Surface moisture. Puncture can; vacuum bake, and observe permanent disappearance of leakage.
	(b) not removed by baking	External leakage path or strong channel, base contact to collector.
High I_{CBO}, in silicon devices, with normal voltage dependence	(a) I_{EBO} also high when measured immediately after I_{CBO}	Large diffusion current, device may be overheating. Examine low-voltage forward characteristic for high logarithmic slope.
	(b) I_{EBO} unaltered	Saturating channel, collector to base contact; may be removable by baking.
I_{CBO} rises, above a threshold voltage, to a new saturated level		Isolated channel. Observe photocurrent as light spot is scanned across junction: response is obtained from channelled areas. Look for corresponding jump in junction capacitance above the threshold voltage. If surface impurity migration is responsible, channel may be removed by baking.
High I_{CBO}, possibly drifting with time and applied voltage, and/or noisy	(a) h_{FE}, I_{EBO}, and floating emitter potential normal	Crack in collector-base junction, breakdown characteristic may be abnormal and noisy.
	(b) h_{FE} low, I_{EBO} and floating emitter potential high	Crack through both junctions.
Low $V_{(BR)CBO}$	(a) $V_{(BR)CBO} = V_{(BR)CEO} + V_{(BR)EBO}$	Punch-through, collector to emitter (Fig. 10). Check that $V_{(BR)CES} = V_{(BR)CEO}$ (i.e. that relationship is not fortuitous), and look for light emitted from avalanching emitter junction. Examine cross-section for abnormally thin base (though it may be a normal-thickness, high resistivity base).

Primary indications	Additional indications	Interpretations and suggestions for further action
	(b) unrelated to $V_{(BR)CEO}$ and $V_{(BR)EBO}$, in epitaxial devices	Punch-through to epitaxial substrate, due to thin, high resistivity, collector layer. Look for non-linearity of $V_{CE(Sat)}$ at low levels, confirming high resistivity, and change of slope in capacitance-voltage characteristic near $V_{(BR)CBO}$. Examine cross-section.
	(c) possibly 'walking-out'	Accumulation layer on collector surface (especially in n-p-n planar).
	(d) combined with low h_{FE} and high I_{CBO}, possibly walking-out	Collector channel (especially p-n-p planar). If emitter contact is expanded over collector, it may be severed and used as a gate electrode to cancel part of the channel, reducing I_{CBO}.[19]
	(e) sharp break in I_{CBO} curve at $V_{(BR)EBO}$, followed by saturated or ohmic leakage, up to true $V_{(BR)CBO}$	Base channel or other current path collector to emitter (Fig. 10). Check that $I_{CBS} > I_{CBO} > I_D$ (the base current in the 'shorted' I_{CBS} condition). Comparison with emitter-base characteristic measures shunt path resistance.
High $V_{(BR)CBO}$		Depletion layer on collector surface (especially in p-n-p planar).
Soft $V_{(BR)CBO}$, with abnormally high voltage dependence of I_{CBO} at lower levels		Local microplasma breakdown due to defects in the collector junction region. Observe light emission.
Loop on $V_{(BR)CBO}$ characteristic	(a) high leakage currents, possibly unstable	Internal moisture. Check that there is no change in a dry gas ambient, and then observe loss of effect on puncturing can and baking.
	(b) excessive junction capacitance	May be constructional fault, or effect of polarized impurities.
Forward characteristic resistive		High collector or base series resistance.
Low slope to logarithmic low-level forward characteristic		Channel over high resistivity side of junction.
Collector-emitter characteristic		
High I_{CEO}, ohmic Sharp break in I_{CBO} curve at $V_{(BR)EBO}$, followed by a resistive region. h_{fe} normal	(a)	Strong base channel (especially in planar n-p-n).
	(b)	External leakage path.
	(c)	Internal path between collector and emitter due to damage.
High I_{CEO}, ohmic	I_{CBO} also high, with $I_{CEO} = h_{FE} I_{CBO}$	High collector-base leakage (q.v.).
High I_{CEO}, saturating	(a) I_{CBO} and I_{EBO} also high and saturating	Base channel (especially in planar n-p-n).
	(b) I_{CBO} also high and saturating. I_{EBO} normal	Saturating channel, collector to base contact.
	(c) I_{CBO} and I_{EBO} normal, h_{FE} very high at low levels	Collector-emitter channel, not touching base contact, acting as a f.e.t. (especially in planar n-p-n).[12]
Low $V_{(BR)CEO}$	(a) Current limited beyond breakdown, $V_{(BR)CBO} = V_{(BR)CEO} + V_{(BR)EBO}$ and $V_{(BR)CES} = V_{(BR)CEO}$	Punch-through, collector to emitter. Examine cross-section for thin high resistivity base region.
Large snapback beyond breakdown to a characteristic between V_{CE} = const and $I_C V_{CE}$ = const		Second breakdown, due to thermal effects often involving high base resistivity and base width. Check thermal resistance versus input power for instability. Apply forward bias to base junction, with constant collector current, and observe increase in V_{CE}.

Primary indications	Additional indications	Interpretations and suggestions for further action
$V_{(BR)CEO}$ high, with snapback to a normal sustaining voltage	(a) I_{EBO} high, h_{FE} low	Base-emitter leakage (q.v.).
	(b) low f_T, h_{FB}, and h_{FE}. I_{EBO} normal	Wide base region limiting the contribution of emitter injection to the avalanche at the collector junction. Examine cross-section.
Linear forward characteristic		High series resistance in emitter or collector.
Two-terminal characteristics with third electrode connected		
Collector-emitter, with base-emitter resistance		
Little diagnostic value		
Collector-emitter with base shorted to emitter		
I_{CES} high	(a) much higher than I_{CBO}. h_{FE} almost normal, but with parallel leakage	Base channel, or other path from collector to emitter. Comparison with I_{CBO} measures shunt path resistance.
	(b) much higher than I_{CBO}. h_{FE} low	Crack across both junctions. Check for high I_{EBO} and floating emitter potential.
	(c) I_{CBO} also high and almost equal	Collector channel.
	(d) I_{CBO} also high. Both recover in hot dry ambient	Header leakage (external).
$V_{(BR)CES}$ showing snapback (possibly with $V_{(BR)CES}$ less than $V_{(BR)CBO}$)		Significant series resistance to emitter or base (Fig. 11).
$V_{(BR)CES}$ low, equal to $V_{(BR)CEO}$		Punch-through, collector to emitter.
Three-terminal characteristics		
Common base operation		
h_{FB} low at all input levels	f_T and h_{FE} also low	Thick or low resistivity base. Examine cross-section.
Common emitter operation		
h_{FE} non-linear with base input	(a) low at low levels, and decreasing at high levels	Narrow and/or lightly-doped base. Examine cross-section.
	(b) very low at low levels, normal at higher levels. I_{EBO} high, I_{CBO} normal	Base-emitter leakage (q.v.).
	(c) very high at low levels, reducing to normal at high levels	Collector-emitter channel, not touching base contact, acting as a f.e.t. (especially in planar n-p-n).[12] Check that slope of a plot of ln I_C vs. $V_{BE} < q/kT$.
h_{FE} low for all input levels	(a) h_{FB} and f_T also low. Possibly 'looped' characteristics	Thick or low resistivity base. Examine cross-section.
	(b) $V_{(BR)CBO}$ low, I_{CBO} and I_{CEO} high	Collector channel (especially in planar p-n-p). See above test for expanded contact devices.[19]
h_{FE} high at all input levels	I_{EBO} rather high, $V_{(BR)EBO}$ possibly low	Base inversion extending emitter area in devices of low uniform base doping (especially n-p-n).
$V_{CE(Sat)}$ high for all input levels	(a) $V_{BE(Sat)}$ normal. High thermal resistance	High collector resistance, or poor collector bond in header-mounted devices.
	(b) $V_{(BR)EBO}$ soft, h_{FE} low, $V_{BE(Sat)}$ high	Poor emitter bond. Examine cross-section.
$V_{CE(Sat)}$ low at low collector currents, increasing more rapidly at higher levels	$V_{(BR)CBO}$ possibly high	High resistivity collector region in epitaxial device.[20] (Fig. 12).
$V_{BE(Sat)}$ high for all input levels	$V_{(BR)EBO}$ soft, h_{FE} low, $V_{CE(Sat)}$ normal	Poor base bond.
'Ballooning' and collapse of characteristics on curve tracer	Device runs hot	Thermal runaway. Increase of forward base drive reduces collector voltage for a given collector current (cf. opposite effect with second breakdown).

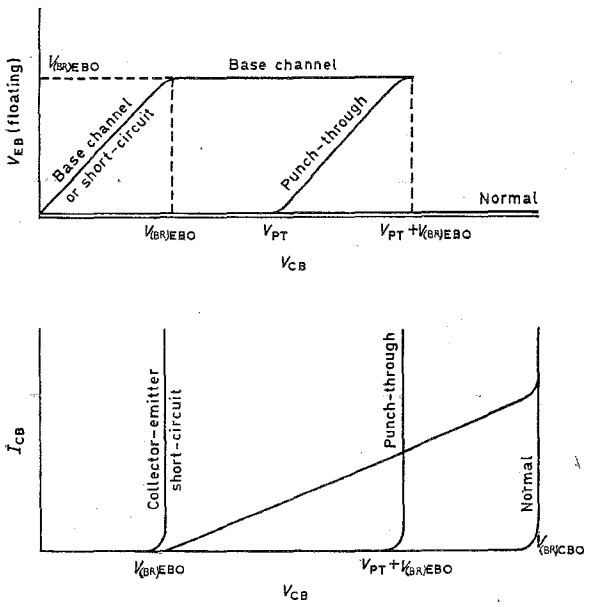
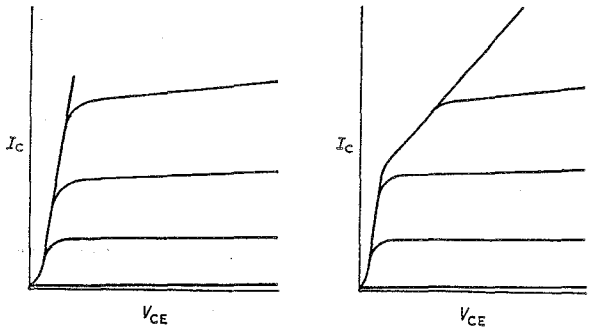


Fig. 10. Effects of emitter junction on collector-base characteristic.

devices, so that to detect them on a spot check might be impossible. However, the data recorded on life tests may reveal the trends, so that this is an area where the much-maligned long-term test may actually give useful information.

The details of leakage current changes with surface state are quite complex, but a very valuable simulation of some of the effects has been reported by Reddi,[11] who used a gate electrode over the emitter-base oxide to swing planar devices of various doping profiles from base inversion to emitter inversion. These emitter junction leakage current results are summarized in Fig. 13, in which the onset of tunnelling at high base doping levels will be obvious. The results shown are for n-p-n transistors: p-n-p devices give results which are basically similar, with the reservation that the common dopant (boron) used for p^+ emitters does not



(a) Low collector body resistance. (b) High collector body resistance.

Fig. 12. Common-emitter characteristics of epitaxial devices.

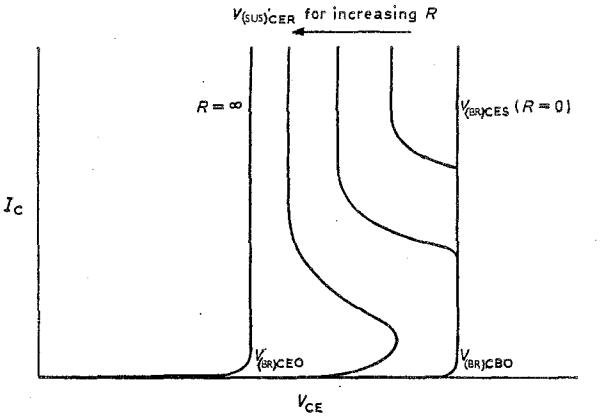


Fig. 11. Relationship of I_{CBO}, I_{CES}, I_{CER} and I_{CEO} characteristics.

reach as high a surface concentration as the phosphorus used for n^+ emitters, so that the normal n-type surface tendency has an earlier incidence in the p-n-p results.

Figure 13(a) is for a base surface concentration of 10^{18} cm^{-3}. In this and subsequent curves, there is tunnelling current at the emitter inversion end of the scale, and minimum current at the ideal 'flat band' condition (when neither side of the junction is depleted or accumulated). As the base becomes depleted, there

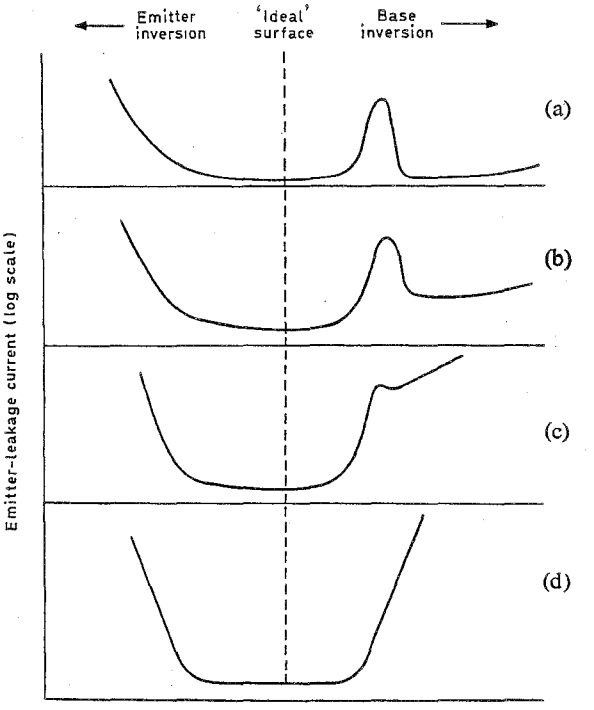


Fig. 13. Effect of changes of surface potential on emitter junction leakage currents.

(a) $C_{BS} = 10^{18}$ cm^{-3} (b) $C_{BS} = 3\times10^{18}$ cm^{-3}
(c) $C_{BS} = 5\times10^{18}$ cm^{-3} (d) $C_{BS} = 7\times10^{18}$ cm^{-3}

is a peak where the surface recombination takes effect, while beyond this, the field-induced junction moves the depletion layer inwards from the surface, and the bulk recombination rate operates to give a current similar to that under flat-band conditions. Figure 13(b) corresponds to a base surface concentration C_{BS} of 3×10^{18} cm^{-3}. Here the bulk recombination rate is increased below the surface, so that when the field-induced junction moves in, the leakage current is higher than at flat-band. In Fig. 13(c), with $C_{BS} \simeq 5\times10^{18}$, there is appreciable tunnelling beyond the surface recombination peak, while at $C_{BS} \simeq 7\times10^{18}$, in Fig. 13(d), the peak is lost in the large tunnelling current to give a nearly symmetrical curve.

Since gain is inversely proportional to base current, we can take the inverse of these curves to represent gain changes, and if there is a progressive change in surface charge density, we can regard the horizontal axes as time axes. On this basis, according to the starting-point, we can simulate many of the upward, downward, or fluctuating changes of gain observed in the early life of many transistors.

Smith and Vaccaro[7] have discussed the rate laws governing the change of properties of p-n junctions in terms of the various known surface, volume, and contact degradation mechanisms. The application of this approach to transistors presents more difficulty, because of junction interactions. In any case, the problems of monitoring the very early stages of degradation and singling out likely specimens for detailed kinetic study of long-term mechanisms are not to be underestimated.

8. Conclusions

The Table shows that some features of transistor behaviour, as seen on a curve tracer display, can lead to quite firm conclusions as to the physical faults which exist. These faults are largely those concerning the bulk junction structure, and those surface and external features which are ohmic in character. When it comes to channels and other non-linear effects, ambiguity sets in rapidly, and although the electrical behaviour may be fully characterized, the physical origins can often be discovered only after extensive examination with a variety of techniques. Consideration of changes of gain, breakdown voltages, and leakage currents during life, can, if these have been recorded, help to remove the ambiguities. It is always important to obtain the maximum of electrical information about a suspect transistor in its encapsulated state, since any subsequent treatment by the failure analyst, even if not actually destructive, may produce irreversible changes which mask the original fault forever. Success in the overall field of failure analysis depends critically on this initial step of intelligent electrical testing.

9. Acknowledgment

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Manuscript first received by the Institution on 25th February 1969 and in final form on 17th June 1969. Paper No. 1285/CC57.)