May 21, 1965

MEMO TO: File

SUBJECT: 1401 Stage II Clock and I/O Delays

Attached is a description of the 1401 Stage II circuit and logic delays encountered in the service request - service response toop.

Logic flow of the Chape II Serial I/O Service Request - Service Repeat e-Service Repeats e-Service Repeats e-Service Repeats e-Service Repeats e-Service as the continuous and militamus calculated delays through each block, and the measured delay through each block. The calculated values were obtained from the IFM Candards Hook in conjunction with IMT. Loo PaintIV of Department 200 (Circulus Sandards). The measured values were found on 1401 #26575 on April 24, 1962, on the Endicott final total time.

Also included is a timing chart of the clock start circuitry, and cumulative figures for service response delays.

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IP/ka

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		uSEC	USEC	BEEC
1.	Delay from output of Service Request terminator on OZAZ to clock control line on OZAZ Fig 1 - BE	1.469	,391	. 400
2.	Delay from clock control line on 01B3 to powered clock pulse on 01B3 Fig 1 - EN	1.988		
3.	Delay through Service Response trigger Fig 1 - NO	.310	* ,112	.100
4.	Time from clock stop set to next oscillator pulse Fig 2 - H	.842	.842	.842
	One oscillator cycle defay (just miss turn off a clock stop tripger) Fig 2 - A	2,885	.000	2.885 and .000
6.	075 time (service response for write) related to 11.54 ms clock cycle	7.212	7.213	7, 212
7.	030 time (service response for read) related to 11.54 ms clock cycle	2,885	2.885	2,885
8.	Clock turn on delay (2) + (4) + (5)	5.715	1.164	4.227 and 1.342
9.	Service Response terminator to Service Response driver for a write operation (1) + (2) + (3) + (4) + (5) + (6)	14,706	8.879	11.939 and 9.054
10.	Service Request terminator to Service Response driver for a read operation (1) + (2) + (3) + (4) + (5) + (7)	10,379	4, 552	7.612 and 4.727



