1401 MULTIPLY/DIVIDE (Revised)

1. Aux Storage Set Latch
   - On = (I~)(Gum)(Div Op + Mult Op) ✓
   - Off = (E~)(t9 – t0) + (Start Rst)

2. Transfer Address Reg. Gate = (Aux Stor Set Latch) ✓

3. A Cycle Eliminate Latch
   - On = (A Reg WM)(R~)(t6 – t9)(Div Op + Mult Op) ✓
   - Off = ($\overline{\Delta B < A\,Lt}$)(Set Quot Trig)($t_3$ – t_0) + (I~)
     + (ΔB < A)($\overline{\text{Set Quot Trig}}$)($t_3$ – t_6)(Process)
     + (Multiplier Lt)(Sig. Digit)($\overline{\text{E Aux Cycle}}$)($t_3$ – t_6)(Process)

4. X-Position Latch
   - On = (A Cycle Elim Lt)(t_3 – $t_{4.5}$)(Process)
   - Off = ($\overline{\text{A Cycle Elim Lt}}$)($t_0$ – t_3)(Process) + I~ ✓

5. Set Quotient Trig
   - On Gate = ($\overline{\text{Set Quot Trig}}$)(X-Pos Lat) (A Elim Lt)
   - Binary Set = (Div Op)(Process)(t_0 – t_3) ✓
   - Off Gate = (Set Quot Trig)
   - Reset = Start Reset

no good trigger will set again (turn off X lat at 10.5 or 9 ?)

SP – 4/20/6[illegible]

1401 MULTIPLY / DIVIDE (Revised)

6. Sign Trigger

On Gate = [(A~)(Aux Stor Set Lt) + (B~)(Div Op) + (Clear B Fd Lt)(B~)(Multiplier Lt)]($\overline{\text{Sign Trig}}$)

✓ Binary Set = [($t_3 - t_6$)(B Reg B $\overline{A}$)]($\overline{\text{End Div Lt}}$)

X Off Gate = [(Div Op) + (Clear B Fd Lt)(Multiplier Lt)] • (B~)(Sign Trig)

Reset = I~ +

7. End Divide Latch

X ✓ On = (B~)(B Reg B)(Div Op)($t_6 - t_7$)

Off = I~

8. Reverse Scan Latch

On = (B < A Lt)(Set Quot Trig)($t_{10.5} - t_0$)

X ✓ Off = ($\overline{\text{A~ Elim Lt}}$)($t_7 - t_0$)

9. A Latch

On = (Δ Subt A Lt)($\overline{\text{Δ Subt 2A Lt}}$)(Δ A-Aux Cycle)

X ✓ + (Multiplier Lt)(B Reg I)($\overline{\text{B-Aux Cycle}}$)(Process)

Off = (X-Pos Lt)(Process)($t_0 - t_{1.5}$) + (Start Rst)

[illegible]

1401 Multiply/Divide (Revised)

10. 2A Latch

On = (Δ Subt 2A Lt)(Δ A-Aux Cycle)
+ (Multiplier Lt)(B-Aux Cycle)(Mlr. ≥ 2)(Process)

Off = (X-Fac LAT)(Process)($t_0 - t_{1.5}$) + (Start Rst)

11. Clear B Field Latch

On = (Mult Op)(I-)(Gm)

Off = (Set Prod Sign Lt)(Process)($t_0 - t_2$) + (Start Rst)

12. Force B2 = (Clear B Fld Lt)(Multiplier Lt)(Not Block Op · B-)
+ (Multiplier Lt)(B Reg > 2)(Not Block Op · B-)

13. Multiplier Latch

On = (X-Fac Lt)(Mult Op)(Process)($t_0 - t_{1.5}$)

Off = (A Cycle Elim Lt)(Process)($t_0 - t_2$)

14. Set Prod Sign Latch (MULTIPLIER LAT)

On = (Clear B Fld Lt)(A[illegible])($t_0 - t_2$)

Off = (Δ B Aux)(Δ A Aux)(Process)($t_0 - t_1$)

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1401 Multiply/Divide (Revised)

15. A-Aux Star Gate Out = (Delta A-Aux Cycle)(t_{9-0})

16. B-Aux Star Gate Out = (Delta B-Aux Cycle)(t_{9-0})

17. A-Star Gate Out = (A-Aux Star Gate Out)(Δ A AUX ~)

18. B-Star Gate Out = (B-Aux Star Gate Out)(Δ B AUX ~)

19. B-Aux Star Set (Units) = (Delta B-Aux Cycle)(B < A Lt)
+(Aux Star Set Lt)(Delta B~)+(Δ B-Aux Cycle)(Multiplier Lt

20. B-Aux Star Set (Tens & Hundreds) = (B-Aux Cycle)(B < A Lt)
+(Aux Star Set Lt)(B~)+(B-Aux Cycle)(Multiplier Lt)

21. A-Aux Star Set (Units) = (Aux Star Set Lt)(Δ A~)

22. A-Aux Star Set (Tens & Hundreds) = (Aux Star Set Lt)(A~)

23. Compliment Gate = (A Lt + ZA Lt)(B~)(DivOp)(X-Pos Lt)
+(Multiplier Lt)(B Reg > 2)(B-Aux Cycle)(Process

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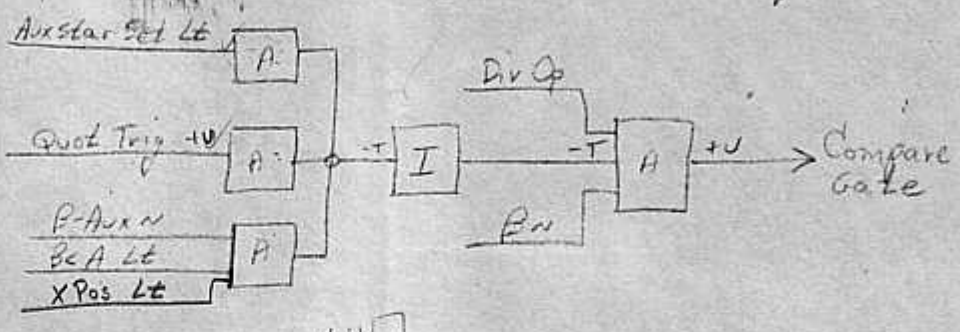
1401 Multiply/Divide (Revised)

24. Compare Gate = (B~)(Div Op)[(Aux Star Set Lt)+(Quot Trig)+(B Aux~)(Be A Lt)



+U]

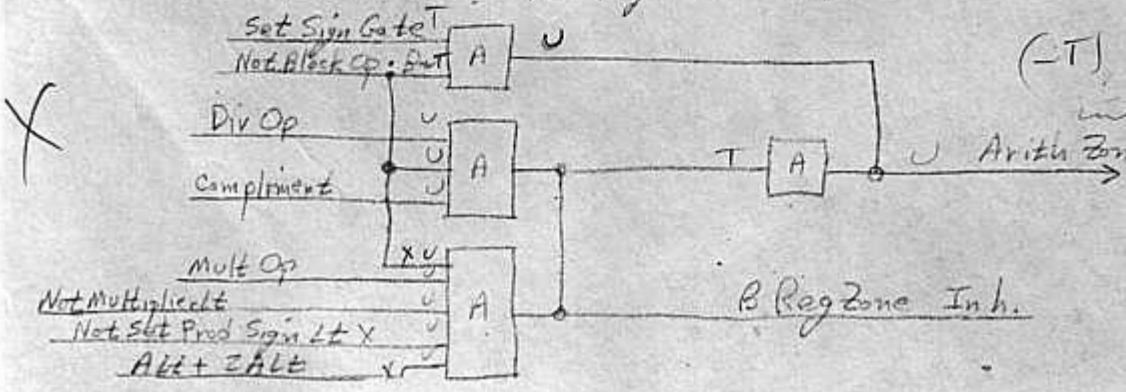
25. Set Sign Gate = (End Div Lt)(Set Quot Trig)
+(Set Prod Sign Lt)(B-Aux Cycle)

26. Force Adder Carry = (Div Op)(A-Aux Cycle)(t_9-t_0)

27. Arithmetic Digit Gate = [(Quot Trig)+(ALt +2 ALt)(X-Pos Lt)
+(Multiplier Lt)(B Reg >2)(B-Aux Cycle)](Not Block Op · Bn)

(-T) inhibit

28. Arith Zone Gate & B Reg Zone Inh.



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1401 Multiply / Divide (Revised)

29. B Reg Transfer Gate
$= (\overline{\text{Arith Digit Gate}})(\text{Div Op})(\text{Not Block Op} \cdot \text{B}\sim)$
$+ (\text{X-Pos Lt})(\text{B-Aux Cycle})(\text{Mult Op})(\text{Not Block Op} \cdot \text{B}\sim)$

30. Set A Translator Output To Z ("Dot or" with #39)
$= (\text{B Reg} > 2)(\text{Multiplier Lt})(\overline{\text{B-Aux Cycle}})(\text{Process})$

31. Block Zone Adder = (Div Op + Mult Op)
$+ \sim$

32. Adder Carry Trig Gate = (Mult Op + Div Op)(Adder Carry)(Arith Dig Gate)

33. Set A Bit In Mem = (Set Sign Gate)$(\overline{\text{Sign Trig}})$(Not Block Op · B~)

34. Set B Bit In Mem = (Set Sign Gate)(Not Block Op · B~)

35. Set Cz In Mem = (Set Sign Gate)$(\overline{\text{Sign Trig}})$(Not Block Op · B~)

Put on 02A1 36. Reset Delta Compare Latches = (A-Aux Cycle) + ~~Start Rel~~
$+ \text{I} \sim$

37. A Gate = $(\overline{\text{X-Pos Lt}})$(A Latch) + $(\overline{\text{Div Op} + \text{Mult Op}})$
(-T) -T

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Ho1 MULTIPLY / DIVIDE (Revised)

✓ 38. 2A Gate (-T) = (X-pos Lt)(2A Latch)

Is this A Reg translator output?? X 39. Set A Reg to 1 = (Quot Trig)(Δ Subt A Lt)(Δ Subt 2A Lt)
-1

X 40. Set A Reg to 2 = (Quot Trig)(Δ Subt 2A Lt)(~~Δ Subt A Lt~~)
-1

X (on 02 A7) 41. Set A Translator Output to ϕ = (A Gate)(2A Gate)(Set L1)(Set L2)

X 42. Set Arith Check Latch
(Arith Digit Gate - Calc)(Arith Check)(Process)(t7.5 - t9)

X 43. Overflow SET LAT = ~~(Set Quot Trig)(Adder Carry)~~ Not Carry Trig Output
(Set Quot Trig)(Δ subt 2A lat)(B reg 8)

X 44. I/E Change = (Over flow) + (End Div Lt)(B< A Lt)(Set Quot Trig)
+ (WM)(Multiplier Latch)(B Reg ϕ) + BLANK)
·(CLEAR B FIELD LAT)
+ (Set prod sign lat)(B aux cy)
·(A lat + 2A LAT)

Check this for timing
(When is adder carry recognized)
(Paul says OK)

WM SEPRAT

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1401 Multiply/Divide (Revised)

Delta A-Aux Cycle Latch → must be set at $t_6 - t_9$

On = (A-Aux Eliminate 'Off')(Process Lt)

Off = (A-Aux Cycle Lt)(Process Lt)($t_6 - t_{7.5}$) + (Start Rst) + (Tape Load) + (Gated Load Key).

A-Aux Cycle Latch

On = (Δ A-Aux Cycle Lt)(Process Lt)($t_0 - t_6$) + (A-Aux STAR Key)

Off = (Δ Process Lt)($t_0 - t_{1.5}$) + (B-Aux STAR Key) + (I-STAR Key) + (A-STAR Key) + (B-STAK Key) + (Mem Scan) + (Print)

Delta B-Aux Cycle Latch · (GWM)(BM)(set pardon latch)

On = (Multiplier Lt)(Φ or Blank)(B-Aux Cycle)(Process Lt)($t_6 - t_{7.5}$) + (Divide)(A-Aux Cycle)(Process Lt)($t_6 - t_{7.5}$)

Should set at 3 time ? (END DIVIDE) Δ B-A)(Set Quot Trig)(Process Lt)($t_6 - t_{7.5}$)

Off = (B-Aux Cycle Lt)(Process Lt)($t_6 - t_{7.5}$) + (Start Rst) + (Tape Load) + (Gated Load Key)

B-Aux Cycle Latch

On = (Δ B-Aux Cycle Lt)(Process Lt)($t_0 - t_6$) + (B-Aux STAR Key)

Off = (Δ Process Lt)($t_0 - t_{1.5}$) + (A-Aux STAR Key) + (I-STAR Key) + (A-STAR Key) + (B-STAR Key) + (Mem Scan) + (Print)

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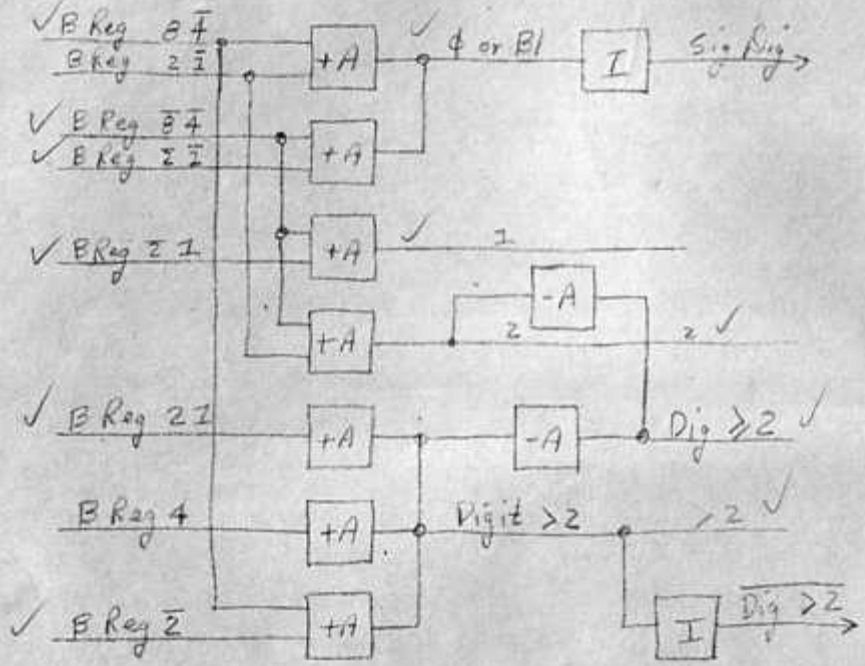
1401 Multiply Digit Recognition



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