November 9, 1959

MEMORANDUM TO: Mr. J. A. Harvilchuck

SUBJECT: R&S Item S-34

REFERENCE: Your Memo dated October 28, 1959
R&S Item S-34 dated October 26, 1959

The B reg check occurs at 6-7.5 time,
the A reg check occurs at 7.5-9.0 time, and
the Adder check occurs at 7.5-9.0 time. Any one of these three checks will stop the 1401 at the end of the cycle in which the check occurs.

The inhibit channel check will occur at 090-000 time. This is too late to stop the machine within this cycle and it will stop at the end of the next cycle. This may be re-evaluated at a later date to see if this condition can be improved.

When a Storage Address Register check occurs we try to prevent a reset and set of the address register and stop the machine at the end of the cycle. There are some close timing conditions involved and a definite statement cannot be made at this time, that this will definitely work.

The op register check will occur during all cycles except I op. This condition may be re-evaluated at a later date to determine the true value gained by changing this check.

W. S. Schaffer

WSS:bd
cc: Mr. P. Farbanish
Mr. J. J. Ingram
Mr. F. O. Underwood