October 28, 1959

MEMORANDUM TO: Mr. W. S. Schaffer

SUBJECT: R&S Item S-34

Please examine the enclosed R&S Item S-34 and evaluate its' merit and application

J. A. Harvilchuck

J. A. Harvilchuck
Department 280
R&S Liaison

cc: Mr. P. Farbanish
Mr. J. J. Ingram
Mr. F. O. Underwood

Date Received 10/26/59

Date Typed 10/26/59

Project 1401

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Date Transmitted 10/26/59

Approved By H. W. Morrow

Area Affected	Recommendations and/or Comments	Name	Date	Code
Register Content on Error Stop	If the 1401 process unit stops running because of a detected error, the contents of the data and program registers should retain useful information to locate the source of the error. The following paragraphs state the requirements for good visual display if any of the six data-flow checks sense an error and cause a machine stop. 1. B Register Check: A B Register check should be gated by a clock pulse that is early enough in the cycle to cause a normal program stop. The faulty character will then appear in the B register indicators, and its memory location will be displayed in the Address Register indicators. This requirement is met by the Release model of the 1401 by gating the check coincidently with the Control Process turn off. 2. A Register Check: An A Register check should be made at a time to retain the character in the B register that has been moved to the A register. It is not necessary to refer to the Address Register, since if there is no B register check, the memory character is not of interest.	H. M.	10/26/59	

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Project 1401

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	The Release Model makes an A register check at clock time 75-90. The Control Process turn-off is time 60-75. The error stop will, therefore, occur the following cycle with a character in the B register that is not related to the error. The original character can be manually displayed from memory by first manually calling out the A-MAR; then adding the number one and setting this address in the Address switches; then displaying. It is far simplier to cause an error stop that turns off the Control Process latch later than the normal program stop, and retain the conditions of the error. 3. Inhibit Channel Check: An Inhibit parity error can be picked up only during the write portion of the core memory cycle too late to keep the invalid character from going into memory. This check is gated by time 75-90 on the Release model and it cannot be expected that the clocking pulse could be an earlier one. This time coincides exactly with the Address Register reset and set time and could not reliably block an address change. However, the address is not the only useful register content. The A and B registers also feed the adder, and their retention is significant. The reset and set of the data registers does not take place until the next cycle. The Control Process latch can be turned off later than normal and preserve a more effective visual display.			

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	4. Adder Output Check: A Qui-binary validity check will necessarily occur late in the cycle since it must be held off until after all stages of adder and translator delay. Consequently, the Address Register cannot be referred to, to find out where the invalid character is stored in memory. It can only be located by displaying the B-MAR and either adding or subtracting the number one after determining the conditions of address progression. This procedure is time-consuming and diverting to trouble analysis. More useful to servicing the 1401 is the retention of the A and B register contents to "freeze" the adder output and the Inhibit Channel indication. 5. Memory Address Check: An addressing parity error has to retain the contents of the Address Register to provide for efficient analysis of addressing failures. An "Address OK" signal should gate both the reset and set of the Address Register. 6. Op Register Check: The Op register check should cause an error stop in I op if the failure results from data movement to the Op register or its reset or set. A late stop should be made to retain the Op character in the B register.			