December 22, 1959

MEMORANDUM TO: Mr. W. S. Schaffer

SUBJECT: R & S Item R-37

Please examine the enclosed R & S Item R-37 and evaluate its merit and application.

J. A. Harvilchuck
Dept. 280
R & S Liaison

JAH:mk
Encl.

CC: Mr. K. A. Bell
Mr. P. Farbanish
Mr. J. J. Ingram
Mr. F. O. Underwood

BL: J. Harvilchuck - 280

BP: J. Keough - 294
T. McAdon - 294
H. Morrow - 294

RELIABILITY & SERVICEABILITY PROGRAM REVIEW

Date Received 12/10/59

Date Typed 12/10/59

Item R-37 Page 1

Project 1401

Approved By H. W. Morrow

Date Transmitted 12/10/59

Area Affected	Recommendations and or Comments	Name	Date	Code
Arith. Digit Adder	The attached logic which eliminates two stages in the digit adder is recommended to reduce the delay of information through the digit adder. The two stages are eliminated by combining: 1. The Arith. digit adder translate and the Arith. digit inhibit gate and 2. The Quinary adder output stage and Binary Carry stage. Since this changes the Adder Quinary output line type from a u line to a T line, the Qui-Binary-Validity check logic blocks must be implemented with the complementary blocks. The Indicators are placed on the Inhibit lines and no longer will indicate Arith. digit output only but will indicate any information on inhibit. Modifications to inhibit gate times may be necessary to achieve optimum indication of the inhibit lines. Alternate methods of implementing the adder Carry are indicated on the attached logic. The transister and card counts follow on the next page.	T. McAdon	12/10/59	

Date Received 12/10/59

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Project 1401

Item R-37 Page 2

Date Transmitted 12/10/59

Approved By H. W. Morrow

Area Affected	Recommendations and or Comments						Name	Date	Code
	Present Adder. Cir.			Proposed Adder. Cir.					
	Adder.	Inh. Gate	Cards	#1 Add Carry	Cards	#2 Add Carry			Cards
CN	1	3	1	6	2+	6			2
CP	24		6	12	3	8			2
2way An	11	5	6	13	4	13			4
2way Ap	11		4	19	6	19			6
3way An	1		1	5	3	5			3
4way An	1			0		0			
4way Ap	0			1	1	1			1
In	3		1	2	1	2			1
Ip	1		1	2	1	2			1
DEn	7		3	2	1	2			1
DEp	2		1	7	3	7			3
EFn	2			0		1			
EFp	0			2		2			
Ext. (EFn)	2		2	0		1			1
Ext. (EFp)	0	—	—	3	2	2			2
Total	64 8	8	26	71	27	68			27

Transistors 72 Present Adder Cir. 26 Cards Present Adder Cir.

71 Transistors #1 Proposal
27 Cards #1 Proposal

68 Transistors #2 Proposal
27 Cards #2 Proposal