IBM Field Engineering

Maintenance Manual

1401 Data Processing System

P.M. Schedual on P. 20

IBM®

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1401 Data Processing System

MAJOR REVISION (August 1963)

This manual, 225-6487-3, supersedes 225-6487-2. Significant changes have been made throughout, and this edition should be reviewed in its entirety.

This manual covers IBM 1401 systems with serial numbers above 1401-20000. At this point a revision was made in the system logics and hardware placement. Except for logic and test-point references, this manual can serve for earlier systems.

Address comments regarding this publication to IBM Product Publications, Endicott, New York

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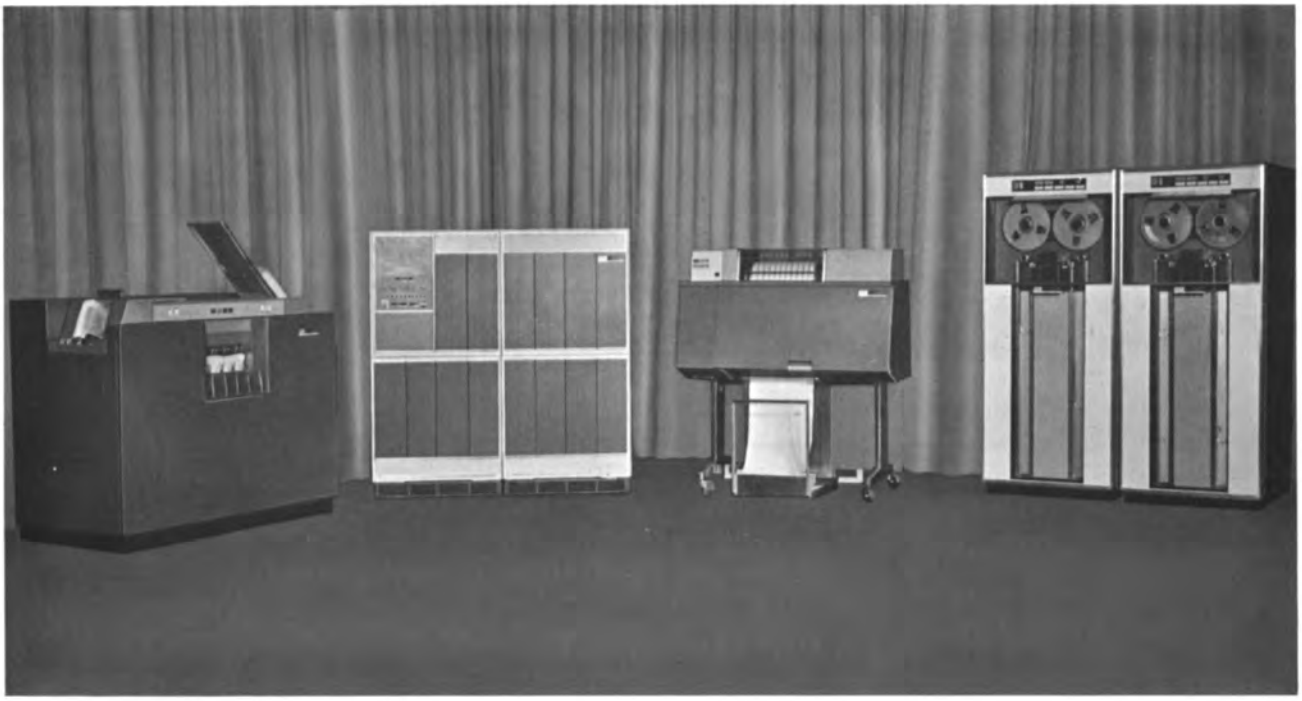


Figure 1. IBM 1401 Data Processing System

Personal safety is a vital part of customer engineering. Insure your own safety, as well as the safety of those around you, by being safety conscious at all times. Practice the following safety precautions:

1. Always wear safety glasses when hazardous conditions exist.
2. Remove any sharp edges on machine frames, gates, etc., that could cause lacerations.
3. Remove rings, wristwatches, and any other jewelry when working around rotating parts or live electrical circuits.
4. Use proper lifting techniques.
5. Replace all safety guards and shields on completion of a call.
6. Practice good housekeeping.
7. Remember that ac power exists in the processing unit even when power is turned off. Always disconnect the power connectors from the power source before working in the power-supply area.

The information in this section is identified by a tab marker on the edge of each page. The following is a list of illustrations and charts by figure number.

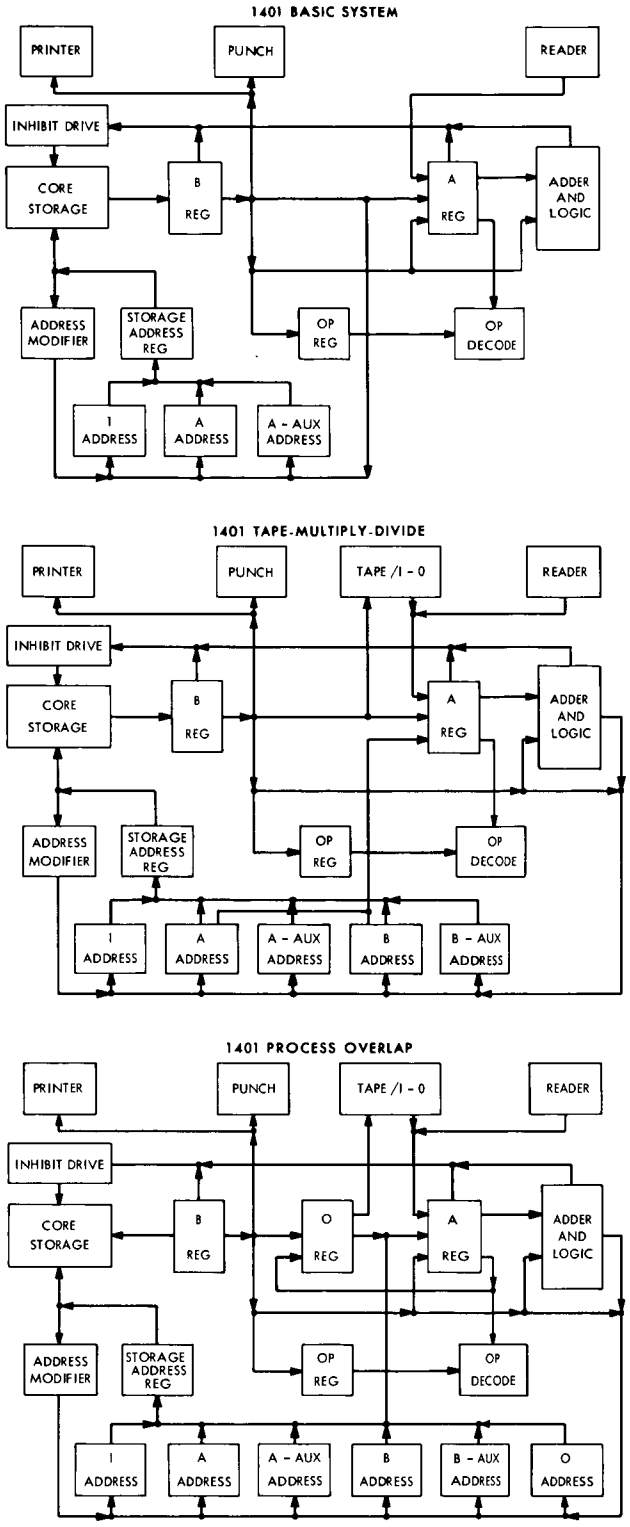


Figure 2. System Data Flow

MFI	Feature	MFI	Feature	MFI	Feature
APF	Advanced Program	IOC	Input/Output Common	RP	Punch Feed Read
BA	Basic	LST	Low Speed Tape	SBA	Sterling Basic
BINQ	Buffered Inquiry	MD	Any Tape Drive	SEE	Sterling Expanded Edit
BSR	1210 Bank Sorter	M2	729 II or V	SMD	Sterling Multi/Divide
BSR	Data Transmission	M3	7330	SS	Sense Switches
BT	Bit Test	M4	729 IV or VI	STC	Selective Tape Lister
CH	Column Binary	M6	729 II/V or IV/VI	X	RPQ
CF	Card Feed (1404)	M8	800 BPI Density	XSS	Space Suppress
CFC	Card Feed Compare	MD	Multiply Divide	1311	1311 Feature
CM	Attachment Circuitry	MM	1311 Multi Module	1K	1.4K Storage Only
CW	Compressed Tape	MR	Move Record	2K	2K Storage Only
DH	Dual Hopper	MT	Magnetic Tape Adapter		4K Storage Only
DR	Drums	MX	Multiplexing		8K Storage Only
DS	Dual Speed Carriage	NNU	No Numeric Paint Control		12K Storage Only
EE	Expanded Print Storage	NPF	No Print Storage		1M-1.4K Storage & Above
EX	Expanded Storage	NU	Numeric Paint Control		2M-2K Storage & Above
FCF	51 Column Feed	OV	Overlap		4M-4K Storage & Above
FP	Read Punch Release	OVR	Overlap Read Punch		8M-8K Storage & Above
HL	Hi-Lo Equal Compare	OVRP	Overlap Punch Feed Read		12M-12K Storage & Above
IN	Indexing	OVT	Overlap Tape		16M-16K Storage & Above
INQ	Inquiry Station	PF	Print Storage		100-100 Print Positions
I/O	Input/Output	PT	Paper Tape Adapter		132-132 Add Print Position
IOA	Input/Output	RAM	Disc Storage		

Figure 3. Machine Feature Index

PRINT ARRANGEMENT		DEFINED CHARACTER	CARD CODE	BCD CODE	PRINT ARRANGEMENT		DEFINED CHARACTER	CARD CODE	BCD CODE
A	H				A	H			
		BLANK		C	G	G	G	12-7	B A 4 2 1
.	.	.	12-3-8	B A 8 2 1	H	H	H	12-8	B A 8
□	)	□	12-4-8	C B A 8 4	I	I	I	12-9	C B A 8 1
		[Left Bracket (Special Character)	12-5-8	B A 8 4 1	–	–	! (Minus Zero)	11-0	B 8 2
		< Less Than (Special Character)	12-6-8	B A 8 4 2	J	J	J	11-1	C B 1
		≢ Group Mark (Note 1)	12-7-8	C B A 8 4 2 1	K	K	K	11-2	C B 2
&	+	&	12	C B A	L	L	L	11-3	B 2 1
$	$	$	11-3-8	C B 8 2 1	M	M	M	11-4	C B 4
*	*	*	11-4-8	B 8 4	N	N	N	11-5	B 4 1
		] Right Bracket (Special Char.)	11-5-8	C B 8 4 1	O	O	O	11-6	B 4 2
		; Semicolon (Special Character)	11-6-8	C B 8 4 2	P	P	P	11-7	C B 4 2 1
		Δ Delta (Mode Change)	11-7-8	B 8 4 2 1	Q	Q	Q	11-8	C B 8
–	–	–	11	B	R	R	R	11-9	B 8 1
/	/	/	0-1	C A 1	≠	≠	≠ Record Mark	0-2-8	A 8 2
,	,	,	0-3-8	C A 8 2 1	S	S	S	0-2	C A 2
%	(	%	0-4-8	A 8 4	T	T	T	0-3	A 2 1
		∨ Word Separator	0-5-8	C A 8 4 1	U	U	U	0-4	C A 4
		\ (Special Character)	0-6-8	C A 8 4 2	V	V	V	0-5	A 4 1
		⧺ Tape Segment Mark	0-7-8	A 8 4 2 1	W	W	W	0-6	A 4 2
≠	≠	⅋ (Special Character Note 2)		A	X	X	X	0-7	C A 4 2 1
#	=	#	3-8	8 2 1	Y	Y	Y	0-8	C A 8
@	'	@	4-8	C 8 4	Z	Z	Z	0-9	A 8 1
		: Colon (Special Character)	5-8	8 4 1	0	0	0	0	C 8 2
		> Greater Than (Special Character)	6-8	8 4 2	1	1	1	1	1
		√‾ Tape Mark	7-8	C 8 4 2 1	2	2	2	2	2
&	&	? (Plus Zero)	12-0	C B A 8 2	3	3	3	3	C 2 1
A	A	A	12-1	B A 1	4	4	4	4	4
B	B	B	12-2	B A 2	5	5	5	5	C 4 1
C	C	C	12-3	C B A 2 1	6	6	6	6	C 4 2
D	D	D	12-4	B A 4	7	7	7	7	4 2 1
E	E	E	12-5	C B A 4 1	8	8	8	8	8
F	F	F	12-6	C B A 4 2	9	9	9	9	C 8 1

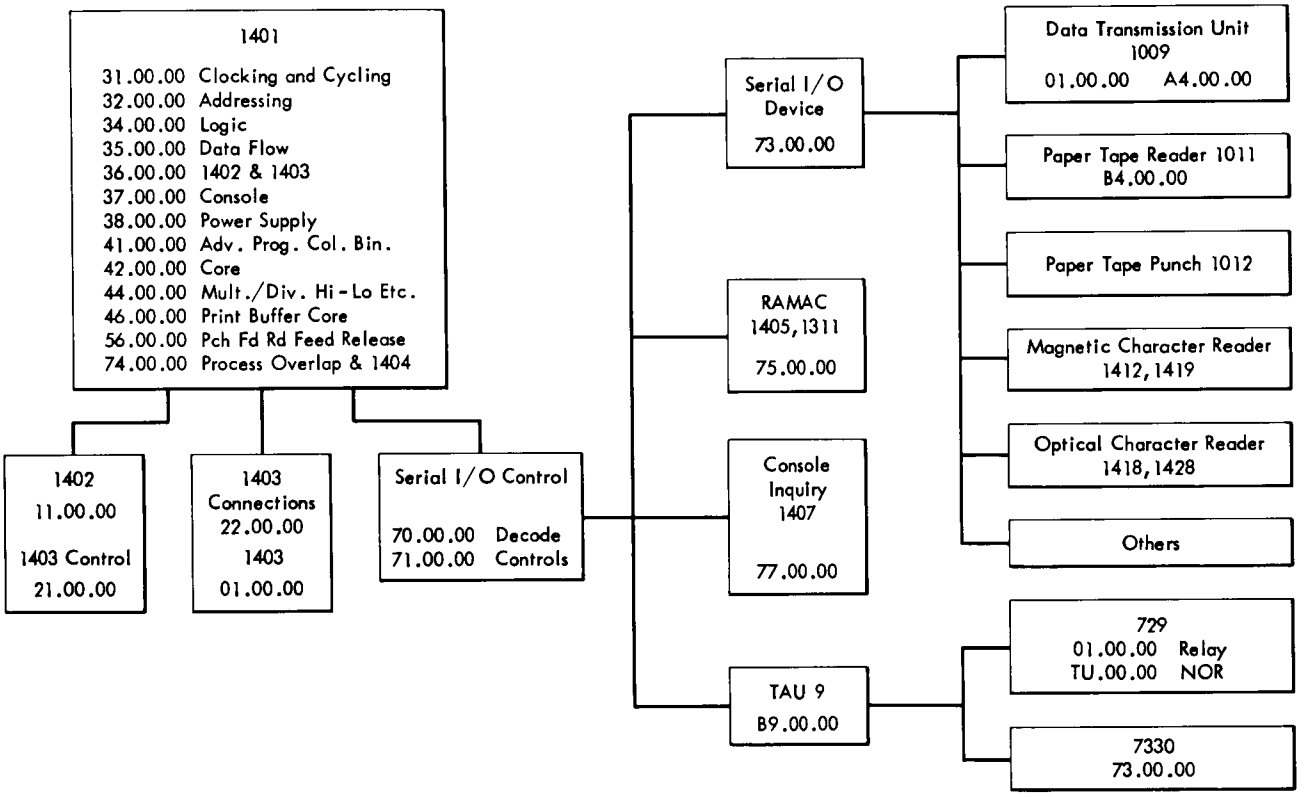
The system has the ability to read MLP card codes in the read feed only. The system ignores the 8-9 punches when they appear in the same column. The system does not punch out MLP card codes.

Note 1. If specified, this code can be made compatible with 705 Group Mark Code (12-5-8).

Note 2. The A-bit coding must be program-generated in the system (it cannot be read from a card; it can be punched as a zero). It is used in conjunction with the C-bit to indicate a blank position on tape that was written in even-bit parity.

Note 3. Other special character printing arrangements can be obtained.

Figure 4. IBM 1401 Character Code Chart



01A1	01A2	01A3	01A4
Core 42.00.00	Console 37.00.00	Data Flow 35.00.00 A&B Register	Print Buffer 46.00.00

01B1	01B2	01B3	01B4
Op Register 35.00.00 Carriage 36.00.00 Options 41. 56.	Clocking and Cycling 31.00.00	Time 31.00.00 Logic 34.00.00	Read/Punch 36.00.00

01A5	01A6	01A7	01A8
Carriage 46.00.00 Print Buffer 46.00.00	Print 36.00.00	Addressing 32.00.00	Addressing 32.00.00 Address Decode 42.00.00

01B5	01B6	01B7	01B8
Hammer Drive 36.00.00	1 Ring 31.00.00 Logic 34.00.00	Rd Pch Chk 36.00.00 Pch Fd Rd 56.00.00	Cables

02A1	02A2	02A3	02A4
I/O Control 71.00.00 TAU Conn B9.00.00	I/O Decode 70.00.00 Serial I/O 73.00.00	Power Supply 38.00.00	Power Supply 38.00.00

02B1	02B2	02B3	02B4
Overlap 74.00.00	TAU(00XA) B9.00.00	TAU(00XB) B9.00.00	TAU(00XC) B9.00.00

02A5	02A6	02A7	02A8
Power Supply 38.00.00	Power Supply 38.00.00	Mult/Div 44.00.00	H L RAMAC Inquiry

02B5	02B6	02B7	02B8
Cables	Adv Program 41.00.00 Comp Word 44.00.00	Mult/Div 44.00.00	1404 74.60.00 Column Binary

Figure 5. ALD Designation

SMS CARD SUBSTITUTION LIST																								
CARD TYPE	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI
2JMX	01A3	F01	BA	01A6	D06	BA	01A7	E17	BA	01B1	D22	BA	01B2	C20	BA	01B3	E05	BA	01B6	C15	BA	01A8	C09	BA
3JMX	01A3	C13	BA	01A7	E06	BA	01A8	B09	BA	01B3	E09	BA	01B4	C10	BA	02A1	D07	MT	01A6	C15	BA	01B3	E12	BA
4JMX	01A3	E01	BA	01A7	A03	BA	01A8	B05	BA	01B1	F13	BA	01B3	C18	BA	01B6	B12	BA	02B6	A16	IN	02A1	C18	MT
AAF	01B1	F08	BA	01B4	D15	BA	01B1	F09	BA															
AEA	01A6	D12	PF	01B5	F18	BA	02A8	E05	RAM	02A8	C17	INQ	01B5	F19	BA	01B5	F21	BA						
AED	01B3	A11	BA	01B7	A04	BA	01B3	A12	BA	01B3	A14	BA	01B3	A15	BA	01B3	A16	BA	01B3	D04	BA	01B3	B26	BA
AJT	02B4	D25	MD	02B4	C20	MD	02B3	B17	MD															
AM	01B3	A25	BA	01A5	A08	PF																		
AC	01B3	C12	BA	01B3	B11	BA	01B3	B24	BA															
CEA	01B3	A21	BA	01B3	C06	BA	01B3	C07	BA	01B3	C08	BA	01B3	C09	BA	01B3	F04	BA						
CED	02A8	F16	RAM	02A8	F17	RAM	02A8	F18	RAM	02A8	F19	RAM	02A8	F20	RAM	02A8	F21	RAM						
CEE	01A8	E02	8M	01A8	E22	BA	01A8	E23	BA	01A8	F02	BA	01A8	F03	BA	01A8	F06	BA	01A8	F07	BA	01A8	F08	BA
CEF	02A8	D17	RAM																					
CEH	01A3	C01	BA	01A3	C03	BA	01A3	C07	BA	01B1	D16	BA	01B1	E08	BA	01B1	E09	BA	02A1	B03	MT	02A1	D10	MT
CEK	01B1	B16	BA	01B1	C15	BA	01B1	C16	BA															
CG	01B1	B19	BA	01B1	C18	BA	01B1	C19	BA	02B6	A25	IN	02B6	A26	IN	01A4	E02	PF	01A4	E06	PF			
CGVV	01A7	B11	BA	01B1	A19	BA	01B1	D25	BA	01B5	E02	BA	01B6	A25	BT	02A1	C09	MT	02A1	C11	MT	01A4	E10	PF
CGVW	02A2	A10	CM	01B6	F09	EE	02A1	C14	MT	01A5	A18	PF	01A5	B18	PF	01A5	C17	PF	01A5	C18	PF	02A8	C22	INQ
CGWW	01A3	B01	BA	01A3	B02	BA	01A7	A02	BA	01A8	B15	BA	01B3	F09	BA	01B3	F16	BA	01B4	F10	BA	02A2	B14	CM
CH	02A8	C10	INQ	02A8	C11	INQ	02A8	C12	INQ	01B5	E16	NPF	01B5	E17	NPF	01B5	F15	NPF	01B5	F16	NPF	01B5	F17	NPF
CHVV	01A7	B20	BA	01A7	E10	BA	01B3	F23	BA	01B4	A08	BA	02A2	A09	CM	02B6	F05	CW	02B6	F11	CW	01B6	F19	EE
CHVW	01A3	B19	BA	01A3	E16	BA	01A8	C05	BA	01B1	B09	BA	01B1	C25	BA	01B2	C24	BA	01B3	D19	BA	01B7	C12	BA
CHWW	01A8	C20	BA	01B3	E15	BA	01B4	A11	BA	01B4	D24	BA	01B5	C03	BA	01B6	C22	BA	01B6	D14	BA	01B7	A24	BA
CJVU	01A8	F04	BA	01B1	B10	BA	01B2	D08	BA	01B7	D07	BA	01B5	E01	BA	01B6	B25	BA	01A6	B08	PF	01A4	E08	PF
CJWF	01A3	A19	BA	01A3	B16	BA	01A8	C22	BA	01B2	B06	BA	01B4	D20	BA	01B6	A07	BA	02A2	B18	CM	02A2	C07	CM
CJWV	01B5	F04	BA	01B5	F05	BA	01A7	A17	BA	01B3	D06	BA	01B5	E03	BA	02A2	B17	CM	02A8	A13	HL	01A6	D02	PF
CJYC	01B3	C20	BA	01B3	C26	BA	01B4	A09	BA	01B5	E06	BA	01B5	E08	BA	01B6	C21	BA	01B7	A09	BA	01A8	B04	BA
CKVU	01A3	D20	BA	01A8	C07	BA	01B1	E13	BA	01B3	B25	BA	01B6	C20	BA	01B3	B10	BA	02A2	B01	CM	02A1	B15	MT
CKWF	01A8	C06	BA	01A8	C18	BA	01B2	B20	BA	01B3	F22	BA	01B3	F25	BA	01B6	B06	BA	01B7	B22	BA	01B7	B25	BA
CKWV	01A7	A18	BA	01B3	C19	BA	01B3	D16	BA	01B6	A18	BA	02A2	A02	CM	02B6	F04	CW	02B6	F23	CW	02A8	A20	HL

Figure 6. Card Substitution List (Part 1 of 5)

SMS CARD SUBSTITUTION LIST																										
CARD TYPE	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI		
CLVQ	01A3	B14	BA	01A3	F09	BA	01A8	B01	BA	01A8	D09	BA	01B1	A07	BA	01B4	D11	BA	01B6	A05	BA	01B7	C06	BA		
CLVR	01A3	A17	BA	01A3	C15	BA	01A8	B08	BA	01B3	C23	BA	01B3	D24	BA	01B4	B09	BA	01B3	D13	BA	01B5	E09	BA		
CLVT	01A3	D10	BA	01A3	D11	BA	01A7	B04	BA	01A7	B05	BA	01B1	A17	BA	01B1	A18	BA	01B2	A19	BA	01B2	C12	BA		
CM	01B3	A24	BA	01A5	B07	PF																				
CNWT	01B3	E18	BA	01A3	D16	BA	01B1	A10	BA	01B1	B22	BA	01B3	D11	BA	01B3	D12	BA	01B5	C04	BA	01B6	D26	BA		
CNWU	01A6	C11	BA	01A6	D03	BA																				
CPWT	01A1	D08	MT	01A5	B05	PF	01A6	B13	BA	02A8	F12	RAM	01A7	B01	8M											
CPWU	01A7	B13	BA	01B1	D10	BA	01B1	E17	BA	01B7	B26	BA														
CQ	01A3	E03	BA	01A3	E08	BA	01A7	E02	BA	01A7	E03	BA	01A7	E09	BA	02A1	B16	MT	02A1	B19	MT	01A4	E03	PF		
CQZT	01A3	C12	BA	01A3	D12	BA	01A8	C16	BA	01B1	E14	BA	01B1	F11	BA	01B3	D05	BA	01B4	B05	BA	01B6	D25	BA		
CQZV	01A8	D03	BA	01B1	C20	BA	01B1	D07	BA	01B4	C18	BA	01B4	D05	BA	01B5	C01	BA	01B5	F02	BA	01B6	A16	BA		
CR	01A7	A08	BA	01A7	E13	BA	01B7	C10	BA	02A2	A07	CM	02A2	A11	CM	02A1	C10	MT	01A4	C08	PF	01A4	C09	PF		
CRYG	01A7	A06	BA	01A8	C03	BA	01B3	F17	BA	01B4	A26	BA														
CRZT	01A3	D19	BA	01B1	B23	BA	01B1	C22	BA	01B2	B05	BA	01B3	F08	BA	01B4	D26	BA	01B4	F17	BA	01B6	C05	BA		
CRZV	01A8	B14	BA	01A8	B17	BA	01B1	A05	BA	01B1	B21	BA	01B2	D10	BA	01B3	E19	BA	01B4	B17	BA	01B4	E08	BA		
CW	01A6	A09	PF	01A6	A10	PF	01B1	F23	BA	01B3	A09	BA	01B3	D13	BA	01B4	A20	BA	01B4	A22	BA	01B6	E20	BA		
CY	01A6	B14	BA	01A6	C10	BA	01B1	A11	BA	01B1	C12	BA	01B1	C13	BA	01B3	D20	BA	01B5	E10	BA	01A6	F11	BA		
DAB	01B3	A05	BA																							
DAZ	02B3	E23	M2																							
DBZ	02B2	C05	M6	02B2	C08	M6	02B2	C09	MD	02B2	D10	M6														
DCK	02B2	C04	BA	02B2	C07	BA																				
DEF	02B4	B10	MD	02B4	B09	MD	02B3	F17	MD	02B3	C12	MD	02B3	A14	MD											
DEG	02B4	A11	MD	02A1	C22	MET																				
DEJ	02B3	B20	M4																							
DFJ	02B2	B08	MD	02B2	B17	MD	02B4	C13	MD	02B4	C10	MD	02B4	B14	MD	02B4	A17	MD	02B3	F09	MD	02A1	B23	MT		
DFQ	02B2	B09	M6	02B2	A18	MD	02B2	C13	MD	02B2	C23	MD	02B3	F21	MD	02B3	D18	MD								
DFR	02B2	A11	MD	02B2	A19	MD	02B2	B12	MD	02B4	C15	MD	02B4	C08	MD	02B3	F14	MD	02B3	F13	MD	02B3	E20	MD		
DGP	01B3	A19	BA	01B3	A22	BA	01B3	B05	BA	01B3	B12	BA	01B3	B14	BA	01B3	B15	BA	01B3	B16	BA					
DGQ	01B3	A18	BA	01B3	B17	BA	01B3	B18	BA	01B3	B19	BA	01B3	B20	BA	01B3	B21	BA	01B3	B23	BA	01B3	C10	BA		

Figure 6. Card Substitution List (Part 2 of 5)

SMS CARD SUBSTITUTION LIST

CARD TYPE	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI
DGS	02B2	A07	MD	02B2	A05	MD	02B2	A04	MD	02B2	A03	MD	02B3	A04	MD	02B3	B03	MD	02B3	B04	MD	02B4	C04	MD
DGT	02B3	B06	MD	02B3	B13	MD	02B3	B16	MD	02B3	C15	MD	02B3	F20	MD	02B4	A14	MD	02B4	D24	MD	02B2	A17	MD
DGU	02B3	C20	M3	02B3	E06	MD	02B3	C16	MD	02B3	B15	MD	02B2	A12	MD	02B2	A20	MD	02B2	B06	MD	02B2	C11	MD
DGV	02B2	B20	MD	02B3	C14	MD	02B3	E11	MD	02B2	B15	MD	02B3	F15	MD	02B3	D19	MD	02B3	C17	MD	02B3	A15	MD
DGW	02B3	D20	M2	02B3	A16	MD	02B2	A06	MD	02B2	C10	MD												
DGX	02B3	E07	M3	02B3	B08	M6	02B4	A15	MD	02B3	E14	MD	02B3	E09	MD	02B3	E08	MD	02B3	D05	MD	02B3	B14	MD
DGY	02B3	A08	M3	02B3	E10	M3	02B3	E04	MD	02B3	D10	M6	02B3	C10	M6	02B3	F08	MD	02B3	E15	MD	02B2	B11	MD
DGZ	02B2	B22	MD	02B3	D11	MD	02B4	D23	MD	02B4	C25	MD	02B4	B18	MD	02B3	B09	MD	02B2	A10	MD	02B2	A15	MD
DHA	02B3	B07	M3	02B3	D03	M6	02B3	A10	M6	02B3	C11	MD	02B3	F07	MD	02B3	A17	M2						
DHB	02B3	D04	MD	02B3	D16	MD	02B4	A18	MD	02B2	B10	MD	02B2	C22	MD	02B2	D12	MD	02B3	B10	MD	02B3	A12	MD
DHC	02B3	F10	MD	02B4	B07	MD	02B4	C11	MD	02B4	C17	MD	02B3	C13	MD	02B3	C24	MD	02B2	B14	MD	02B2	D11	MD
DHD	02B4	E21	MD	02B3	E19	MD	02B4	A10	MD															
DHE	02B3	F04	MD	02B3	F03	MD	02B3	F05	MD	02B3	F06	MD	02B3	F02	MD									
DHF	02B3	C09	MD	02B3	E18	MD	02B4	C21	MD	02B3	F18	MD	02B4	C22	MD	02B4	C23	MD	02B3	C07	MD	02B3	C05	MD
DHG	02B4	B24	MD	02B4	B25	MD	02B4	B26	MD	02B4	B20	MD	02B4	B21	MD	02B4	B22	MD	02B4	B23	MD			
DHH	02B4	B06	MD	02B4	B11	MD	02B4	B13	MD	02B4	B17	MD												
DHJ	02B4	B08	MD	02B4	B15	MD	02B4	A21	MD	02B4	A25	MD												
DHK	02B4	C05	MD	02B4	C07	MD	02B4	C18	MD	02B4	C16	MD	02B4	C14	MD	02B4	C12	MD	02B4	C09	MD			
DKA	01A1	F04	BA	01A1	F05	BA	01A1	F07	BA	01A1	F08	BA												
EY	02B2	A24	M6	02B2	C24	M6	02A1	A22	M6	02A1	A23	M6												
FP	01A4	C10	PF	01A4	C13	PF	01A4	C16	PF	01A4	C19	PF												
FT	01A5	A07	PF																					
FW	01A4	A15	PF	01A4	A16	PF	01A4	A17	PF	01A4	A18	PF	01A4	A19	PF	01A4	A20	PF	01A4	A21	PF	01A4	A22	PF
GJ	02A8	C18	INQ	01B1	C23	BA	01B1	F15	BA	02A1	D12	MT	01A6	A12	PF	01A6	F12	PF	02A8	D05	RAM	02A8	E08	RAM
GK	02B2	B23	M6	02B2	B24	M6																		
HN	01A4	C11	PF	01A4	C12	PF	01A4	C14	PF	01A4	C15	PF	01A4	C17	PF	01A4	C18	PF	01A4	C20	PF	01A4	C21	PF
JB	02B3	A11	M1																					
JFVA	01B3	A04	8M																					
JFVN	01B3	C04	BA	01B3	C13	BA	01B3	F13	BA	02B6	F06	IN												
JFVP	01A3	A03	BA	01A3	A06	BA	01A3	A09	BA	01A3	A12	BA	01B4	C08	BA	01A6	D11	PF						

Figure 6. Card Substitution List (Part 3 of 5)

SMS CARD SUBSTITUTION LIST

CARD TYPE	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI
JG	01A5	B10	PF	01A5	B11	PF	01A5	B12	PF	01A5	E04	PF									
JGVV	01B3	D25	BA	01B3	E08	BA	01B3	E10	BA	01A5	B16	PF	01A5	B03	PF						
JGWW	01A7	A20	BA	01B5	F25	BA	01A6	C13	BA												
JH	01A3	E09	BA	01A3	E17	BA	01A3	E18	BA	01A3	E20	BA	01A5	E19	PF	01A6	B02	PF			
JHVU	01B5	E24	BA	01A5	B13	PF															
JHWV	01A5	B15	PF	01A6	B06	PF	01A6	C18	BA	01A6	E05	PF									
JJVA	01A3	E21	BA	01A3	D18	BA															
JJVN	01A3	F17	BA	01B3	A23	BA	01B3	E21	BA	01B3	E23	BA	01B3	E22	BA						
JJVP	01A3	E19	BA	01A4	D21	PF	01A5	B06	PF	01A5	B09	PF	01A5	D15	PF						
JLVB	01A3	C16	BA	01A3	C18	BA	01A7	B18	BA	01B2	B11	BA	01B3	C05	BA	01B4	B22	BA	01B6	D19	BA	01B7	C21	BA
JN	01B1	F22	BA	01B3	C24	BA	01A6	E14	PF	01A6	E15	PF	01A6	E16	PF						
JZ	01B1	E23	BA	01B1	F21	BA	01B3	D26	BA	01B3	E13	BA	01B4	A06	BA	01A6	D04	BA	01A6	F14	BA	01A6	F15	BA
KA	01A3	C20	BA	01A7	F06	BA	01A8	C23	BA	01B1	A04	BA	01B1	B04	BA	01B1	C04	BA	01B3	C14	BA	01B4	E20	BA
NB	02A1	D11	MT	02A1	D13	MT	02A1	D14	MT	01A6	A04	BA									
NC	01B1	C17	BA	01B1	D14	BA	01B1	E21	BA	01B1	E24	BA	01B1	F07	BA	01B1	F12	BA	01A6	A05	BA			
NGTF	01B1	D04	BA	01B1	D05	BA	01B1	E04	BA	01B1	E05	BA	01B1	F05	BA	01A5	F09	DS	01A5	F11	DS	01A5	F13	DS
NGXX	01B4	C05	BA	01B4	C06	BA	01B4	F06	BA	01B4	F07	BA									
NT	01A6	A23	BA																		
NU	01B5	E25	BA	01B1	A09	BA	01B2	A23	BA	01B4	B26	BA	01A5	B08	PF						
NW	01A2	A03	BA	01A2	A06	BA	01A2	A09	BA	01A2	A12	BA	01A2	A21	BA	01A2	A22	BA	02A1	D19	MT			
PP	01A3	B03	BA	01A3	B04	BA	01A7	A04	BA	01A7	B07	BA	01B2	B24	BA	01B3	A20	BA	01B4	A07	BA	01B6	E19	BA
PQ	01A3	A02	BA	01A3	A05	BA	01A3	A11	BA	01A7	B16	BA	01A8	C10	BA	01B2	B12	BA	01B3	A13	BA	01B7	A07	BA
QC	01B1	F25	BA	01B4	A04	BA	01B4	F08	BA	01A5	F18	DS									
TAB	02B2	D04	M3	02B2	D05	M3	02B2	D06	M3	02B2	D07	M6	02B2	D08	M6	02A1	A21	M3	02A1	B21	M3			
TBG	02B3	D23	M3																		
TBQ	02B3	D22	M3																		
TBR	02B3	F22	M4																		
TBS	02B3	E22	M2																		
TBV	02B3	F23	M5																		

Figure 6. Card Substitution List (Part 4 of 5)

SMS CARD SUBSTITUTION LIST																								
CARD TYPE	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI	LOCATION	TEST POINT	MFI
TCK	02B2	C03	M3	02B2	D09	M3																		
TDB	02B2	B03	M3	02B2	B04	M3	02B2	B05	M3															
TDC	02B3	B11	M2																					
TDD	02B3	A22	M3																					
TDE	02B3	B22	M2																					
TDF	02B3	A23	M3																					
TDG	02B3	C22	M4																					
TDH	02B3	B23	M2																					
TDK	02B3	C23	M4																					
WL	01A4	C01	PF	01A4	C02	PF	01A4	C03	PF	01A4	C04	PF	01A4	C05	PF	01A4	C06	PF						
YBY	02B4	F05	MD	02B4	F07	MD	02B4	F09	MD	02B4	F12	MD	02B4	F14	MD									
YCB	02B4	E11	MD																					
YCC	02B4	D15	MD	02B4	D16	MD	02B4	D17	MD	02B4	D18	MD	02B4	D12	MD	02B4	D13	MD						

Figure 6. Card Substitution List (Part 5 of 5)

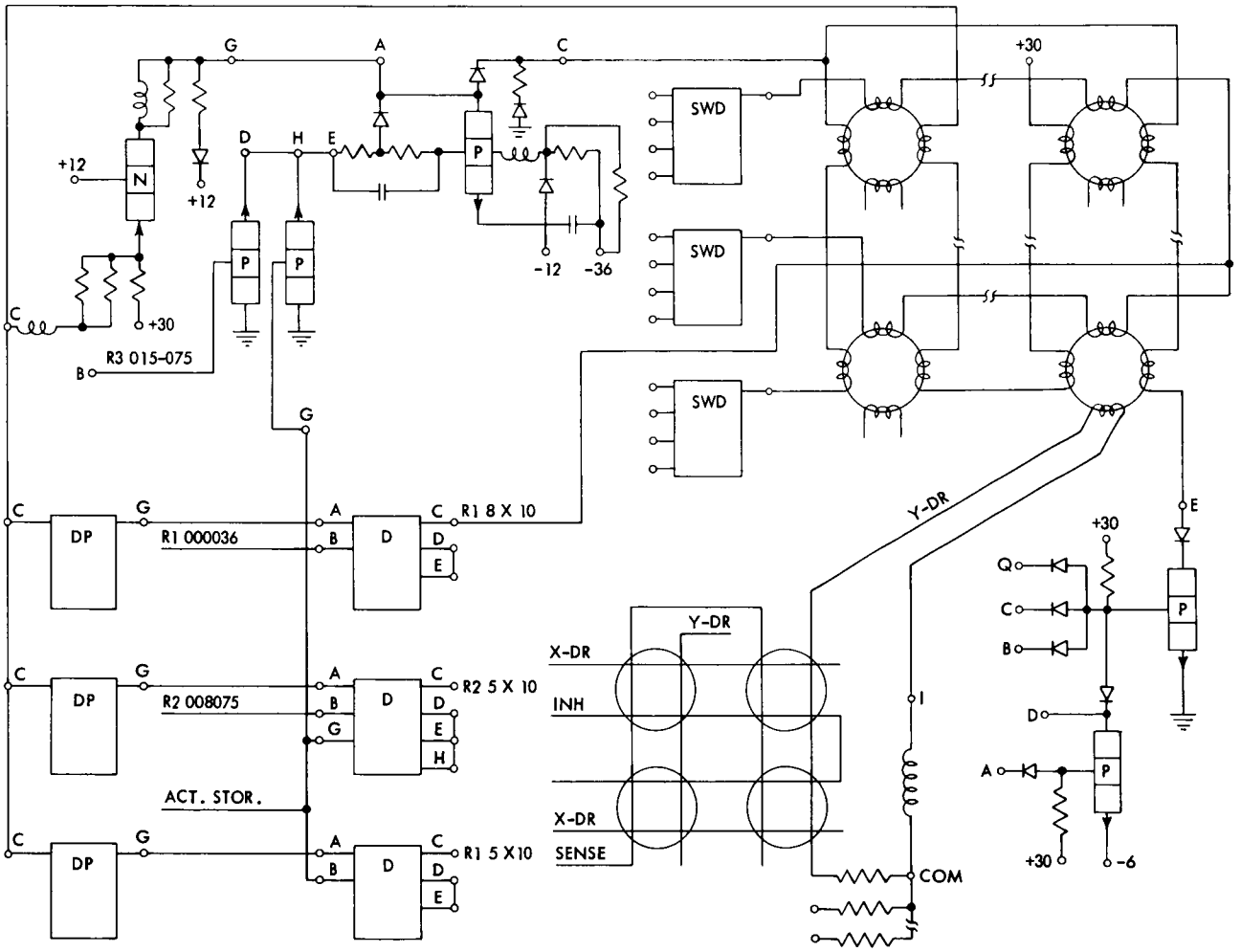


Figure 7. Core Composite

Scheduled Maintenance

Scheduled maintenance is to make the most possible machine time available to the customer. This includes only procedures necessary for continuous, satisfactory machine operation and procedures designed to reveal potential troubles. Do not disassemble or adjust satisfactorily operating units; this consumes time and gains nothing – it may even cause trouble. When performing scheduled maintenance, always check with the customer about machine performance. His comments may help spot intermittent or potential troubles.

Visual Inspection

The first step in scheduled maintenance is visual inspection. Look for corrosion, loose wires and pins, burned contact points, need for lubrication, badly worn parts, loose screws, and dirt. Many potential troubles are spotted visually and corrective action can be taken before machine failure. Make visual inspection a continuous operation when you are working around the IBM 1401 Data Processing System (Figure 1).

Installation Procedures

System Installation Procedures

Before installing the 1401, check all material against the shipping check-off list that is contained in the system installation parts package.

Refer to Figures 8, 9 and 10 for the number and types of cables for installing the 1401 system. The 1401 installation procedures are included with the 1401 Automated Logic Diagrams (ALD's).

Sales Feature Installation Procedures

PREREQUISITE B/M'S

1. Prerequisite requirements are analyzed by the plant and are included in the MES package.
2. Any gate shipped with sales changes are at the latest E. C. level, and the backpanel wiring includes the portion of the prerequisite changes affecting that gate.
3. It is not possible to install prerequisites in advance of the feature installation on changes requiring an existing gate replacement. This does not apply to features that add a gate to a dummy location.
4. If prerequisites are to be installed in increments, ensure that all wiring changes are made for the B/M's to be installed at that time.

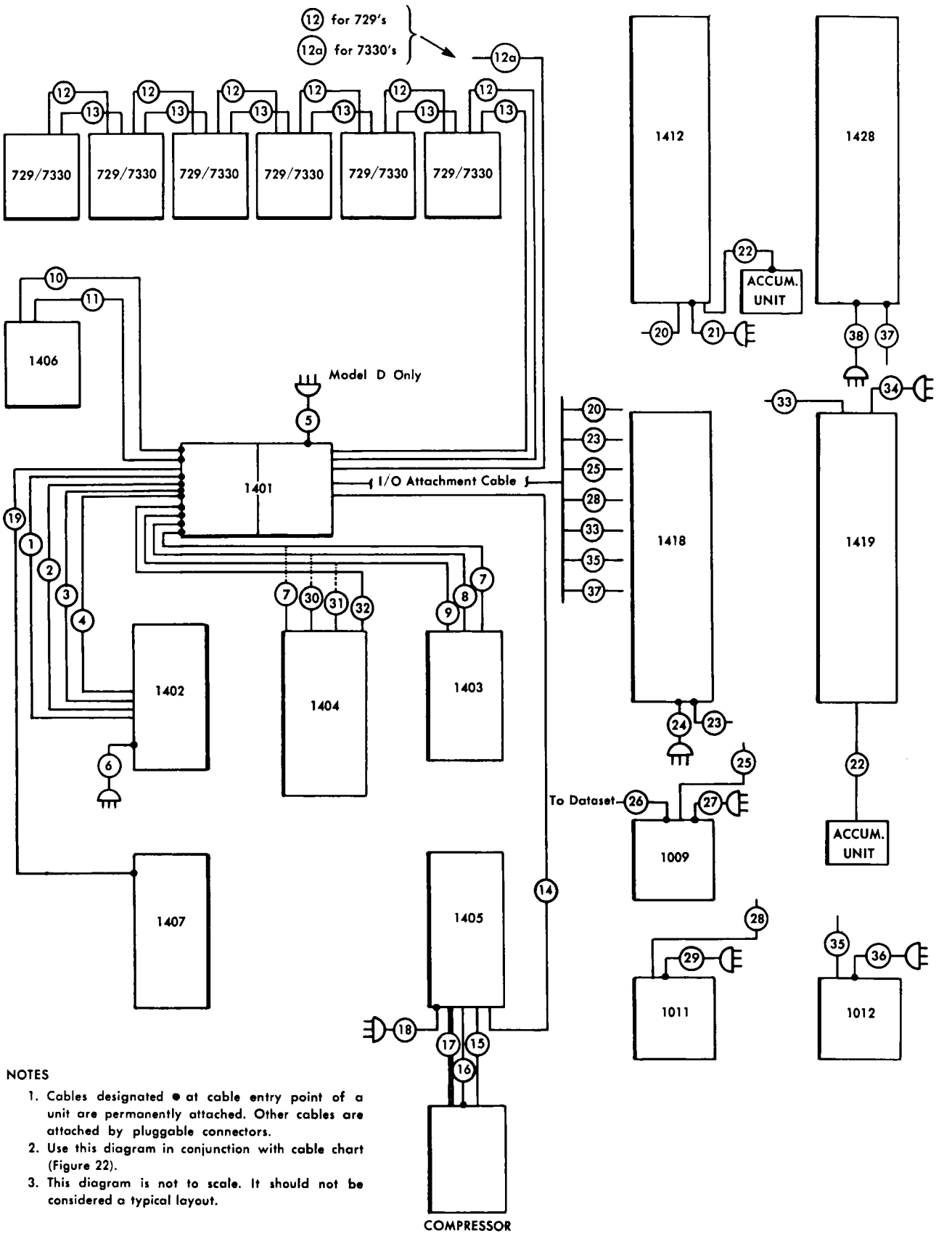
BEFORE INSTALLATION

1. Make certain all necessary parts have been received. Open all boxes to make certain they contain the correct parts.
2. Ensure that all special tools required are available. On installations requiring the addition of a gate, a 250-watt soldering iron, preferably with a wide tip, is necessary for soldering voltage leads to the laminar bus.

DURING INSTALLATION

1. Refer to 1401 MFI terminology when installing additional SMS cards.
2. The E. C. level of wired chassis may not always match the E. C. level of the index. This can happen if engineering changes affect the logics, but not the chassis, or vice versa.
3. To clarify cable routing to the interframe connectors 02A0 and 02A9, each cable is labeled *Frame Route I* or *Frame Route II*. Frame Route I refers to the outer sides (front and rear) of the interframe connectors. Frame Route II refers to the inner sides of the interframe connectors.

   When plugging new cables into the interframe connectors, start from the furthest point away from you so that the identification decals are not obscured. Interframe connectors can be loosened and turned for greater accessibility. The front interframe connector is 02A0; the rear interframe connector is 02A9. Refer to *1401 Service Aid CEM* for further interframe connector identification.
4. Where soldering of the lower laminar bus is required, the holding screw can be removed and the bus turned to facilitate soldering.
5. If paddle connectors must be added to 01A2, the cable trough can be unhooked from the center frame member and bent down to provide access to the socket.
6. Refer to the tie-down list in the logics (page 42. 40. 10) when installing features to ensure that all tie-down removals and additions are complete.



NOTES

1. Cables designated ● at cable entry point of a unit are permanently attached. Other cables are attached by pluggable connectors.
2. Use this diagram in conjunction with cable chart (Figure 22).
3. This diagram is not to scale. It should not be considered a typical layout.

Figure 8. Cable Diagram

CONNECTING UNITS	KEY NO.	FUNCTION	DIAM.	AVAILABLE LENGTHS	NOTES
1401 — 1402	1	Signal	1¼"	11', 15', 18'	1402 not available on Model D
1401 — 1402	2	Signal	1¼"	11', 15', 18'	
1401 — 1402	3	Power	1¼"	11', 15', 18'	
1401 — 1402	4	Power	1½"	11', 15', 18'	
1401 — Power Receptacle	5	Power	1"	14'	Model D only
1402 — Power Receptacle	6	Power	¾"	14'	Models A, B, F (Card)
1402 — Power Receptacle	6	Power	1"	14'	Models C, E, F (Tape)
1401 — 1403/1404	7	Signal	1⁹⁄₁₆"	13', 16', 21'	Cable lengths are for 1401 Models B, C, D, E and F. Cables for Model A are 3' shorter (10', 13', 18'). See note below.*
1401 — 1403	8	Signal	1⁹⁄₁₆"	13', 16', 21'	
1401 — 1403	9	Power	⅞"	13', 16', 21'	
1401 — 1406	10	Signal	1¼"	10'	
1401 — 1406	11	Power	1¼"	10'	
1401 — 729	12	Signal	1⁷⁄₁₆"	100' max.	Length is total from 1401 to first 729 (7330) and to each additional 729 (7330). Both cables 12 and 12a are used when 729's and 7330's are intermixed.
1401 — 7330	12a	Signal	1⁷⁄₁₆"	100' max.	
1401 — 729 (7330)	13	Power	1⁵⁄₁₆"	80' max.	
1401 — 1405	14	Signal	1⁵⁄₁₆"	40' max.	
1405 — Compressor	15	Signal	½"	40' max.	
1405 — Compressor	16	Power	¾"	40' max.	
1405 — Compressor	17	Air Hose	⅞"	40' max.	
1405 — Power Receptacle	18	Power	⅝"	14'	
1401 — 1407	19	Signal/Power	1¾₆"	10'	
1401 — 1412	20	Signal	1½"	25' max.	Connected to I/O Attachment Receptacle on 1401**
1412 — Power Receptacle	21	Power	¾"	10'	
1412 — Accumulator Unit	22	Signal/Power	⅝"	5'	Also connects 1419 to Accumulator Unit.
1401 — 1418	23	Signal	1⁹⁄₁₆"	25' max.	Connected to I/O Attachment Receptacle on 1401**
1418 — Power Receptacle	24	Power	1¾₆"	15'	
1401 — 1009	25	Signal	1"	15'	Connected to I/O Attachment Receptacle on 1401**
1009 — Dataset	26	Signal	⅜"	15'	
1009 — Power Receptacle	27	Power	⅜"	15'	
1401 — 1011	28	Signal	1"	80' max.	Connected to I/O Attachment Receptacle on 1401**
1011 — Power Receptacle	29	Power	½"	14'	
1401 — 1404	30	Signal	1⁹⁄₁₆"	13', 16', 21'	
1401 — 1404	31	Power	1⅜"	13', 16', 21'	
1401 — 1404	32	Signal	¾"	13', 16', 21'	Required only when 1404 is equipped with Comparing feature.
1401 — 1419	33	Signal	1½"	40' max.	Connected to I/O Attachment Receptacle on 1401**
1419 — Power Receptacle	34	Power	¾"	6'	
1401 — 1012	35	Signal	1"	80' max.	Connected to I/O Attachment Receptacle on 1401**
1012 — Power Receptacle	36	Power	½"	14'	
1401 — 1428	37	Signal	1⁹⁄₁₆"	25' max.	Connected to I/O Attachment Receptacle on 1401**
1418 — Power Receptacle	38	Power	1¾₆"	15'	

*For all models of 1401 prior to machine serial number 1401-20890, cables numbered 7, 8, and 9 are 8', 11', and 16' long, and are measured from a different raised-floor cutout (see Figure 4).

**Only one of these units can be connected at a time to the I/O Attachment Receptacle.

Use this chart in conjunction with Cable Diagram (Figure 21).

Figure 9. Cable Requirements

UNIT	VOLTAGE	KVA	SERVICE AMPS.	PLUG TYPE OR EQUIV.*	NOTES
Model A System	208 or 230 volts 3ϕ-60 cycle	3.2	30	R & S #3760	Power from 1402. Includes 1401 A, 1402 and 1403.
Model B System	208 or 230 volts 3ϕ-60 cycle	4.0**	30	R & S #3760	Power from 1402. Includes 1401 B, 1402 and 1403/1404.
Models C & E Systems	208 or 230 volts 3ϕ-60 cycle	4.5**	60	R & S #SC7328	Power from 1402. Includes 1401 C and E, 1402 and 1403/1404.
Model D System	208 or 230 volts 3ϕ-60 cycle	3.7	60	R & S #SC7328	Includes 1401 D and 1403.
Model F (Card System)	208 or 230 volts 3ϕ-60 cycle	4.6**	30	R & S #3760	Power from 1402. Includes 1401 F, 1402 and 1403/1404.
Model F (Tape System)	208 or 230 volts 3ϕ-60 cycle	4.6**	60	R & S #SC7328	Power from 1402. Includes 1401 F, 1402 and 1403/1404.
1406 Models 1, 2, 3	------	0.4	—	------	Power from 1401 unit. Add KVA to system KVA.
729 Models II, IV, V	------	1.6	—	------	Power from 1401 unit. Add KVA for each 729 to system KVA.
7330	------	1.1	—	------	Power from 1401 unit. Add KVA for each 7330 to system KVA.
1405 Models 1, 2	208 or 230 volts 3ϕ-60 cycle	5.0	30	R & S #3760	
Compressor	------	4.0	—	------	Power from 1405 unit. Add KVA to 1405 KVA.
1407	------	0.2	—	------	Power from 1401 unit. Add KVA to system KVA.
1412 Model 1	208 or 230 volts 1ϕ-60 cycle	2.7	30	R & S #3750	
1419 Model 1	208 or 230 volts 1ϕ-60 cycle	3.3	30	R & S #3750	
Accumulator Unit	------	—	—	------	Power from 1412 or 1419.
1418 Models 1, 2	208 or 230 volts 3ϕ-60 cycle	4.6	30	R & S #3760	
1428 Models 1, 2	208 or 230 volts 3ϕ-60 cycle	4.6	30	R & S #3760	
1009	115 volts 1ϕ-60 cycle	0.3	20	P & S #5267	208/230 volts 1ϕ optional — uses R & S #3720 plug.
1011	208 or 230 volts 1ϕ-60 cycle	1.8	15	R & S #3720	
1012	208 or 230 volts 1ϕ-60 cycle	1.8	15	R & S #3720	

*These plug types are used on the power cords attached to the IBM units. The customer provides power receptacles to match the plugs.

**Add 0.7 KVA when 1404 is used instead of 1403.

R & S — Russell and Stoll
P & S — Pass and Seymour

Figure 10. Electrical Requirements

7. When an unplugged chassis is received with a change, the cards and card guides from the old chassis are used on the new chassis. Refer to the new plug chart(s) received with the change for correct plugging. Figure 11 illustrates the proper method for removal of the card guide.
8. When a new chassis is sent to replace an existing chassis on the 1401, it is customary to completely replace the logics for the old chassis. However, when print storage is added in the field, gate 01A5 retains the DS Index and all pages are listed on it.

   The result is two indexes, plug charts, etc. in the logics for gate 01A5. When card plugging is checked, the DS and PF plug charts must be used.
9. In installations such as print storage, remove and discard certain cables. In this case, it is more practical to cut the cables rather than attempt to slip the edge connectors through the cable lacing.

BACKPANEL WIRING RULES

1. There should not be more than two wires on any backpanel pin on the 1401 except under the following conditions:
   a. RPQ's. (Special circuits called out on feature designated by B/M 880xxx or 299xxx).
   b. Remote recycle-device attachment circuitry cable.
   c. Tie-downs (white wires).
2. If a sales feature (B/M 494xxx or 495xxx) calls out a field bill of material (485xxx or 486xxx) as a prerequisite, disregard the *Machines Affected* section of the prerequisite field bill of material.
3. On all gates affected by the change, check all cards in the gate against the plug chart. Missing or incorrect cards can cause hard-to-analyze troubles after the installation of the change.

AFTER INSTALLATION

Ensure that machine records are updated to indicate which prerequisites and features are installed. Return B/M installation report cards to the appropriate plant.

MACHINE FEATURE INSTALLATIONS USING COMPOSITE "NET LIST" INSTRUCTIONS

The *Net List* set of instructions is a composite listing of all the changes necessary to install a feature. This set of instructions includes both the feature installation instructions and prerequisites required. This document is prepared on a computer and is tailored to an individual 1401.

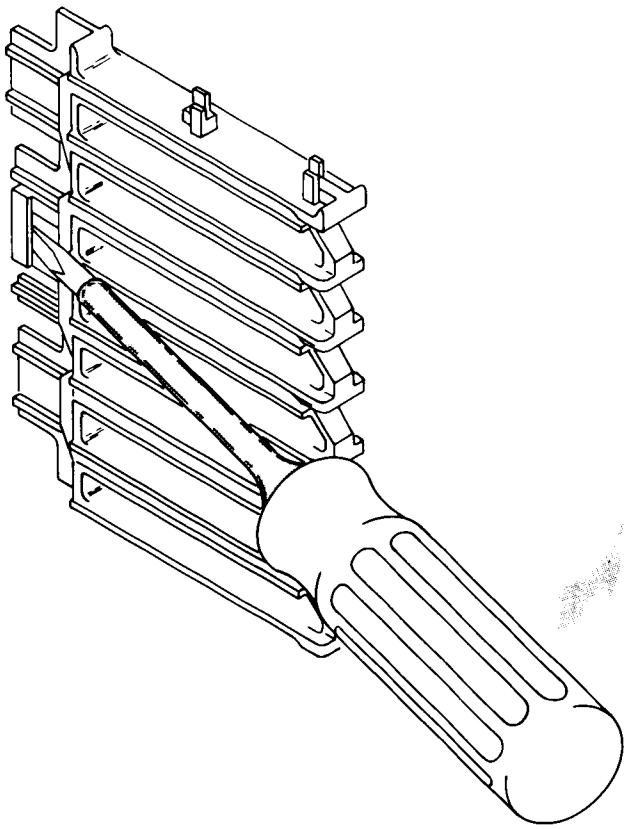


Figure 11. Card Guide Removal

Use of this program can cut installation time up to 50% because of reduction in analyzation time and duplication.

Scheduled Maintenance Procedures

The scheduled maintenance procedure for the IBM 1401 Data Processing System can be found in Figure 12.

Details that are to be performed on each item are listed in the scheduled maintenance chart. During normal inspection, perform only operations listed on the chart.

1401 DATA PROCESSING SYSTEM

CODE	UNIT OR ROUTINE	FREQ. WEEKS	OPERATION	OBSERVE
0	Blower and Filters	6	Check for clogged screens on both sides of Muffin Fans. Clean as required. See Note 2.	ALL INDICATORS REPLACE AS NECESSARY

Figure 12. Scheduled Maintenance

Troubleshooting

If the IBM 1401 Data Processing System fails to operate properly, the cause of the trouble must be found and corrected quickly to hold unproductive machine time to a minimum. Rapid and effective diagnosis depends upon thorough knowledge of machine logic and effective use of diagnostic tools available. Diagnostic programs, marginal checking, checking indicators and CE test panels are aids for troubleshooting the 1401 system.

Diagnostic Programming

The 1401 customer engineering tests are specifically designed to help the customer engineer in the field to test functional operations of the 1401 and its associated components.

These tests, when properly used, help the customer engineer to install the 1401 with a minimum of time and effort, thereby assuring efficient operation of the system before it is released to the customer.

A complete set of write-ups along with flow charts that describe the various tests are shipped with each 1401 system.

Marginal Checking

Marginal checking (MC) has two basic maintenance functions:

1. Scheduled maintenance — to increase system reliability.
2. Unscheduled maintenance — to minimize system down-time in troubleshooting for *intermittent* symptoms produced by degrading components. Marginal checking can force these into the region of solid failure.

In tube machines, marginal checking is of value in both of these functions. With the much higher reliability of solid-state machines, preventive maintenance becomes less important, and troubleshooting becomes the main purpose of marginal checking. Scheduled MC is required in order to clean up any bugs that excessively limit the MC range. This is necessary to ensure that adequate MC range will still be available when the next intermittent symptom occurs.

The marginal-checking scheme used in the 1401 system is an inherent part of the circuit design. Separate voltage busses are provided exclusively for marginal checking. Only those circuits which can benefit from marginal checking are connected to the MC bus. These connections to the MC bus are specifically designed to give each circuit approximately the same sensitivity to MC voltage variation. In every case, the MC connection to the circuit is designed so that good components cannot be damaged by the full ±3v marginal-check variation. The only possibility for component damage occurs with defective components that are already out-of-specification and on the brink of failure.

A ±3v variation on the +6M or −12M voltages will have very little effect on the steady state performance of normal circuits. Dynamically, the 3v MC shifts will cause about a 25 percent change in timing in most circuits.

The 1401 engineering specifications specify correct machine operation with a minimum variation of any marginal-check voltage by ±1.2v. This is a minimum variation. Many systems surpass this.

As soon as time permits after a new machine is installed, make a complete marginal check. Record the limits for future reference. Replace any out-of-specification cards that limit the MC range. After this, MC at two- or three-month intervals should be sufficient. If experience shows very little change in the limits, the MC interval can be increased. Make a complete MC check after installing any major machine changes.

When performing marginal checking, the combined 1401 CE diagnostic tests are to be used. These tests are arranged from the simple to the more complex operations. Refer to *Power Supplies* for a description of marginal checking.

Method of Performing Marginal Test

Note: Machines that have switches for selecting the gates to be marginal-checked have caused considerable trouble because of poor contacts. The marginal-check switches should be pushed in and left to eliminate the poor-contact problem. Future systems will eliminate these switches.

1. Select voltages to be biased by jackplug. Place the jackplug in the rest position when the marginal test is not being used.

The +6M voltage provides base bias on NPN inverters.

The −12M voltage provides base bias on PNP inverters.

The +12M voltage provides base bias on SDTDL circuits in TAU-9.

The +30M voltage provides base bias on current-source circuits for core storage by varying the +18v differential.

The remote hub provides bias to remote units. The voltage is selected at remote unit with another jackplug (Figure 13).

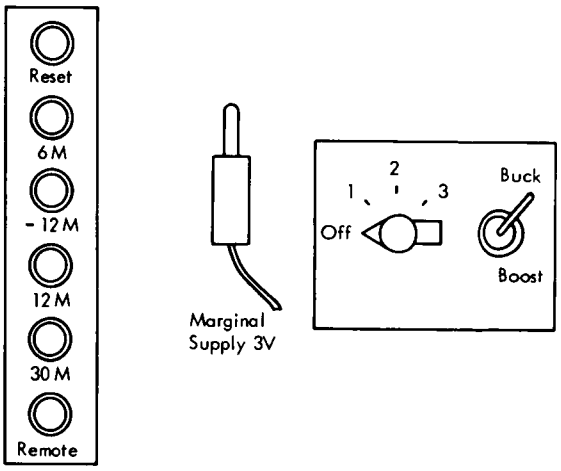


Figure 13. Marginal-Check Controls

2. Connect a meter to the supply selected with the jackplug. If the circuit breaker on the marginal 3v supply kicks out, no indication is made. The meter tells you exactly how much you are varying the supply being tested.
3. Set the buckboost switch.
4. Vary it with the Variac* switch.

VOLTAGE-LEVEL CHECKING

1. Periodic checking is recommended as a PM procedure.
2. Voltages should be exact; +12 variable is the exception.
3. Voltage should be measured at the place it is most likely to give trouble.
4. Voltage should be measured with the most accurate instrument available. A ½% dc meter is recommended.

PRECAUTIONS TO OBSERVE

1. The −12v supply is referenced to −6v. Therefore, it must be adjusted after the −6v supply.
2. The +12v fixed and variable supplies are developed from the +30v supply. Therefore, they must be adjusted after +30v.
3. Ripple on a supply can give a false meter reading.

PURPOSE OF SUPPLIES

−6v	Emitter voltage for NPN transistors.
+6v	Collector voltage for NPN transistors.
−12v	Collector voltage for PNP transistors.
+12v	Supplies base of transistors in core storage circuits.
+12v extender	Supplies the TAU-9 circuitry.
+18v differential	(+12 variable) Supplies current source circuits in core storage.
−20v	Supplies row-bit cores.
−20v filtered	Supplies bias for decode switches.
+30v	Supplies bias current for switch cores, collector voltage for decode switches.
−36v	Supplies TAU-2 circuits.

SEQUENCE FOR CHECKING VOLTAGES

+6v, −6v, and −12v for frame 1 are located in 02A4 and 02A5. Measure at gate 01B3: clock circuits and distribution.

+6v, −6v, and −12v for frame 2 are located in 02A3 and 02A6. Measure at gate 02B2 – TAU. If TAU is not on the machine, check at available optional-feature gate 02A7 or 02A8.

+30v measure at 02B2. If there is no TAU, measure at 01B3.

If there is TAU-2, measure −36 at 02B2.

−60v located in 1402. Model D location 01B4. Measure at 01B8 on −60v bus bar.

−20v located in 1402. Model D location 02A8. Measure at 01A2 A24Q.

Marginal Check Techniques

Studies have proven that marginal failures in solid-state circuitry are not all aggravated by any single marginal-check technique. Laboratory and field tests determined that base-voltage variation, the standard technique now in use, is primarily effective where failures are caused by transistor turn-on delays. Other known techniques have proved superior where intermittent failures were caused by noise, incorrect levels, or critical timing conditions.

*General Radio Corporation

When troubleshooting an intermittent failure, analyze the symptoms very carefully; note all console error lights, contents of registers, cycle lights, etc. Work with the customer's program at the start. Try inserting a branch op to define a failing loop. Often a failure that appears intermittent will fail solidly if the same data, or the same sequence of operations, is repeated.

If the problem cannot be duplicated with this approach, or with the diagnostic tests, try the marginal techniques listed here. The failure rate of most intermittent problems can be increased by one of these techniques. Branch offices already using this approach report a high degree of success.

Two cautions should be carefully noted:

1. Techniques described here are presented as troubleshooting tools *only*. Their use as preventive maintenance tools results in excessive service time and unwarranted parts replacement.
2. On any of the techniques, a difficult-to-diagnose failure, unrelated to the customer problem, may be introduced. This point can be within voltage limits specified here, particularly on older machines. If these problems cannot be resolved in a reasonable length of time, move on to another voltage or to the next technique.

   Base-voltage variation should be the first marginal technique tried. Other techniques can be applied in any convenient sequence. A detailed description of each technique follows.

BASE-VOLTAGE VARIATION

The +6M and −12M voltages supply transistors base potential throughout the 1401. The standard technique of varying these two voltages is known as *base-voltage variation*.

Vary these voltages toward their ±3.0 volt limits. Attempt to correct any failures that occur within these limits, or to the limit where the customer failure is duplicated.

Note: Some twin SMS cards, P/N 373000, will fail above ±1.2 volts bias unless capacitors announced in 1401 EC-CEM 579 are installed.

FREQUENCY VARIATION

Basic 1401 clock frequency is increased in this technique. It is most effective where failures are caused by marginal timing conditions (line delays, slow cards, etc.). Proceed as follows:

1. Set the scope as indicated in Figure 14. Display the output of the ±0 hub, located on the CE console with the machine in static condition. The output should appear as shown in Figure 14A.

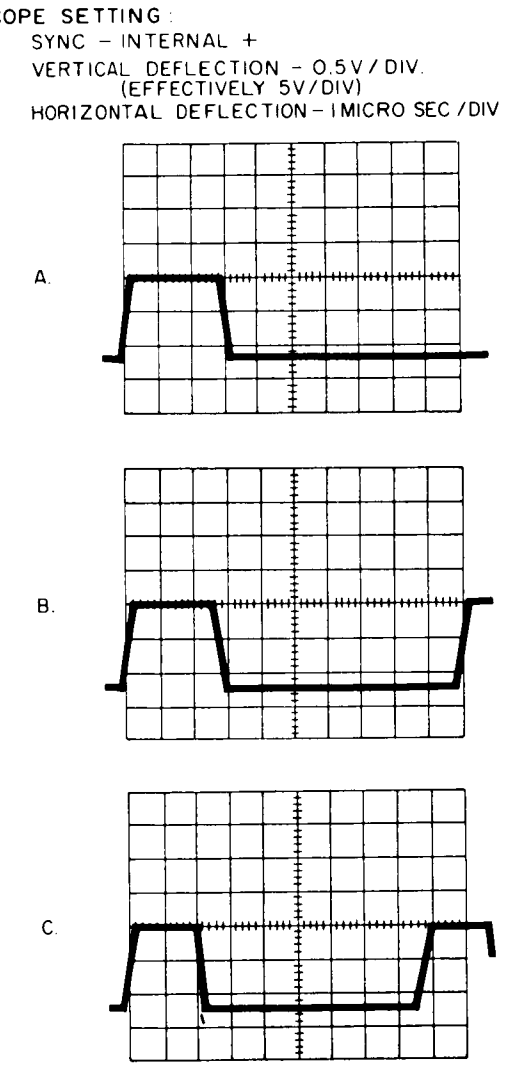


Figure 14. Clock Frequency Variation

2. By adjusting the time-per-division calibration knob counterclockwise, bring the positive-going portion of the next pulse onto the right side of the scope and line it up with the last vertical line on the scope face (Figure 14B).
3. Turn the power off and remove SMS card (RK −), P/N 371788, in location 01B3 A 26. Install variable oscillator SMS card, P/N 372561.
4. Turn the power on. Without changing the scope, adjust the pot on the variable oscillator card so that the scope picture is again identical to Figure 14B.
5. Run diagnostic tests. Vary the oscillator slowly so that the leading edge of the second pulse moves from the rightmost vertical line to a point 1⅓ horizontal divisions to the left (Figure 14C). This effectively increases the clock frequency from 11.5 to 10.0 microseconds.

CAUTION: The leading edge of the pulse should not be moved to the right of the last vertical line on non-print buffered systems. This *decreased* frequency causes hammer-driver fuses to blow on these systems when a print op is performed.

6. Troubleshoot all failures that occur within this range.
7. When limits have been met, drop the power and replace the oscillator card with a standard one.
8. On machines equipped with a print buffer, if machine failures are associated with a print operation:
   a. Rather than replace the basic block oscillator, observe the +U RO Time 000-030 pulse at 01A5 B14N, with the scope set as indicated in Figure 14.
   b. Adjust the scope as in Step 2, observing Figures 14A and B.
   c. Remove buffer clock oscillator SMS card (FT–), P/N 371405, from location 01A5 A07. Install variable oscillator SMS card, P/N 372561, using SMS card extender, P/N 451075.
   d. Follow the procedures as in Steps 4, 5, 6, and 7.

Note: Do not *decrease* frequency beyond 11.5 microseconds when printing.

MECHANICAL VIBRATION

Vibrating SMS cards is effective in showing failures caused by SMS socket contact resistance, cracked land patterns, or poor component connections.

With the palms up, run the backs of your fingers down the card rows, from top to bottom, while diagnostic tests are running. Vibrate the cards on any gate that may be associated with the machine problem.

CAUTION: Component damage can result from excessive vibration. If adjacent SMS cards contact, serious machine damage will result. To determine how hard to vibrate, a good rule to follow is: "If the vibration hurts your finger, slow down!" Vibrate the cards on all gates that may be associated with the failure.

COLLECTOR VOLTAGE VARIATION

This technique varies voltages (+6 and —12) that supply transistor collector potential. It is particularly effective in showing failures caused by electrical noise or bad levels.

From #22 gage (or larger) wire, make a jumper about 18 inches long. Solder spade clips to both ends. Proceed as follows:

1. Analyze the failure to determine the possible machine operation or unit involved.

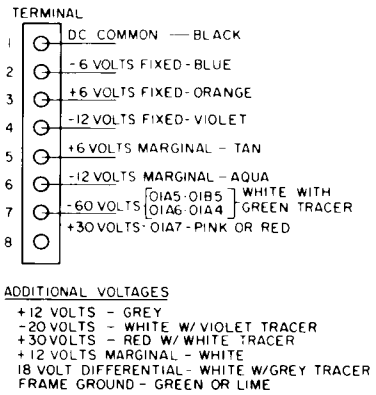


Figure 15. Voltage Terminal Block

2. Refer to the gate logic index pages in the front of Logic Book I. Select the gates containing the circuitry unique to this operation or machine function.

   As an example:

   a. Assume the failure appears to be a carriage problem. Logic indexes indicate Gates 01A5 and 01B1 contain this circuitry.
   b. If STAR-bit pickup is occurring, Gates 01A7, 01A8 (and 02B6, 02A7 if on the system) are affected.

   Note: TAU gates and memory gate 01A1 should not be collector-biased.

3. Select one of the affected gates. Drop the power and make the following changes at gate voltage terminal block. (Refer to Figure 15 located to the left of Row A.)
   a. Disconnect the external voltage (orange) wire from the +6v terminal and connect one end of the jumper to this terminal.

   CAUTION: Be certain the orange wire is positioned so that it does not short to frame, or the other connections.

   b. Connect the other end of the jumper to the +6M terminal (the terminal with the tan wire attached).

   Note: If no tan wire comes to this gate, connect the jumper to the terminal on the adjacent gate where this voltage is available.

   c. Connect a voltmeter to a +6v pin (Pin L) on the gate. Insert the marginal-voltage supply jack in the +6M hub (or set the marginal-supply switch to +6M on earlier machines).
4. For gates other than 01A4, 01A5, 01A6 and 01B5, proceed to Step 5. For Gates 01A4, 01A5, 01A6 and 01B5, disconnect —60v hammer-magnet return by

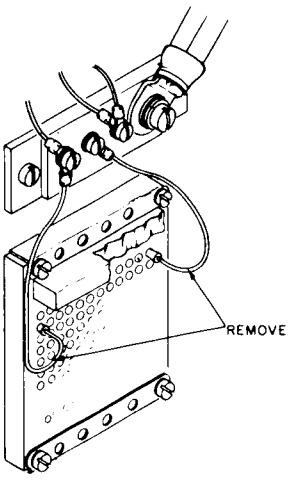


Figure 16. Relay Base Terminal Block

removing two black wires at the —60v return-relay, base-terminal block in 01B8 (Figure 16). Turn on the power. Begin by loading the print area with blanks and programming a simple print and branch loop. Observe the console-error lights and scope the output of the print-reset check latch at 01B5E01A to determine if errors occur. Now proceed to Step 6.

5. For gates other than 01A4, 01A5, 01A6 and 01B5:
   a. Turn on the power.
   b. Select the diagnostic tests applicable to failing machine function or operation.
   c. Run diagnostics and proceed to Step 6.
6. a. Vary the marginal-voltage supply. Collector voltages can be varied as much as +3.0 volts without causing machine damage. Vary the voltage to this limit in search of the trouble, if no other trouble occurs prior to this limit.

      Note: When biasing 01B7, a point is reached where all magnet drivers fire simultaneously. Do not continue to run the machine or bias beyond this point.

   b. Fix any failure that occurs before reaching the limits of 1.0v buck to 1.5v boost. If this trouble appears to be similar to the trouble, consider the machine fixed.
   c. When going beyond the limits of 1.0v buck to 1.5v boost, fix a trouble only if it appears to be the reported trouble. For future reference, it might be well to record the symptoms of failures in this area.

      Note: The trouble may appear somewhat different because the machine is undergoing a more severe test than it normally receives.
7. If customer-reported trouble has not been found, and the bias limits of the +6v on this gate have been reached:
   a. Drop the power and restore the voltage wires to normal.
   b. Disconnect the external voltage (violet) wire and connect one end of the jumper to the —12 volt terminal on the gate voltage terminal block (Figure 15). Be certain the violet wire is positioned so that it does not short to frame, or other connections.
   c. Connect the other end of the jumper to the —12v voltage terminal (the terminal with the aqua wire attached).

      Note: If no aqua wire comes to this gate, connect the jumper to the associated terminal on an adjacent gate.

   d. Connect a voltmeter to a —12v pin (Pin M) on the gate. Insert the marginal voltage-supply jack in —12M hub (set marginal check switch to —12M on early machines).
   e. Repeat Step 6.
8. If the trouble has not been found, and the —12v limits have been reached:
   a. Drop the power and restore gate voltages to normal.
   b. If other gates are involved, select one of these gates and continue, starting with Step 3.

DUAL BASE VOLTAGE VARIATION

Note: To utilize this technique, the machine must be equipped with a marginal-voltage jackplug receptacle. Obtain an additional marginal-voltage power supply. Plug the first supply into the +6M jack hub; plug the second supply into the —12 jack hub.

Vary marginal voltages ±1.5 volts separately or collectively, in any combination. Run diagnostic tests and follow this guide:

1. Set +6M to 4.5 volts; vary the —12M ±1.5 volts.
2. Set +6M to 7.5 volts; vary the —12M ±1.5 volts.
3. Set —12M to —10.5 volts, vary the + 6M ±1.5 volts.
4. Set —12M to —13.5 volts; vary the +6M ±1.5 volts.

A variable oscillator SMS card, P/N 372561, has been automatically shipped to each branch office, for use as an office tool.

Check Circuits

The following check circuits are used in the IBM 1401 Data Processing System: parity, validity, invalid address checking, and wrap-around checking.

PARITY CHECKING FOR A-REGISTER, B-REGISTER, AND INHIBIT CIRCUITS

Parity checking is accomplished by switching an even-digit and even-zone or an odd-digit and odd-zone bit combination to develop the error condition, when the bit sum is even.

The A-register error condition is gated with ACTIVATE STORAGE, NOT I-RING OP, and time 075-090.

The B-register error condition is gated with ACTIVATE STORAGE, and 045-060.

The storage parity check is gated with ACTIVATE STORAGE, NOT START OR ENTER, and 090-105.

ADDRESS VALIDITY CHECK

Address validity checking includes parity checking for a valid bit combination, and checking for a valid address.

Address parity checking is accomplished by switch ing an even-digit and odd-zone bit combination or an odd-digit and an even-zone bit combination to produce an odd-bit line on all bits combined. The absence of an odd-bit configuration signal switched with ACTIVATE STORAGE at times 015-030, 045-060, or 075-090 sets the check latch.

An invalid bit combination would show up either as a no-even or no-odd digit, or as zone-bit combination lines that indicate an error as previously stated in the section *Parity Checking for A-Register, B-Register, and Inhibit Circuits.* The invalid bit combination shows up in this manner because only valid bit combinations develop the even- and odd-digit bit-combination lines. Valid digits in the storage-address register are the digits 0 through 9.

INVALID ADDRESS CHECKING

Checking for a valid storage-register address is accomplished in a manner similar to validity checking. However, the validity of the address depends on the storage capacity of the system. Any 3-digit address, including the hundreds position zone, is valid for a 4k system. Only addresses between 0000 and 1399 are valid for systems with 1.4k storage. The invalid address is brought up when indexing to above-capacity storage.

Examination of the addresses that are involved with the 4k storage shows that there is no invalid address. The possible bit combinations of the hundreds position (zones) AB, AB, AB, and AB along with any valid digit), are all valid because they address locations between 0000 and 3999.

Close examination of the hundreds position of the invalid addresses involved with the 2k storage system (2000 to 3999) shows that they all have a B-bit in common. Because there is no B-bit output from the storage-address register on systems less than 4k storage, the B-bit will be lost and a parity check error will result.

The same invalid addresses (2000 to 3999) are detected the same way on systems with 1.4k storage. In addition, check circuits are provided to detect addresses between 1400 and 1999. This is accomplished by switching a 4-bit and an A-bit together (1400 and 1799) or an 8-bit and an A-bit together (1800 to 1999) at hundreds time, thereby detecting an invalid address.

WRAP-AROUND CHECKING

Wrap-around describes the process of modifying the highest address of a system by plus one, or the lowest address by minus one. For example, wrap-around on a 1.4k storage system would mean modifying 1399 by a plus 1 to obtain 0000, or modifying 0000 by minus 1 to obtain 1399.

If wrap-around is detected at any time other than during a storage-scan operation or a clear operation, it sets the storage-address register check latch at 075-090 time, thereby stopping the machine at the end of the next cycle.

A good analyzation of the 1401 console-error indicators, A- and B-registers and the op-register, assists in breaking down the type machine failures that have been encountered during the program routine. Figures 17, 18, and 19 act as a recall on what should happen when a specific error is encountered.

Additional charts showing which latches are affected when detecting these various errors can be found on Figures 20, 21, and 22.

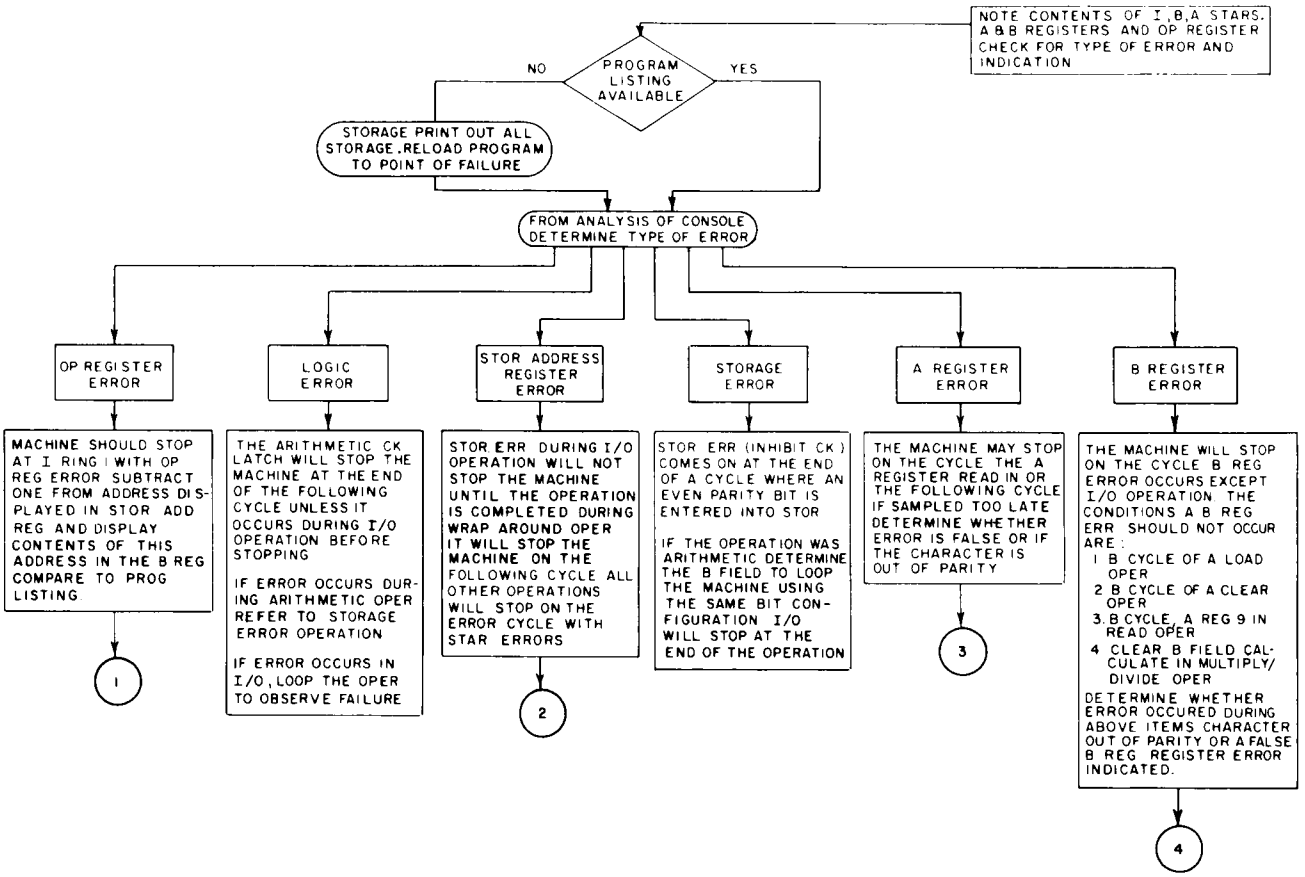


Figure 17. Analyzing Error Indicators

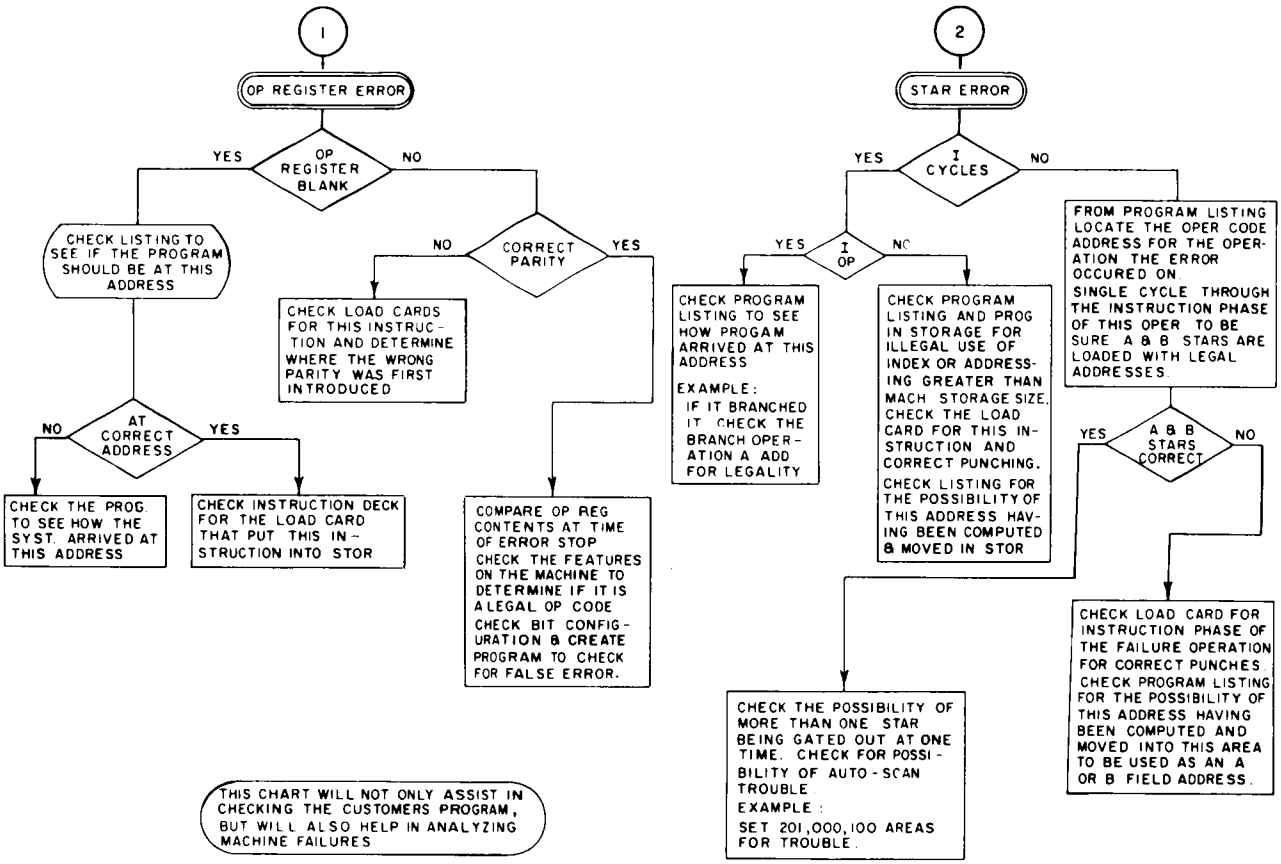


Figure 18. Op Register and STAR Analyzations

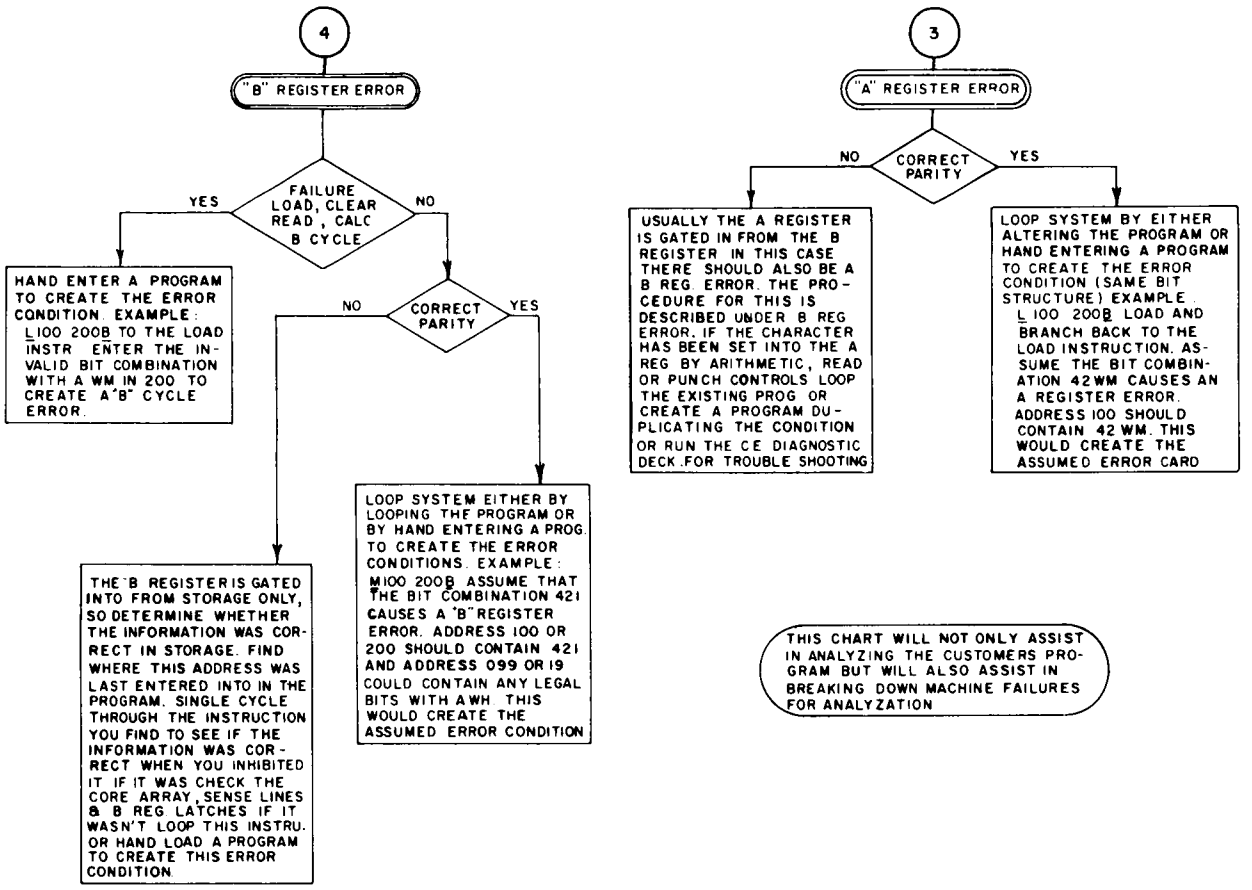


Figure 19. A- and B-Register Analyzations

UNIT	TYPE OF ERROR	LATCH INVOLVED	MACHINE STOPS (PROCESS CK STOPS "ON")	STORAGE ADR REG CONTAINS	LIGHTS ON WHEN STOPPED	RESET BY	REMARKS
A Reg 075–090	Parity	A Reg Ck Latch	End of next Cycle	Address of error +1 or -1	Process A Reg Check Reset	Check Reset Key	Contents of A Reg at the time of error may be still on display. Dependent on cycle error occurred.
B Reg 045–060	Parity	B Reg Ck Latch	End of Cycle in which error is detected	Address of Location that was read into "B" register	Process B Reg Check Reset	Check Reset Key	Contents of B Reg at the time the error is detected will remain on display in B Register.
Arith 075–090	Validity	Arith Ck Latch	End of following cycle	Normally 1 less than the location that the resultant is in (only if error occurs on A cycle eliminate)	Process Logic Ck Reset	Check Reset Key	Adr Reg will indicate one less than the location that the resultant is read into except for: 1. When the error is detected in the last cycle of the first forward scan on a recomplement operation when it will indicate the same location or 2. It will indicate one more than the location the resultant is read into on a reverse scan operation. The bit combination which causes the error will be in the storage unit and not on display under "Logic" (remember that it is in qui-binary from when checked and goes through the translator before going into storage.
Inhibit Switching 090–105	Parity	Inhibit Check Latch	End of following cycle	Dependent upon operation being performed and phase that system is in	Process Storage Ck Reset	Check Reset Key	This type error indicates that on even bit configuration has been read into storage.
Op Reg 030–060 Not I op	Validity and Parity	Op Reg Check	End of cycle in which error is detected unless I op, then 11.	Dependent upon type of operation being performed and phase	Process Op Reg Check Reset	Check Reset Key	The check latch will not turn on during I Ring Op time.
Storage Address Register 000–015 030–045 060–075	Parity and Validity	Stor Addr Reg Error Latch	End of cycle in which error is detected	Bit combination that caused error	Process Storage Address Ck Reset	Check Reset Key	The error check is made after the address is serialized. An error could be caused by a fault in serializing. (Resets and gate outs blocked.)
	Wrap Around 060–090	Stor Addr Reg Error Latch	End of following cycle	Dependent upon operation being performed and modification	Process Storage Address Key Ck Reset	Check Reset Key	Can be modified by +1 or -1. Main Star will contain 000 or highest address
							NOTE: If any of the above errors occur during an input/output operation, the system will complete the particular operation involved before stopping.

Figure 20. Process Unit Error Conditions

Unit	Error	Latch Involved	Machine Stops I/O Check Switch "On"	Lights ON When Stopped	Reset By	Remarks
Reader	Read Check	Read Check (36.14.11)	At the end of the feed cycle	Read Check (1402) Read (Process)	Check Reset Key on the 1402	Cards must be run out before check reset key becomes effective.
Reader	Validity	Validity (36.14.11)	"	Validity (1402) Read (Process)	Check Reset Key on the 1402	Cards must be run out before the check reset key is effective.
			Note: Also, if the invalid combination causes incorrect parity:			
				Storage (Process) Process (Process) Check Reset (Process)	Check Reset on the Process Unit	
Reader	Jam	Picks R:4	At the end of the feed cycle	Reader Stop (1402) Read (Process Unit)	Check Reset Key (1402)	Cards must be run out before the reset key is effective.
Punch	Punch Check	Punch Ck (36.14.11)	At the end of the feed cycle	Punch Check (1402) Punch (Process)	Check Reset Key (1402)	
Punch	Parity	Punch Stop B Reg Check	"	Punch (Process) Process (") B Reg (") Check Reset (Process)	Check Reset Key (1401)	
Punch	Jam	R-31 Punch Stop	"	Punch Stop (1402) Punch (Process)	Check Reset Key (1402)	Cards must be run out before the reset key is effective.

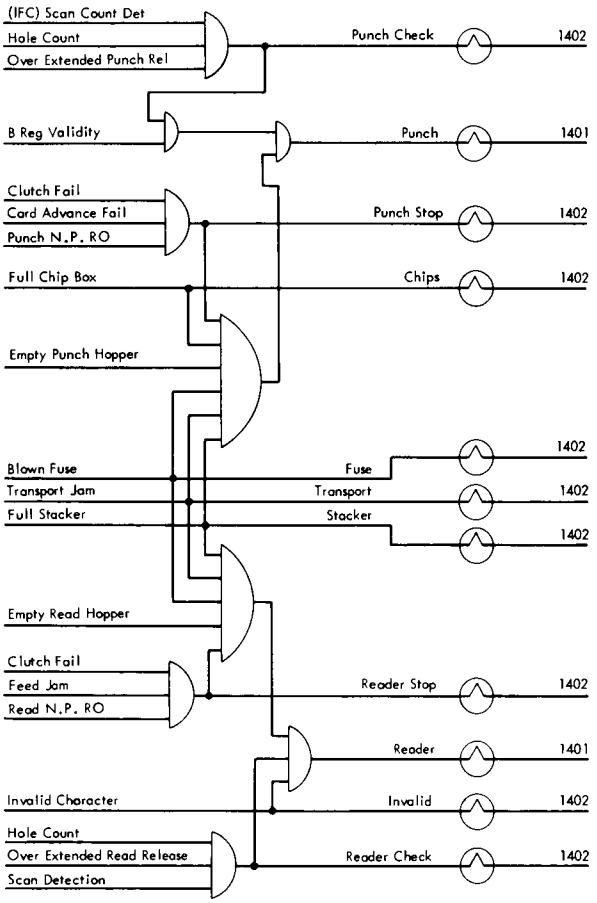


Figure 21. IBM 1402 Error Conditions

ERROR	LATCH	1401 STOPS (I/O CK STOP SWITCH ON)	LIGHTS ON		RESET BY	REMARKS
			PROCESS UNIT	PRINTER		
Parity	B Reg Check	Upon Completion of Print Operation	B Reg Process		Check Reset (Process out)	
Chain Sync	Home Error 36.37.11 Reset Ck.	"	Printer	Sync Check	Check Reset (Printer)	Sync Chk will Cause Reset Chk
Hammer Fire	Print Check 36.37.21	"	Printer	Print Check	Same	Sets Error Store Core
Print Line Complete	"	"	"	"	"	"
Chain Sync	Home Error Reset Chk					
Run Trigger Going Off During a Print Scan	Reset Chk					
Print Comp Eq & Print Line Comp on Same B Cycle	Reset Chk					
Star Error While Printing	Reset Chk					
Hammer Reset Drive Lines Not Sequencing Properly	Reset Chk					
A Reset Chk will cause a print line complete error. This is because a reset chk will block the print comp. equal sample. When scan 49 is taken, all print line complete cores will not be set and a print chk will be indicated.						

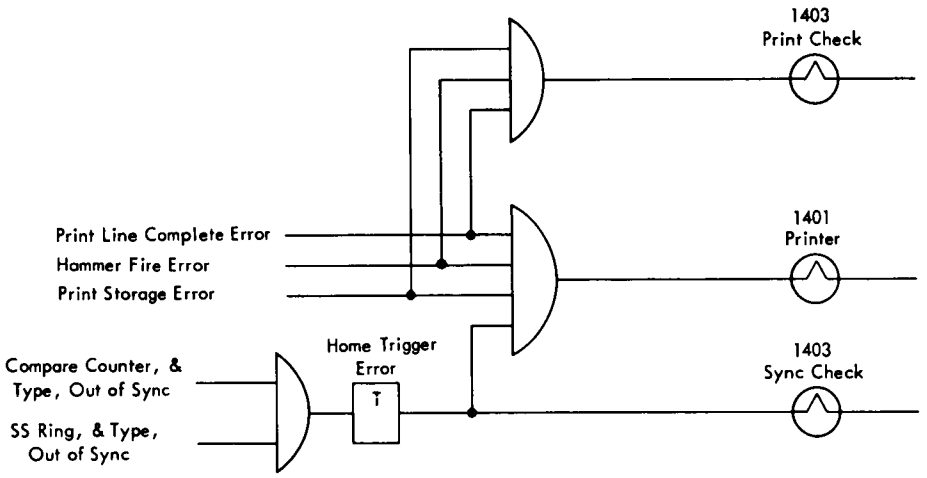


Figure 22. IBM 1403 Error Conditions

The following section contains a set of flow charts that are designed as recall diagrams for the various operation codes. Use these flow charts as a guide in determining the troublesome areas of operation.

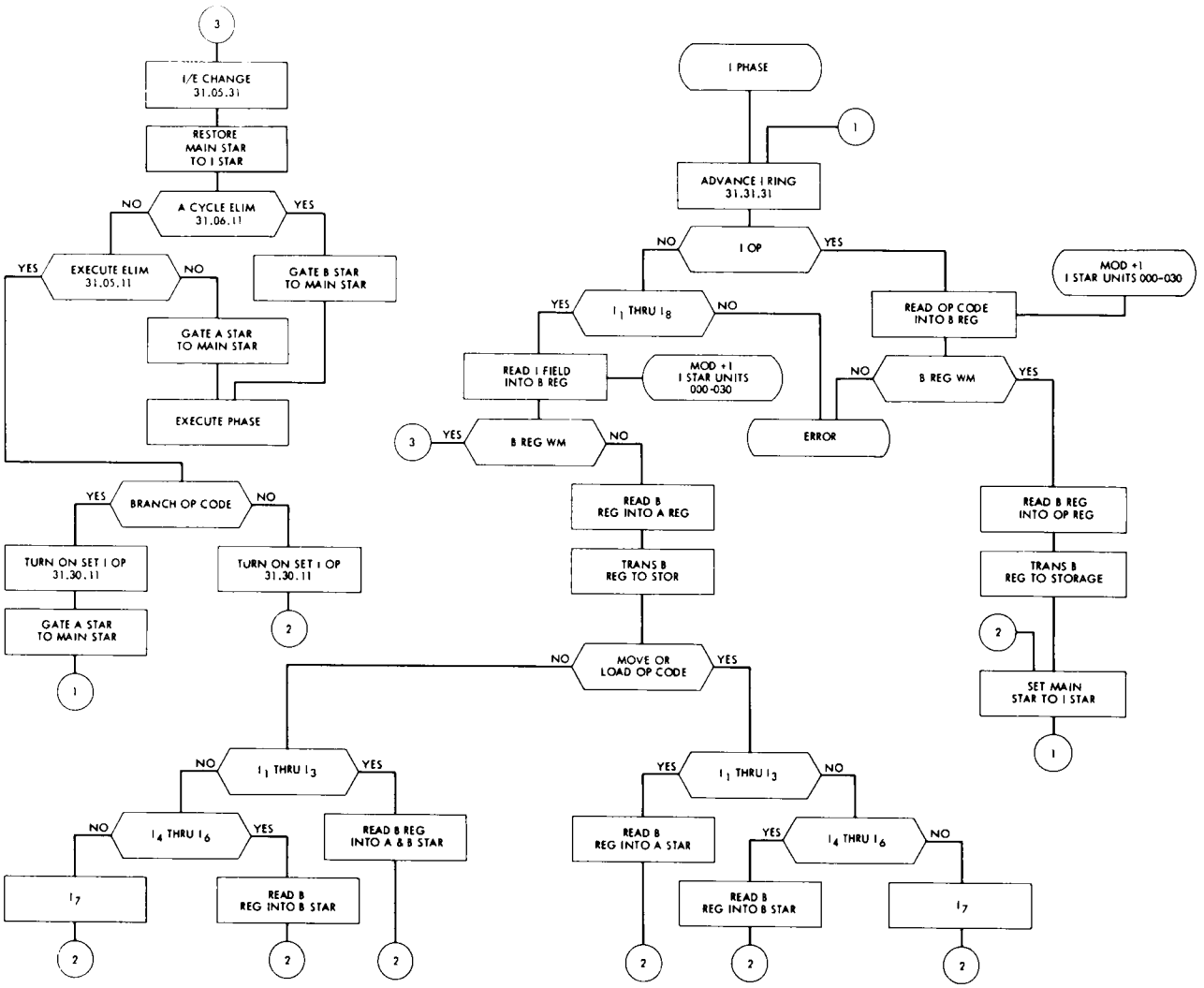


Figure 23. I-Phase

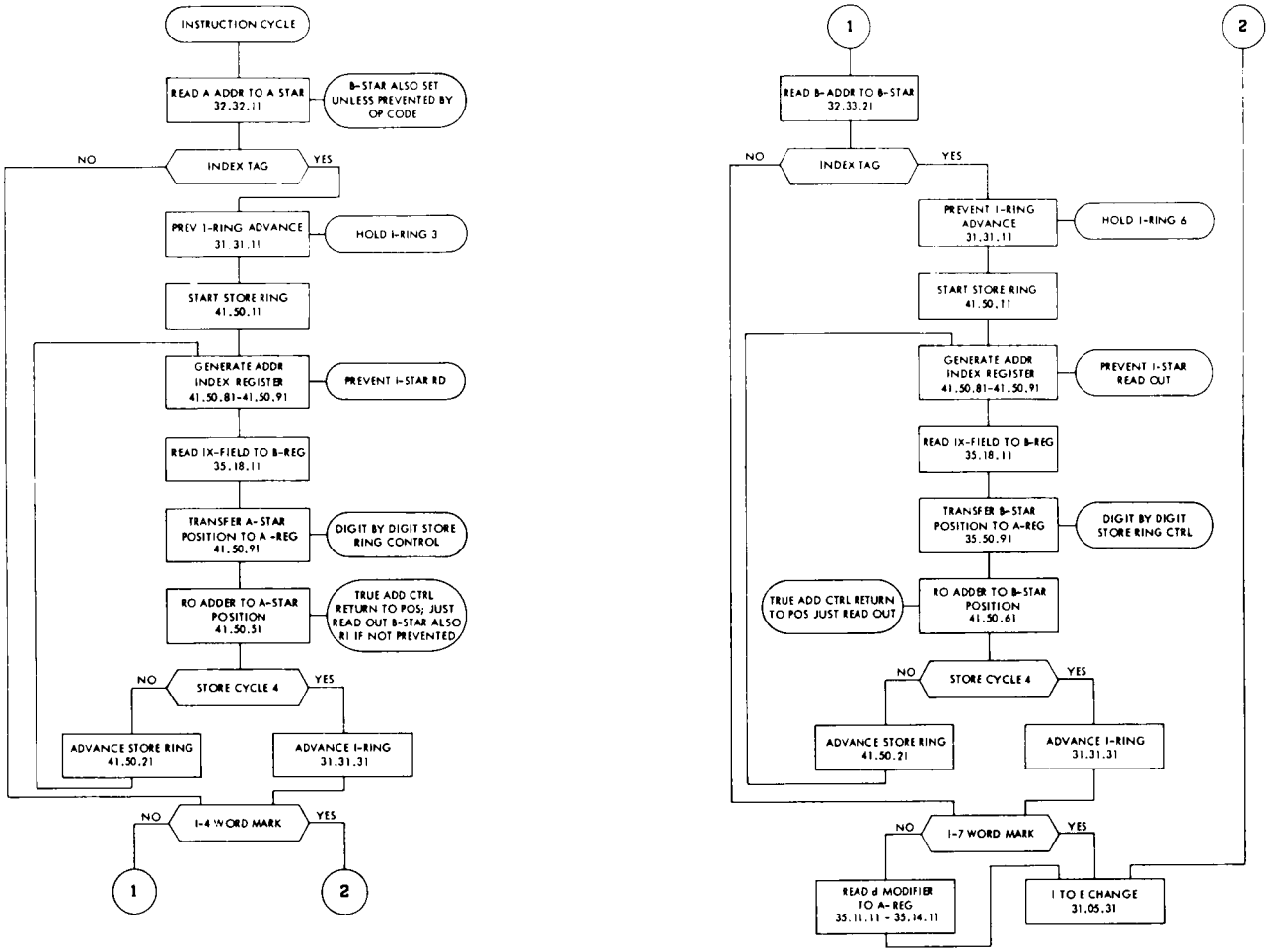


Figure 24. Indexing

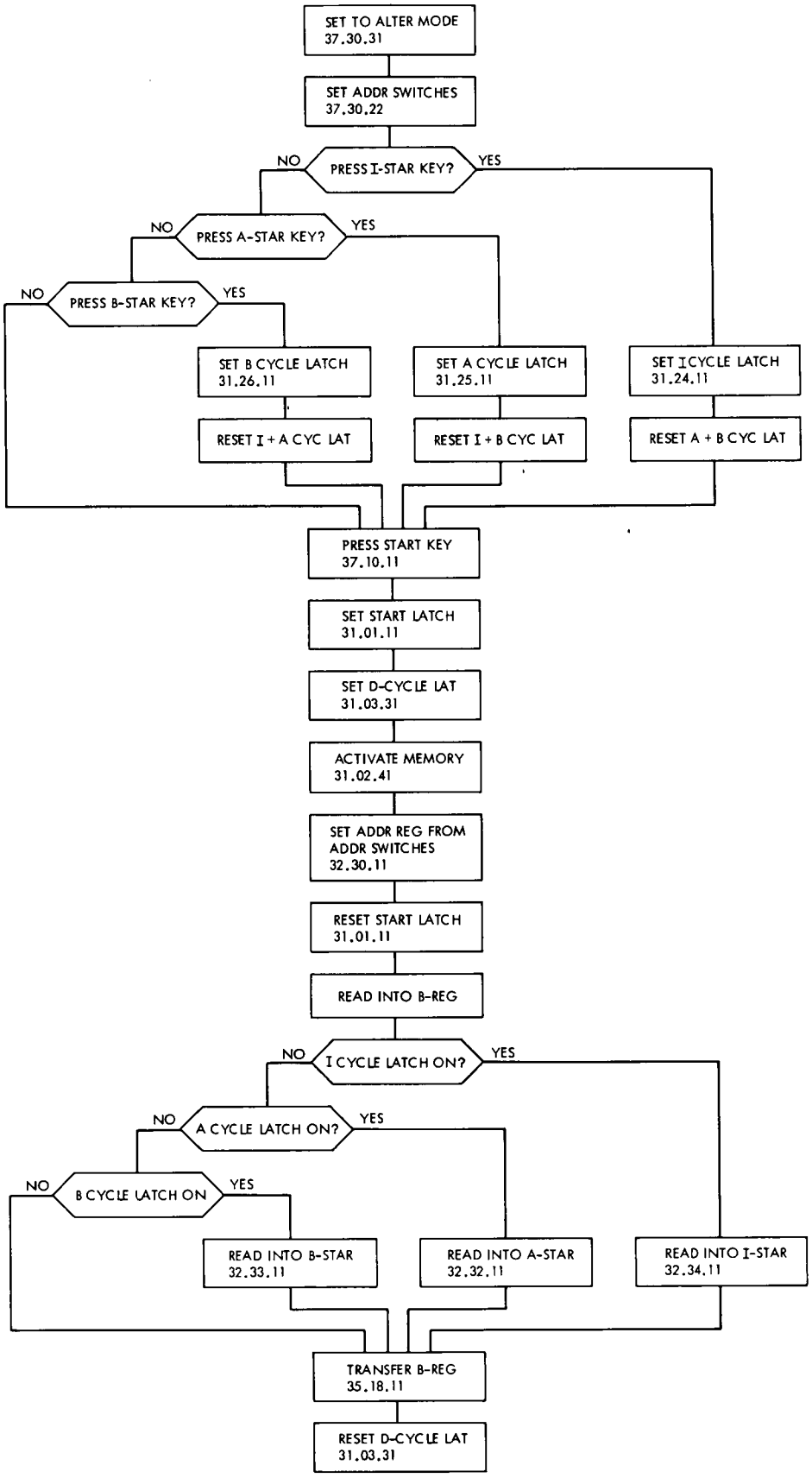


Figure 25. Manual Address Setup

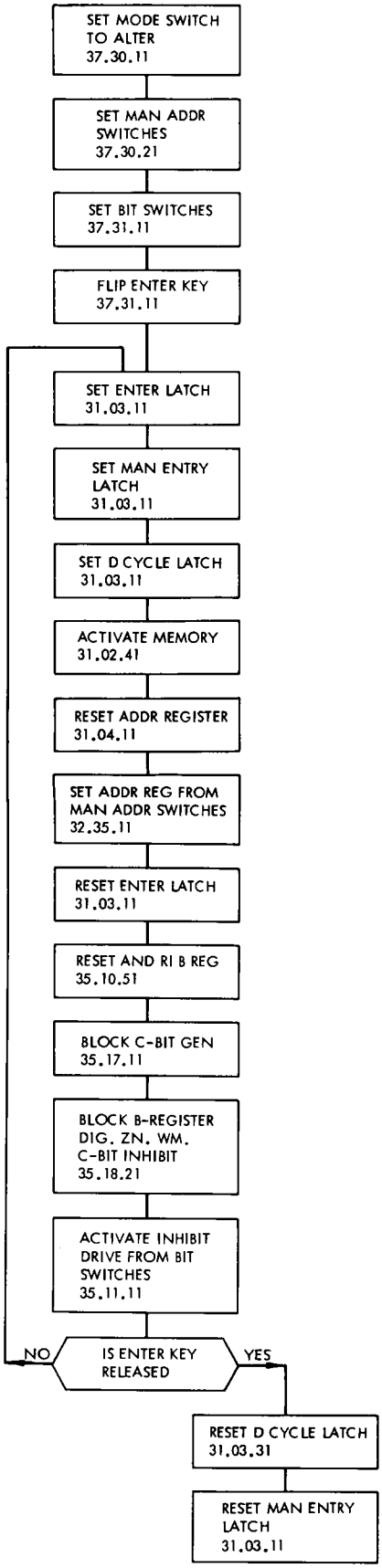


Figure 26. Manual Entry Operation

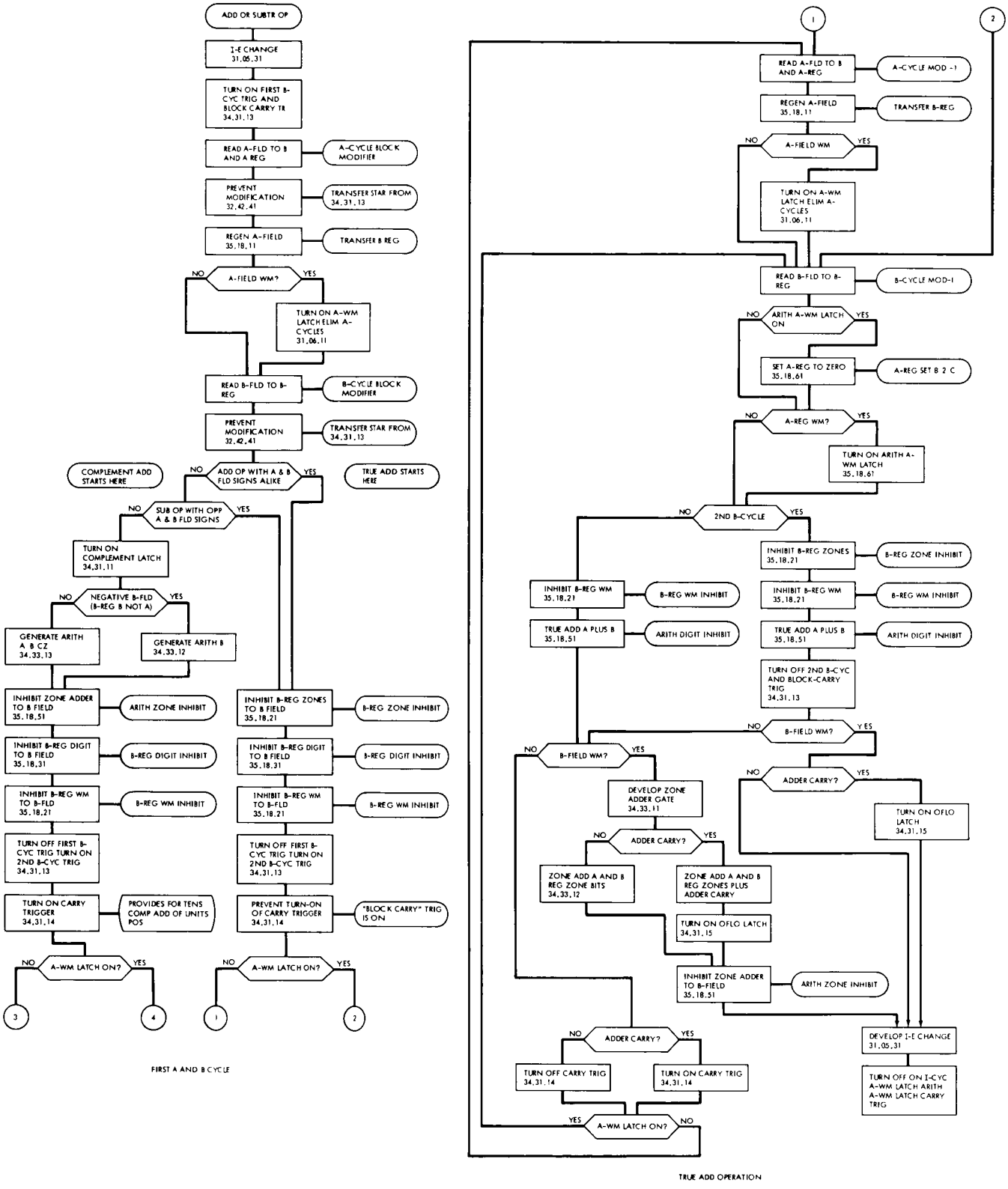


Figure 27. Add or Subtract Operation (Part 1 of 2)

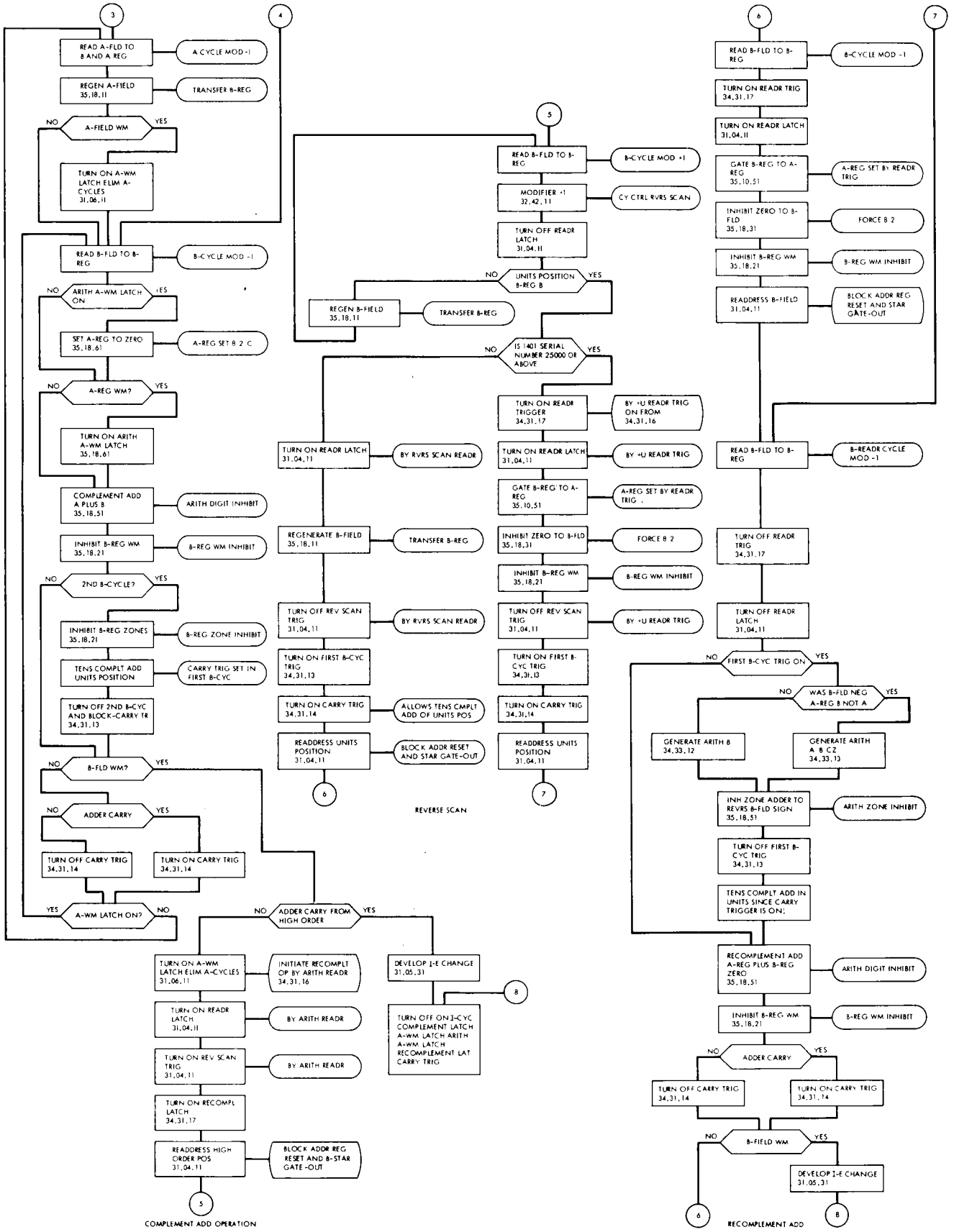


Figure 27. Add or Subtract Operation (Part 2 of 2)

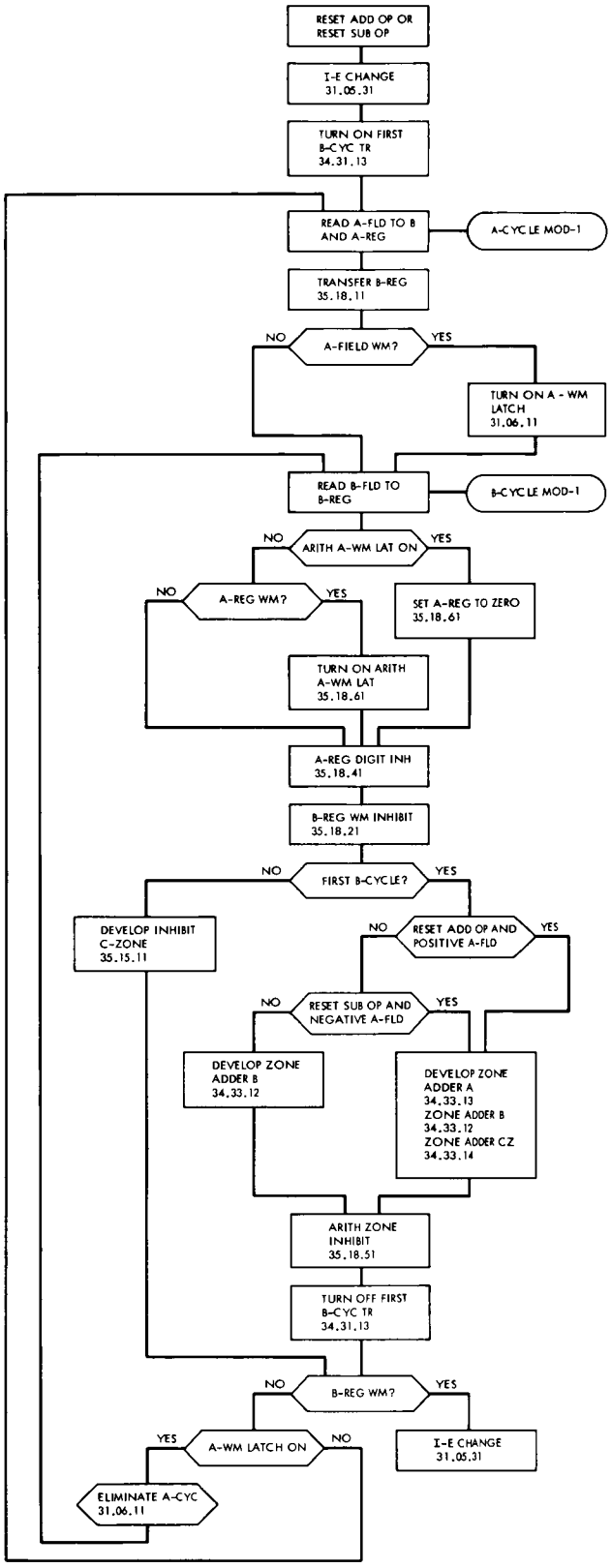
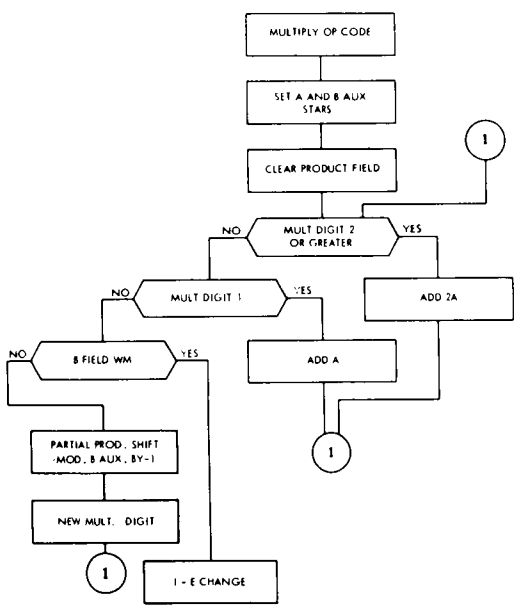


Figure 28. Reset Add or Subtract Operation



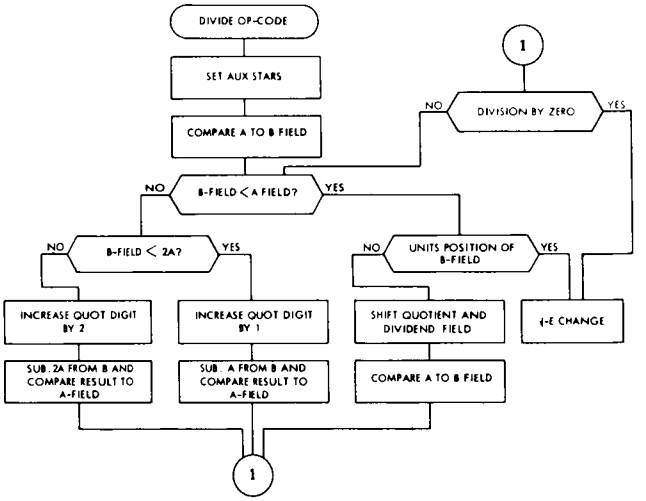


Figure 29. Simplified Multiply/Divide

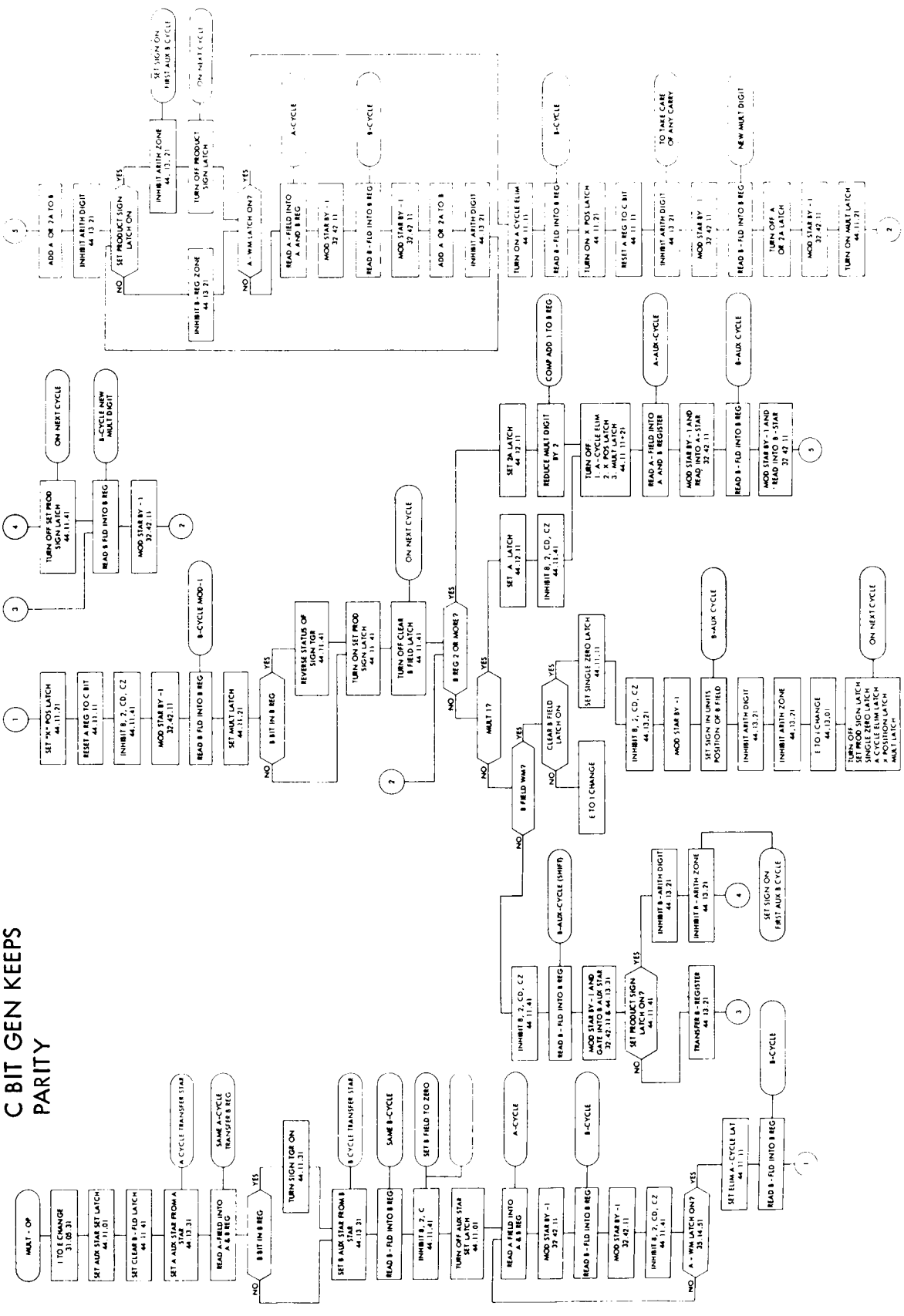


Figure 30. Multiply Operation

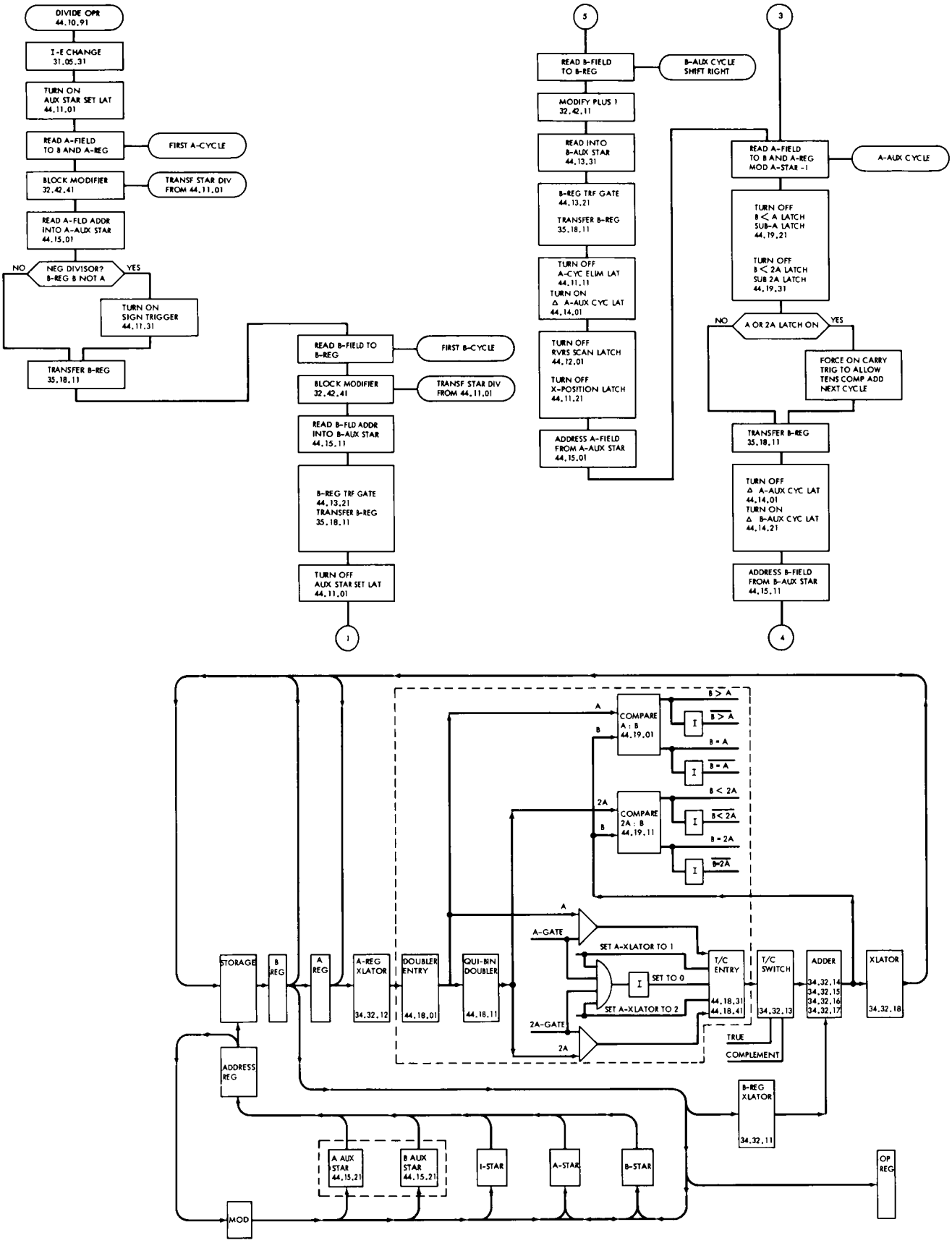


Figure 31. Divide Operation (Part 1 of 2)

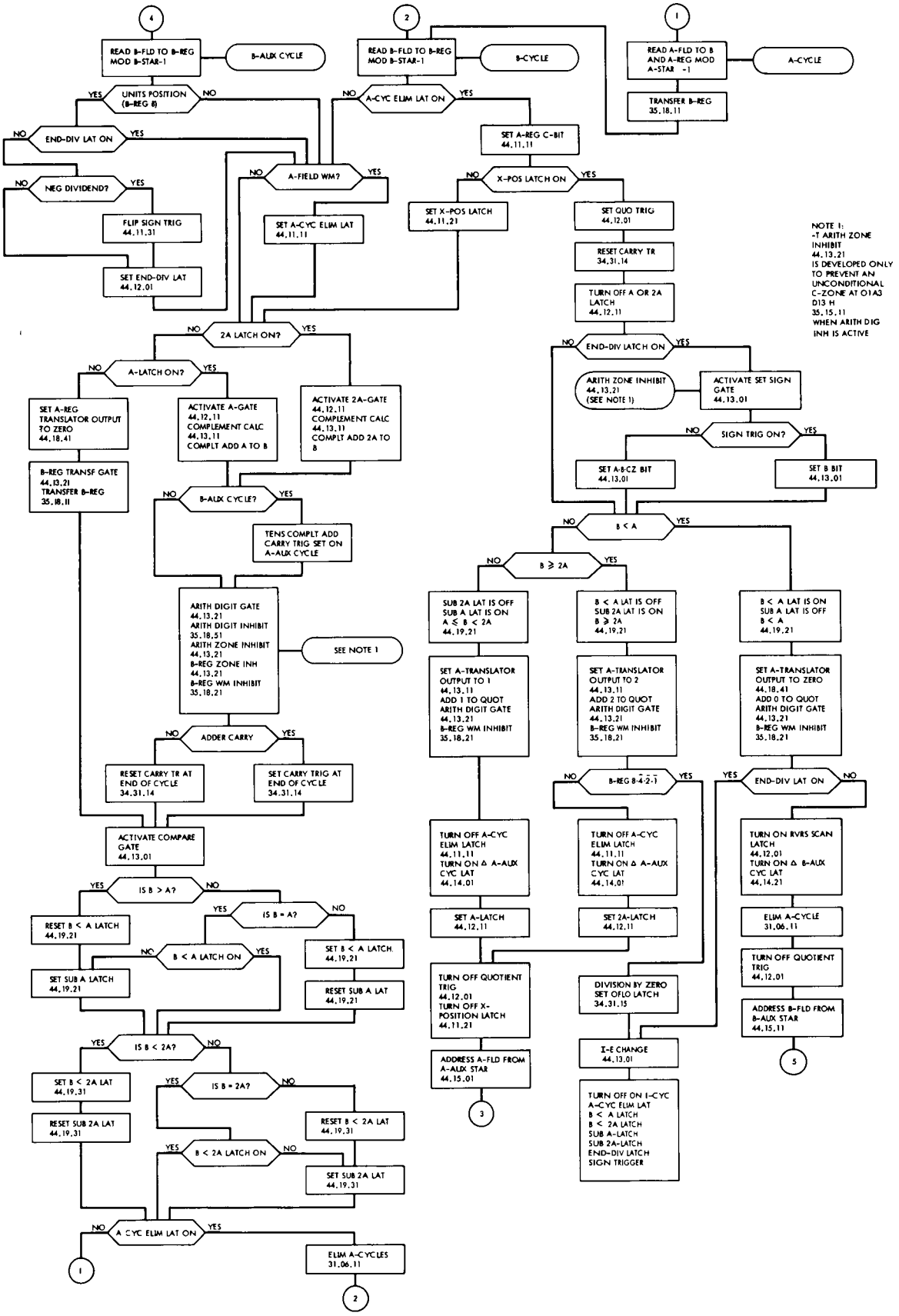


Figure 31. Divide Operation (Part 2 of 2)

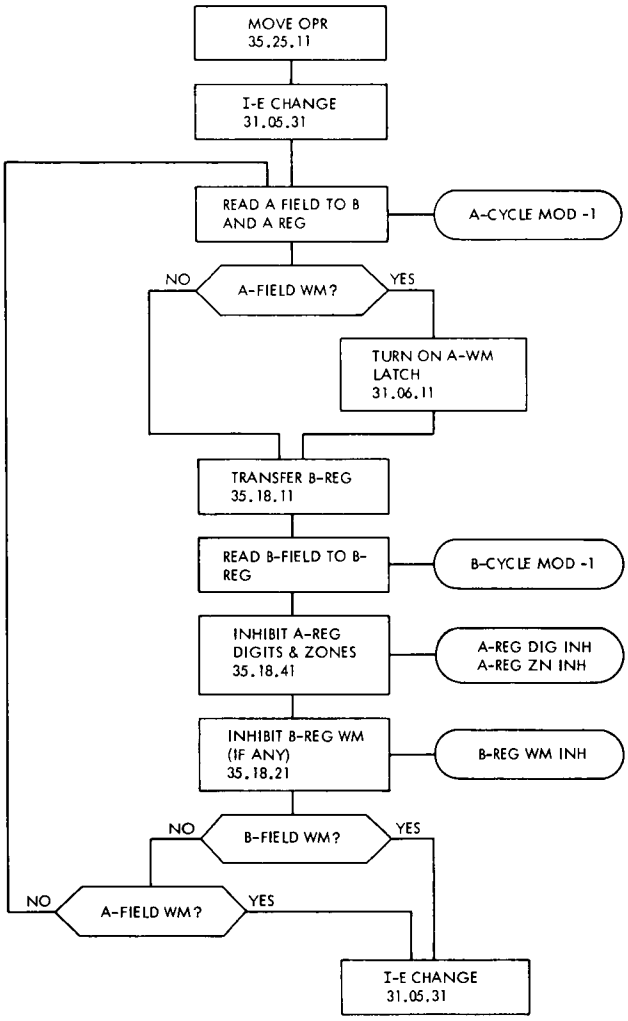


Figure 32. Move Operation

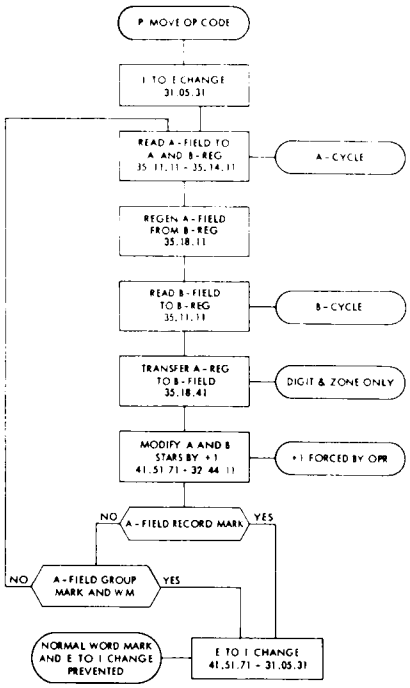


Figure 33. Move Record

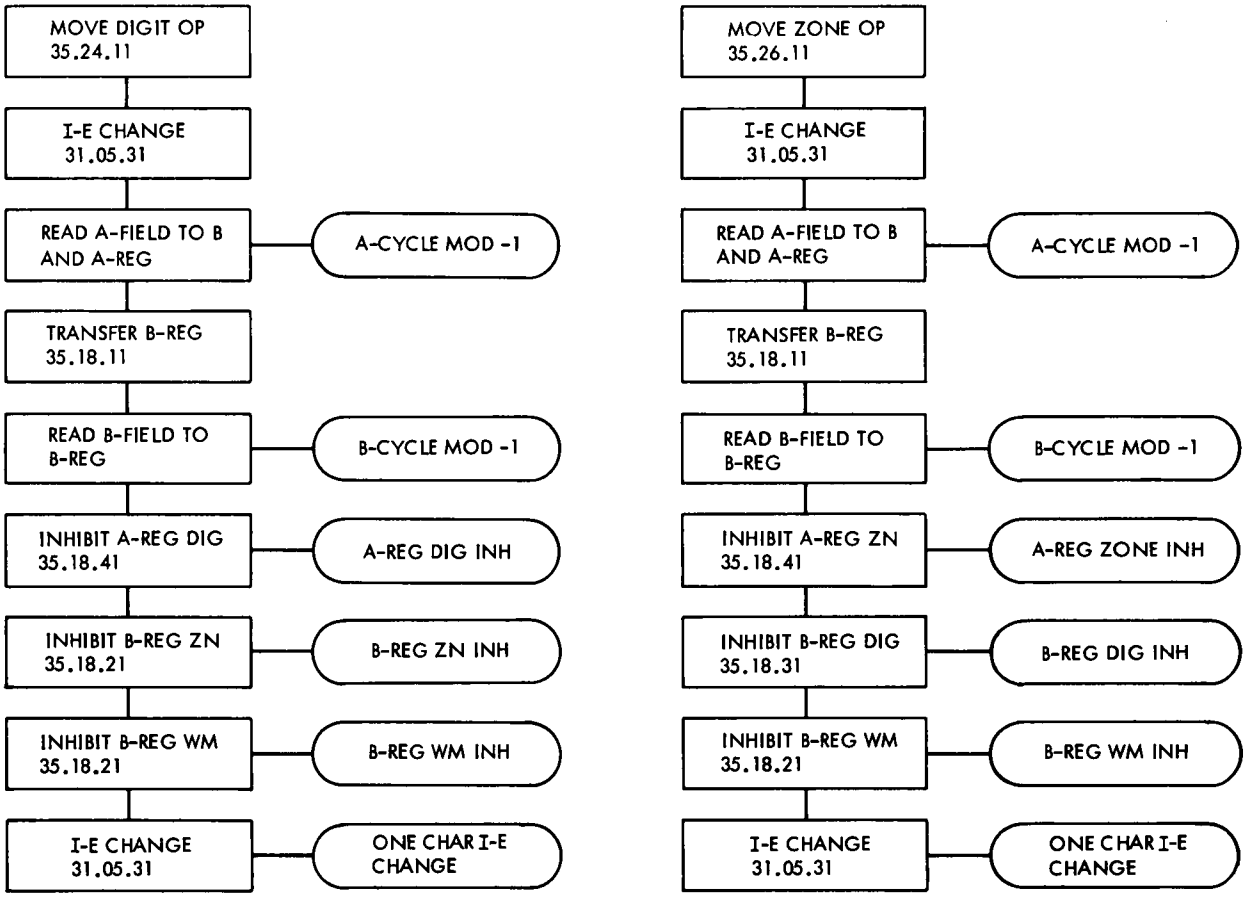


Figure 34. Move Digit Move Zone

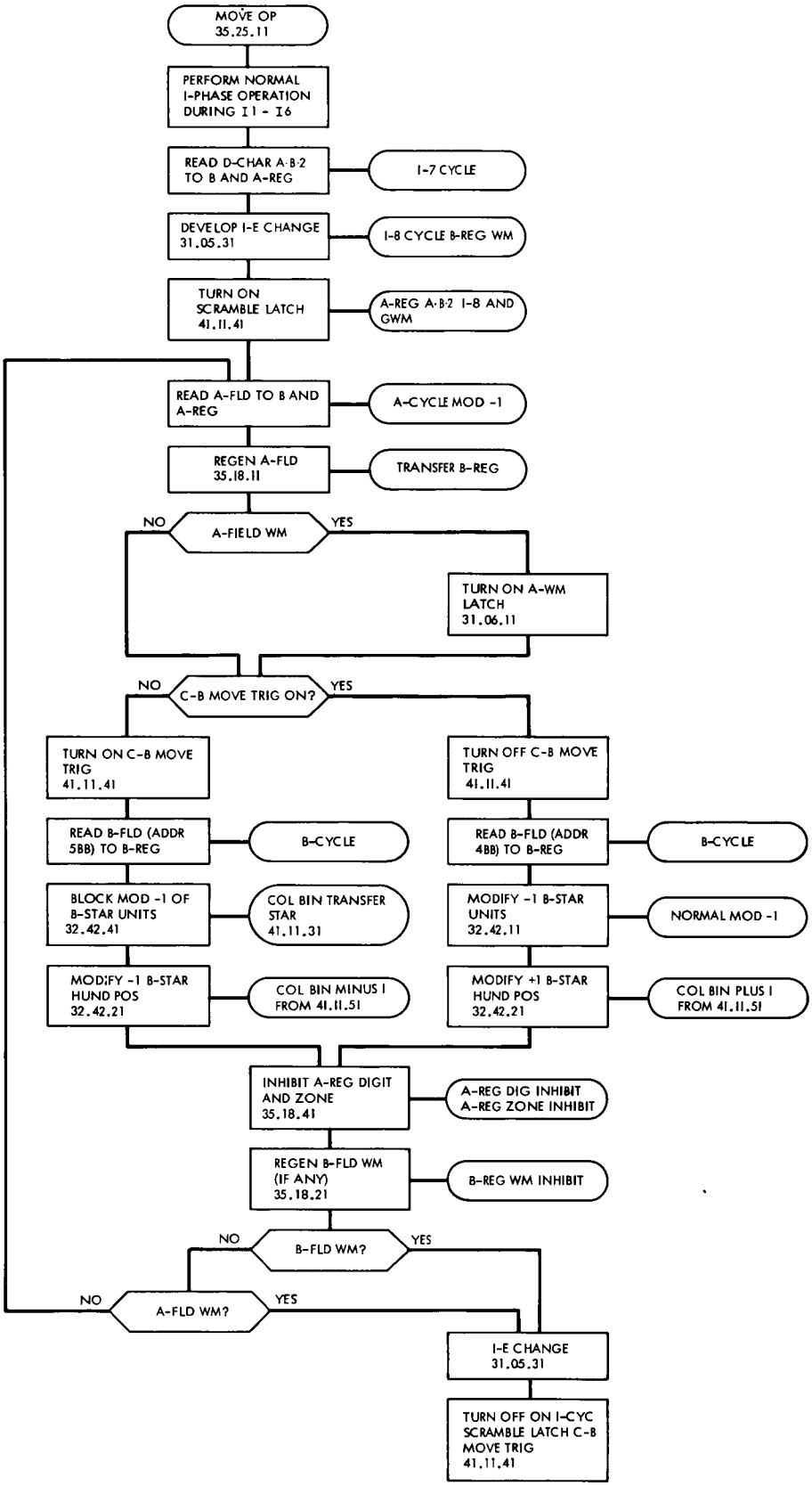


Figure 35. Move and Binary Code (Scramble)

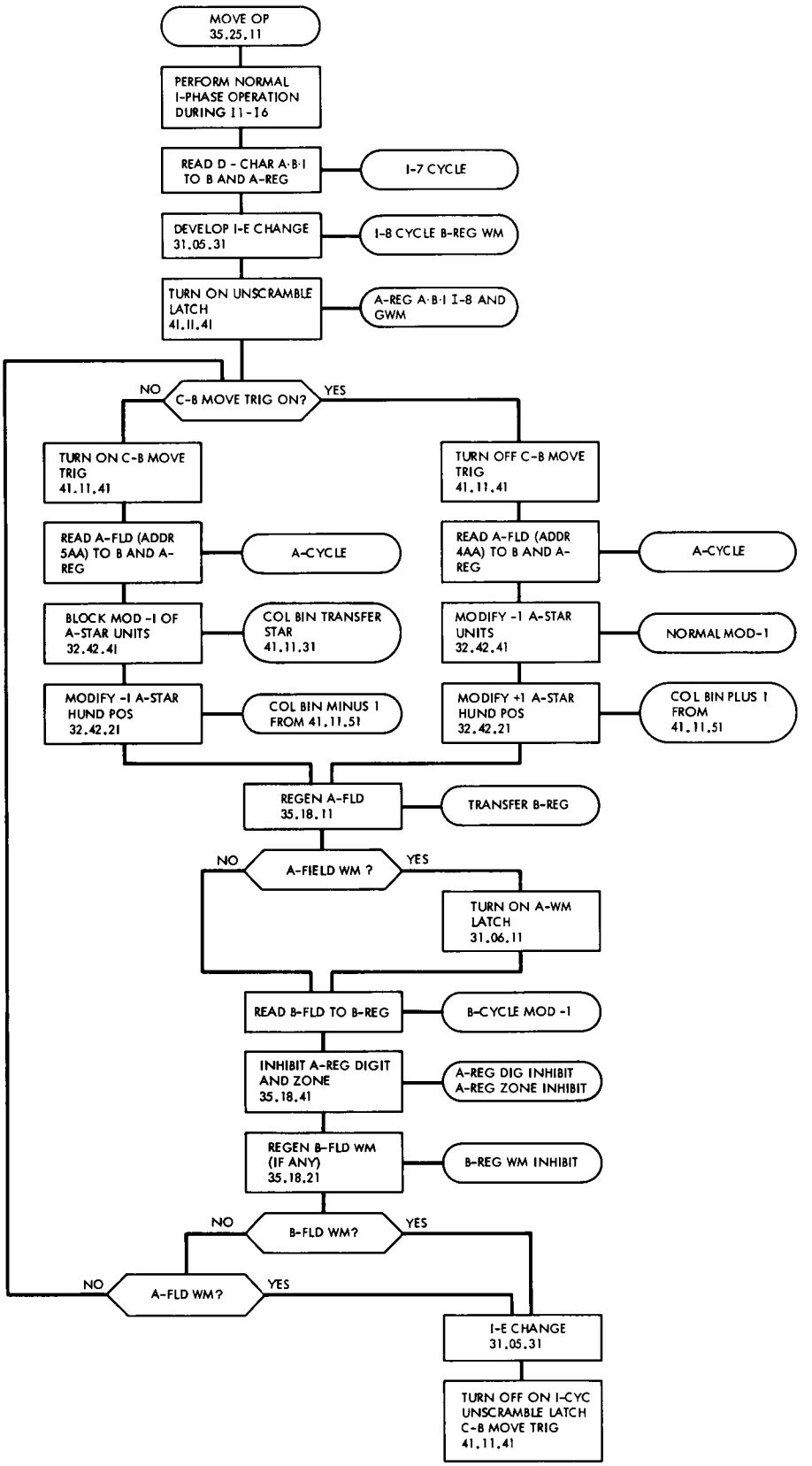


Figure 36. Move and Binary Code (Unscramble)

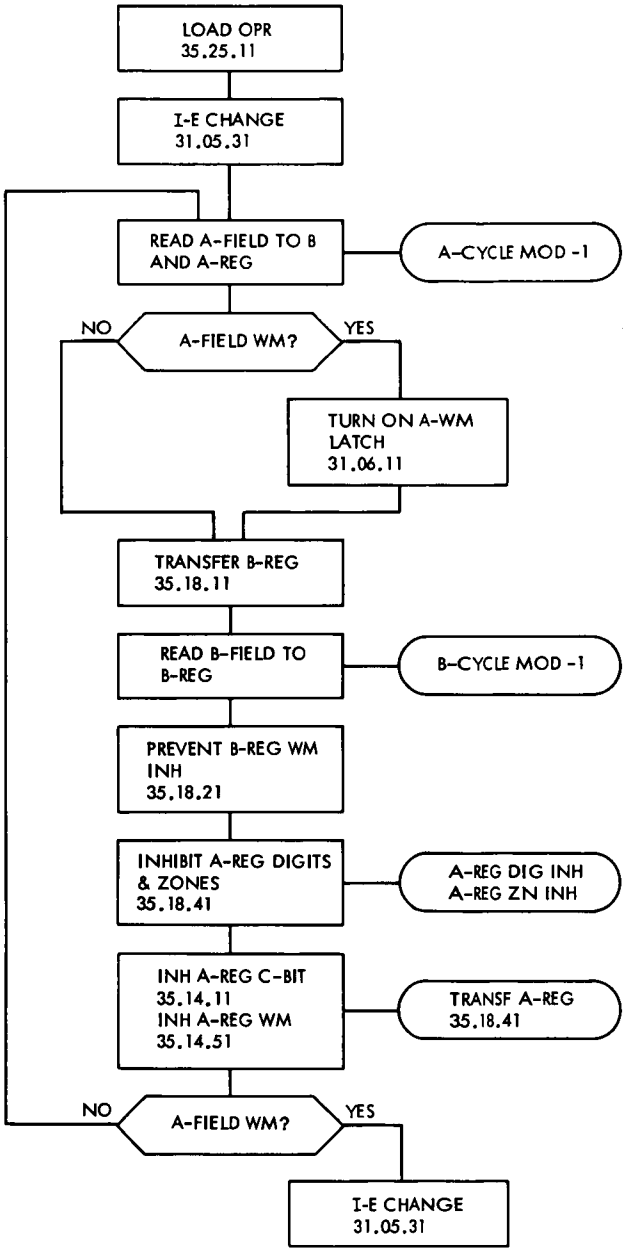


Figure 37. Load Operation

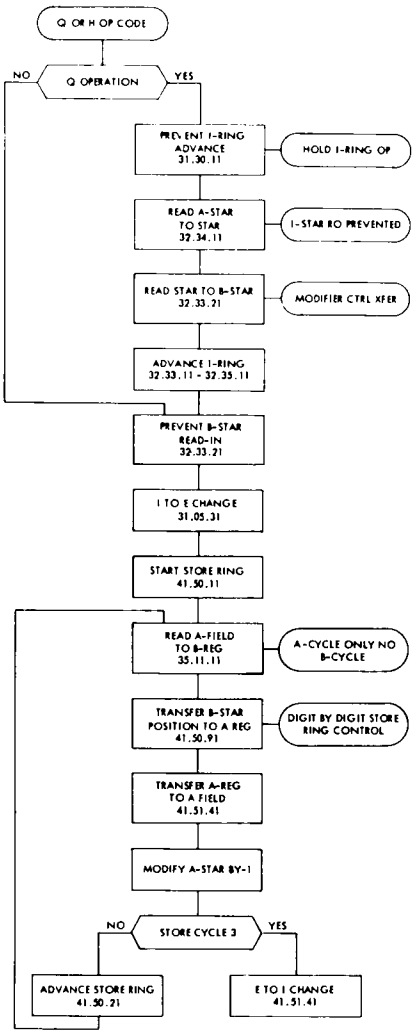


Figure 38. Store Operation

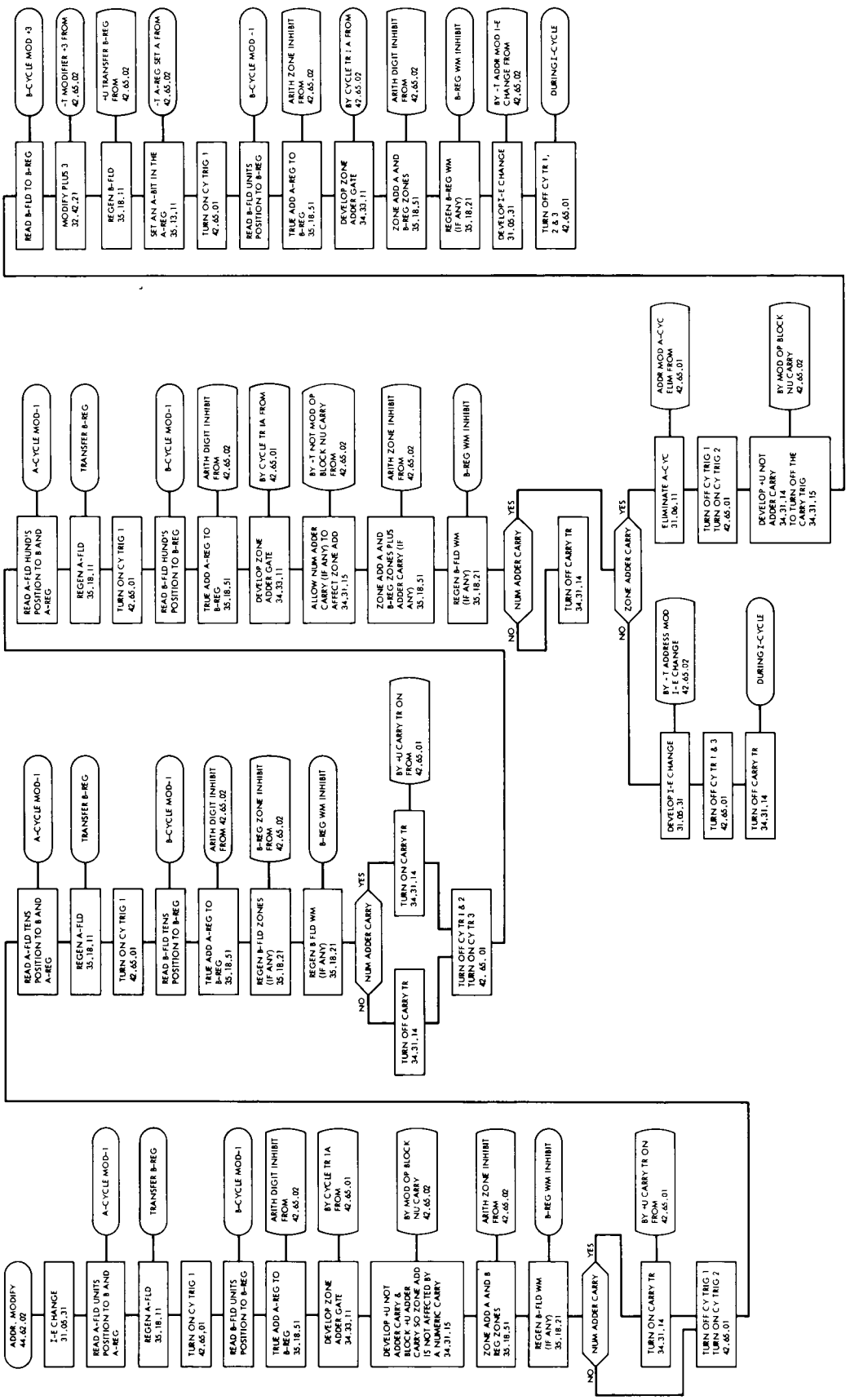


Figure 39. Address Modify

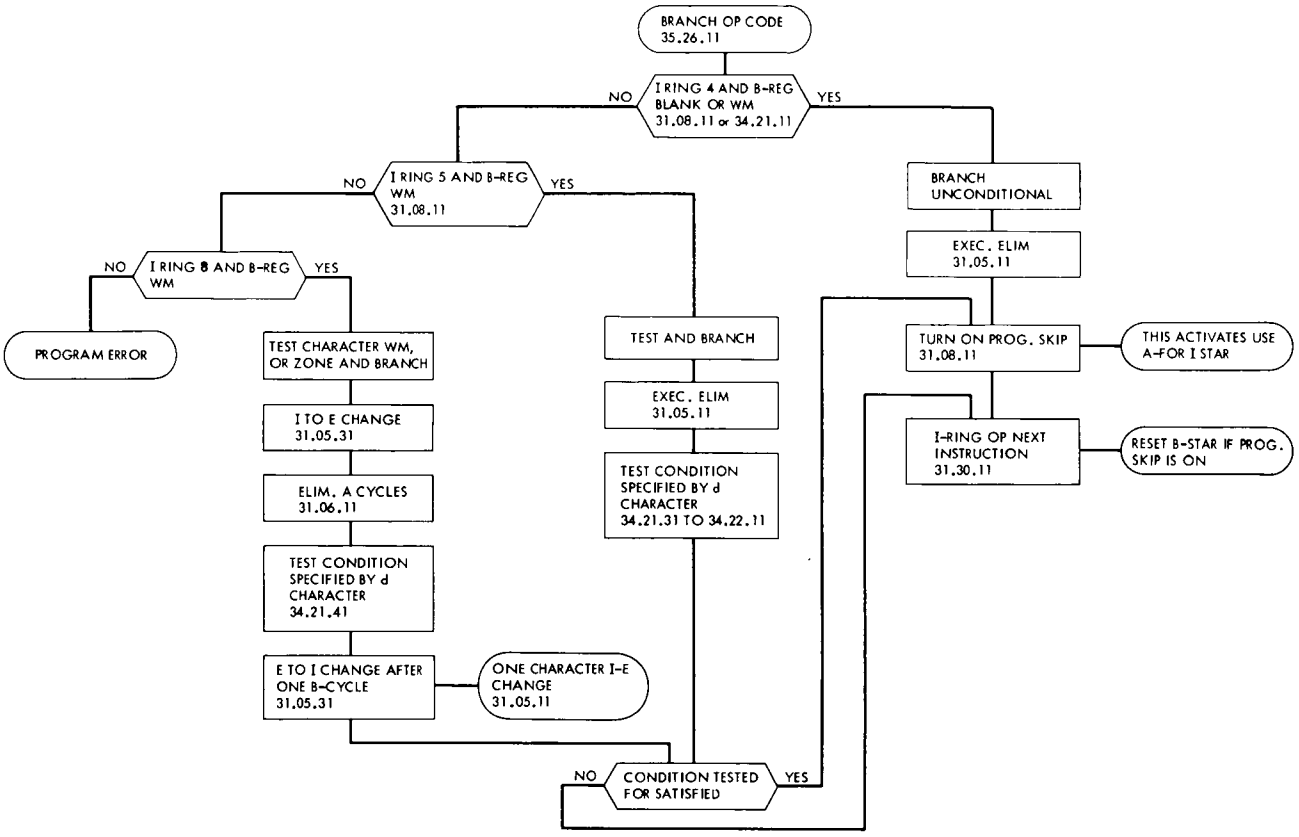


Figure 40. Branch Operation

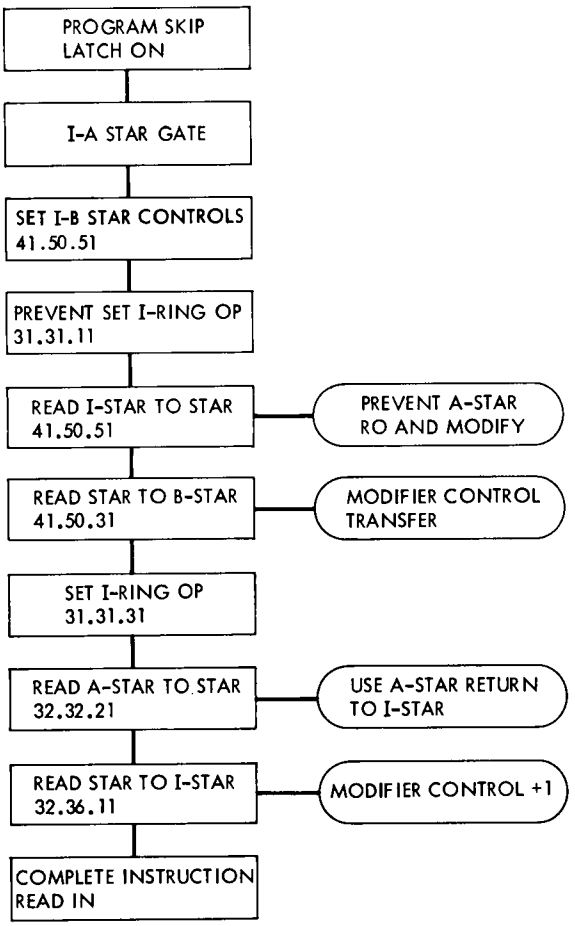


Figure 41. Branch Modification

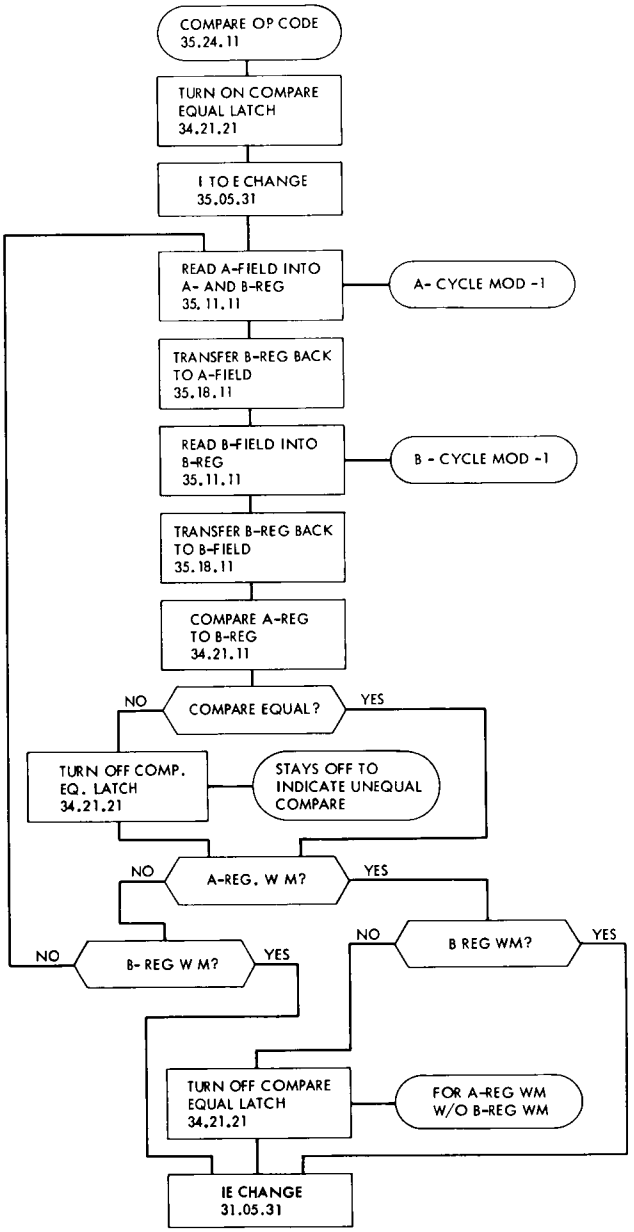


Figure 42. Compare

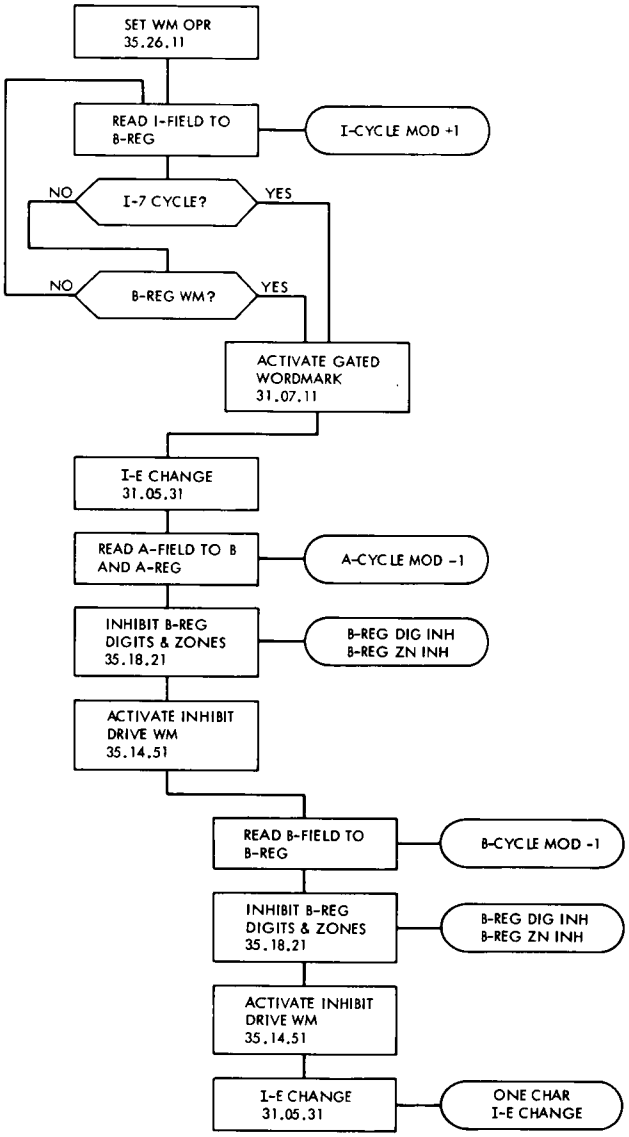


Figure 43. Set WM Operation

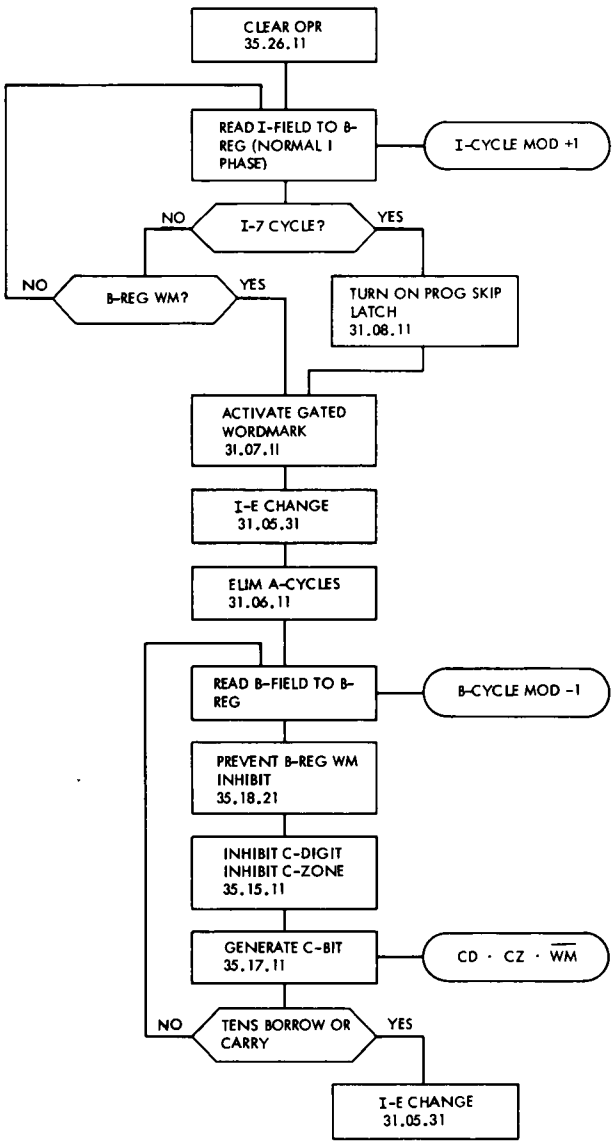


Figure 44. Clear Operation

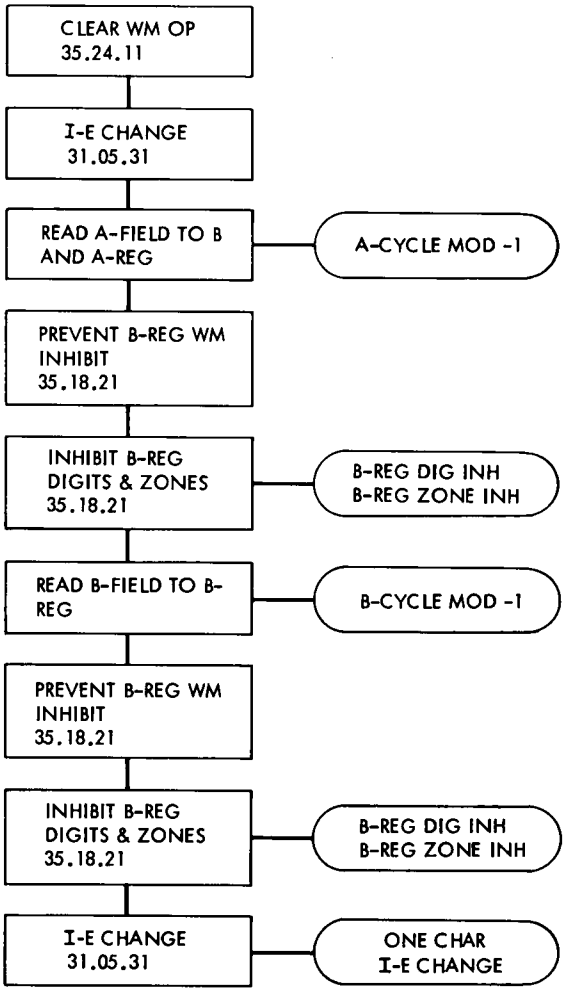


Figure 45. Clear WM Operation

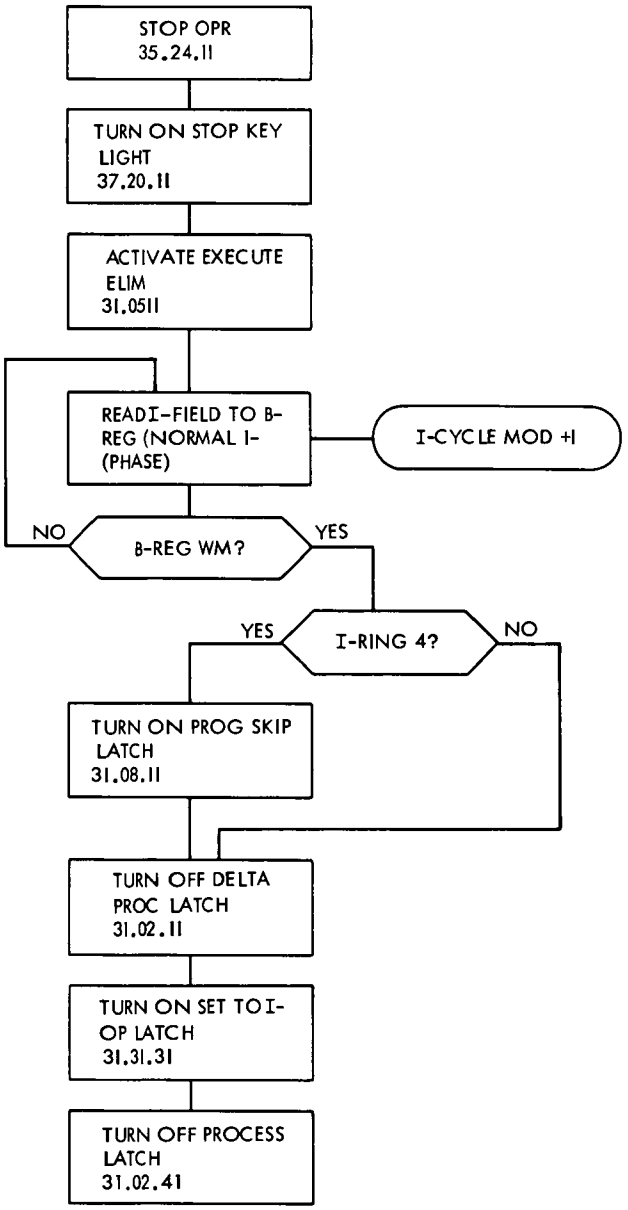


Figure 46. Stop Operation

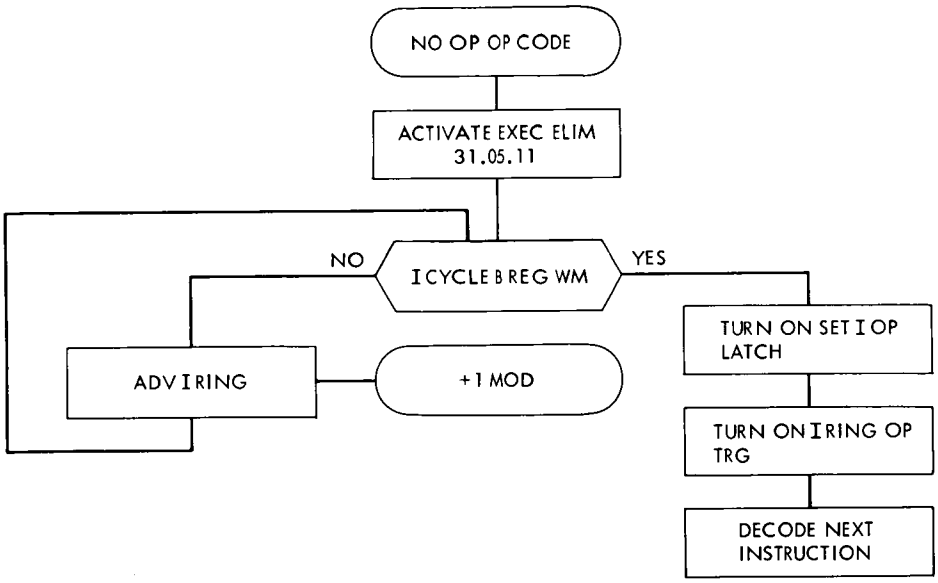


Figure 47. No Operation

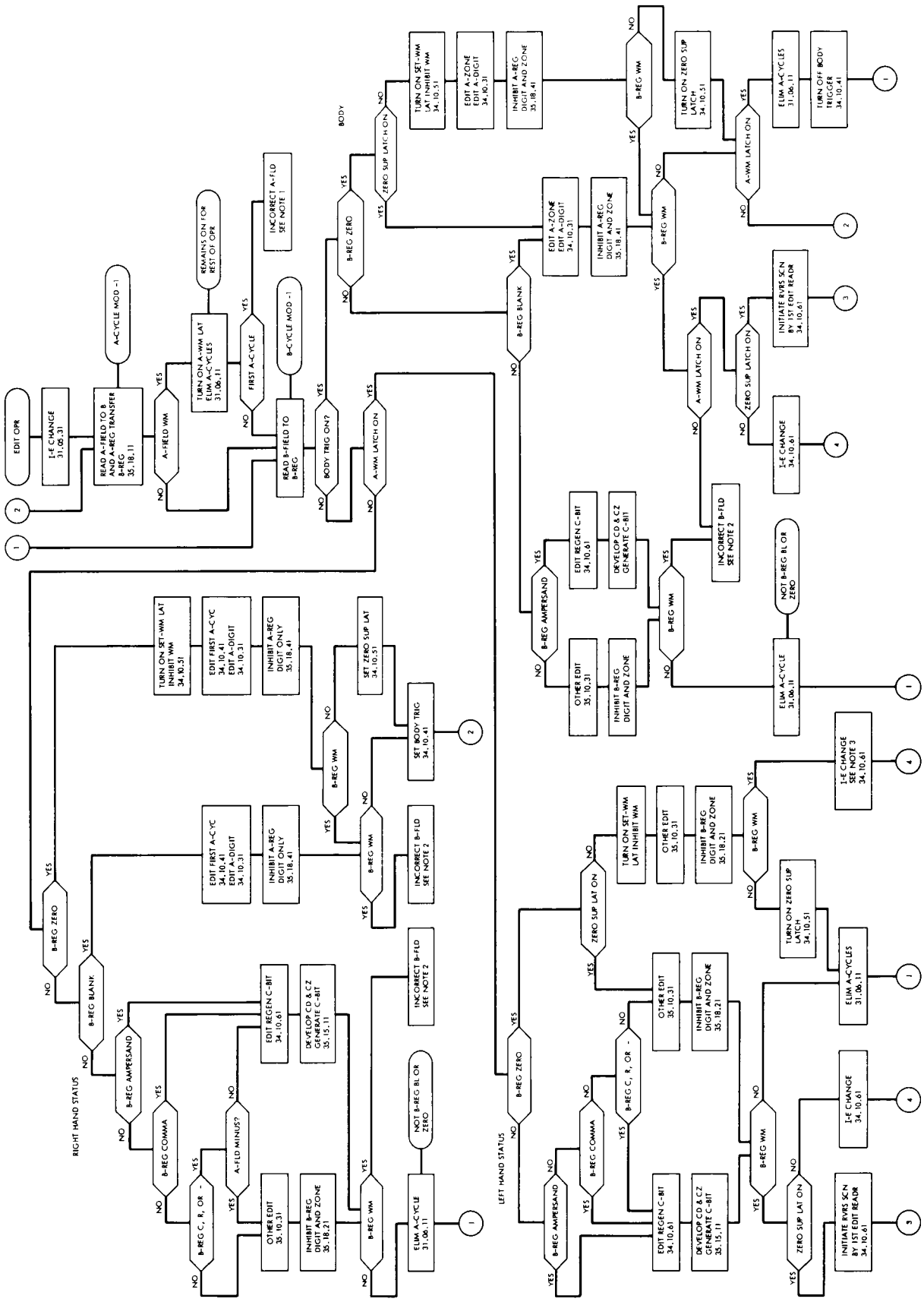


Figure 48. Edit (Part 1 of 2)

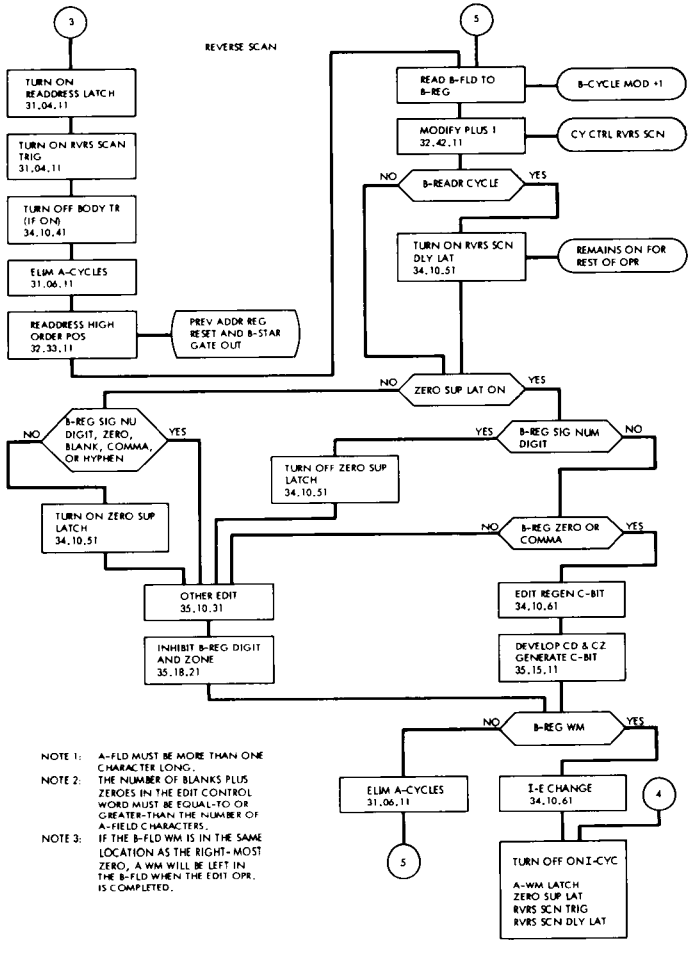


Figure 48. Edit (Part 2 of 2)

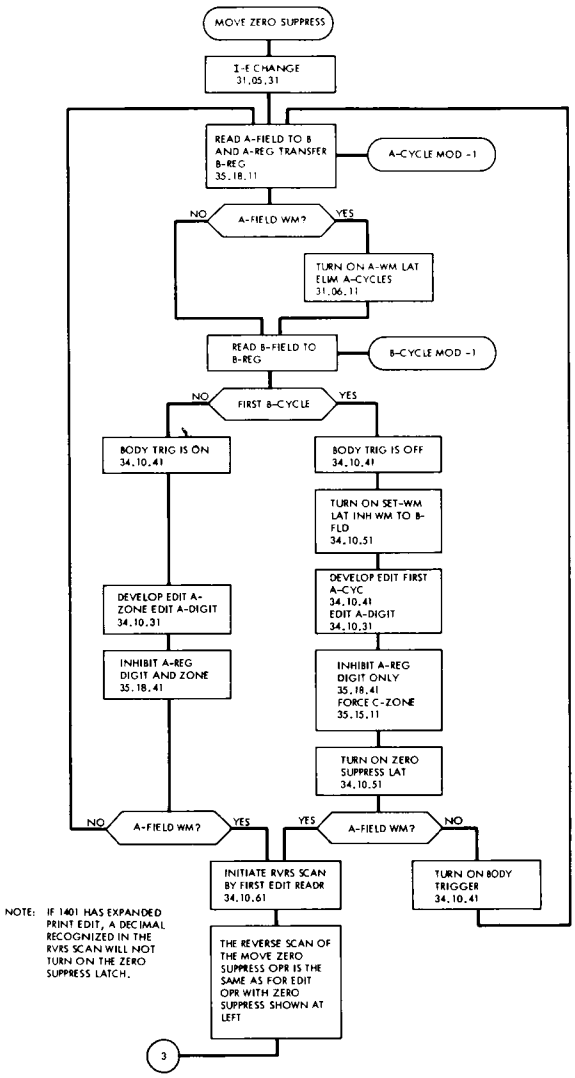


Figure 49. Move Zero Suppress

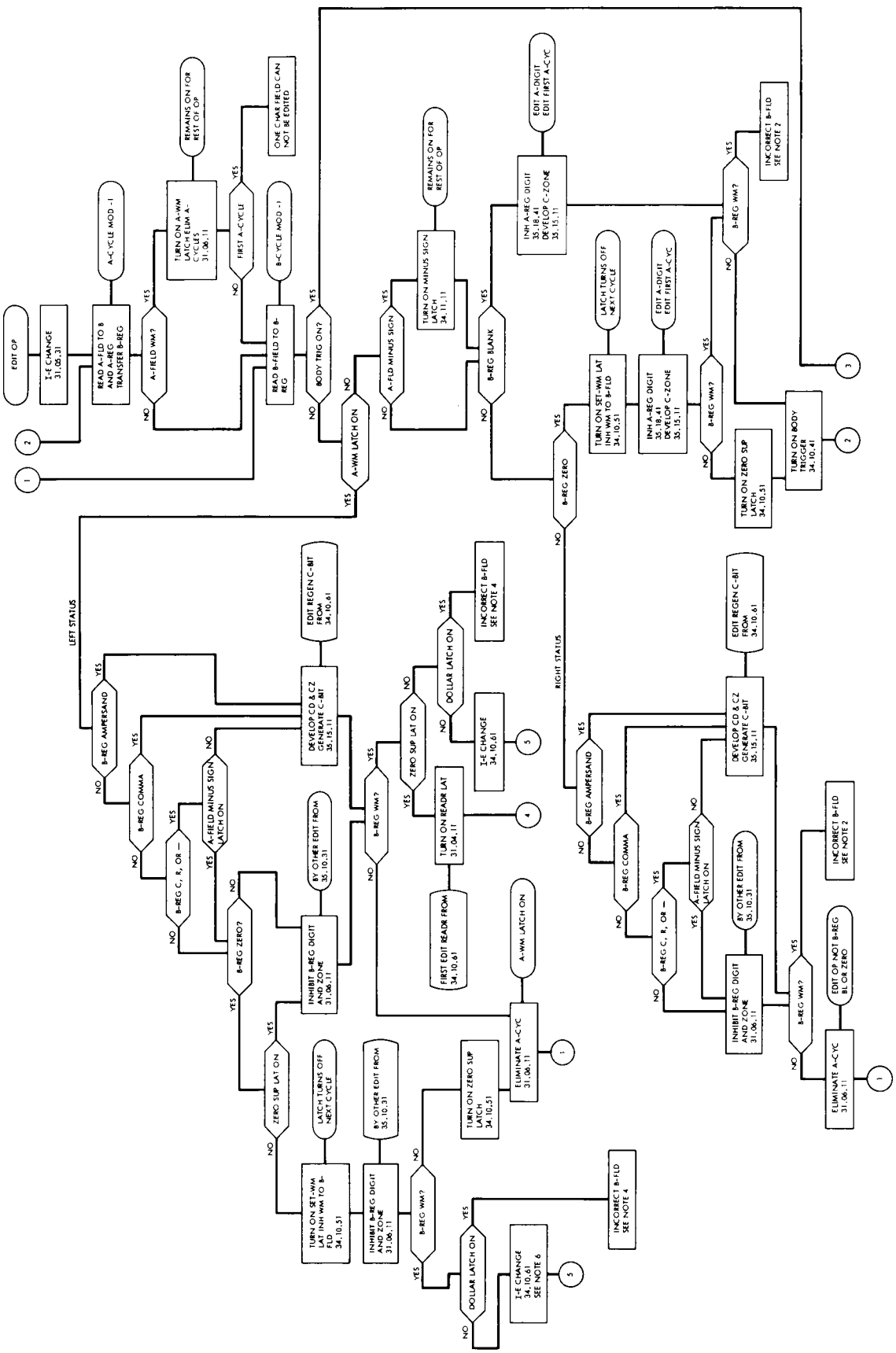


Figure 50. Expanded Edit (Part 1 of 3)

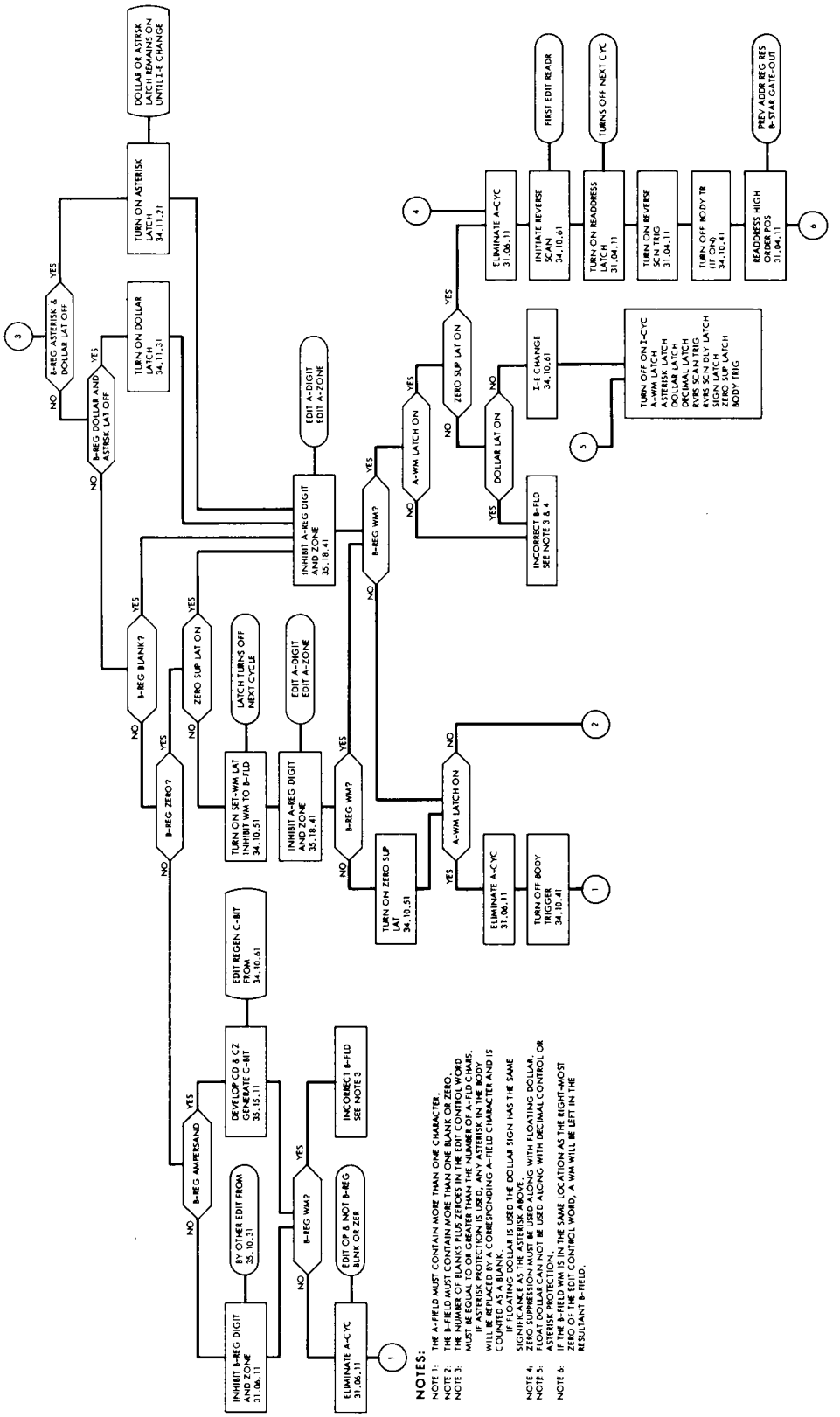


Figure 50. Expanded Edit (Part 2 of 3)

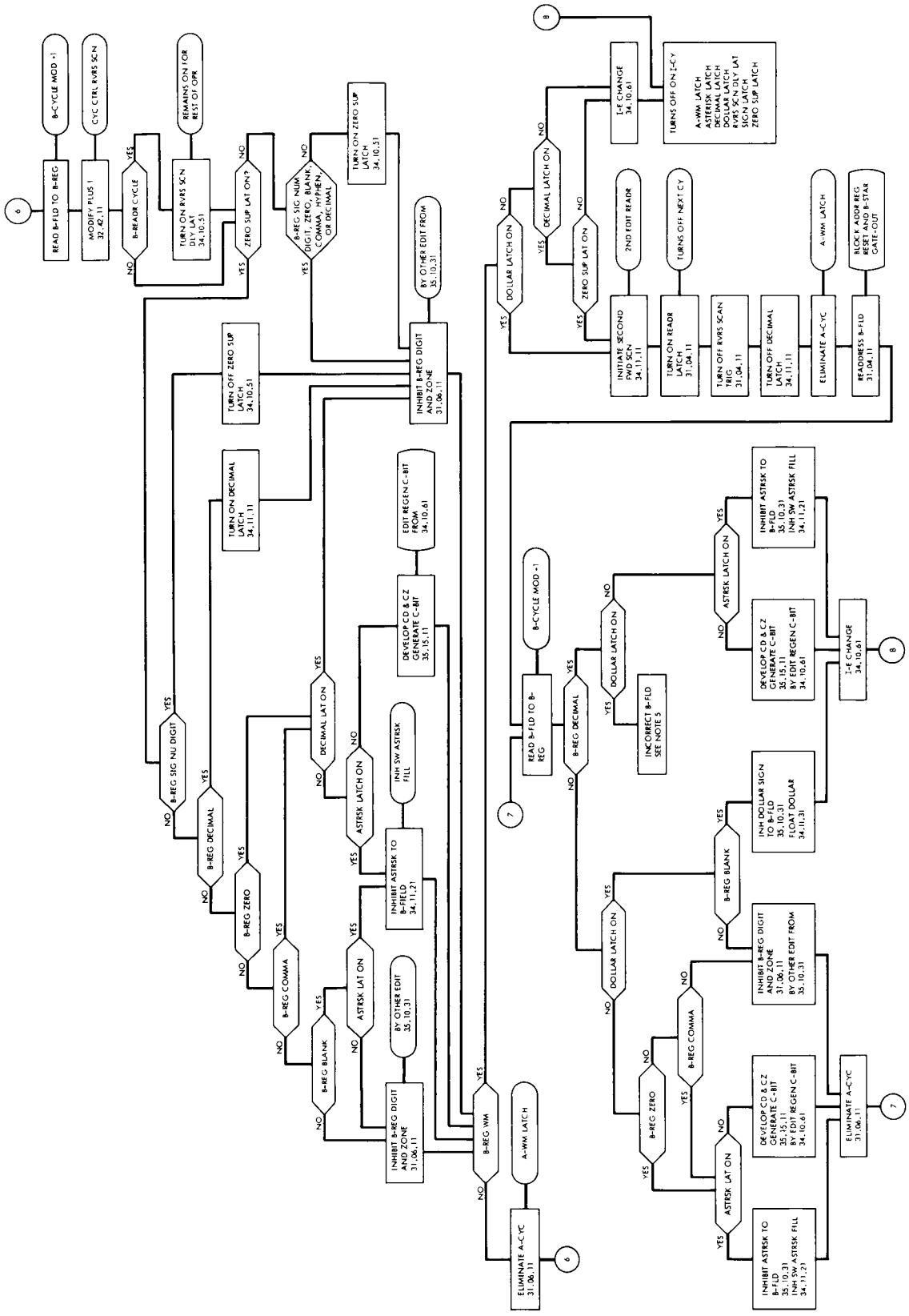


Figure 50. Expanded Edit (Part 3 of 3)

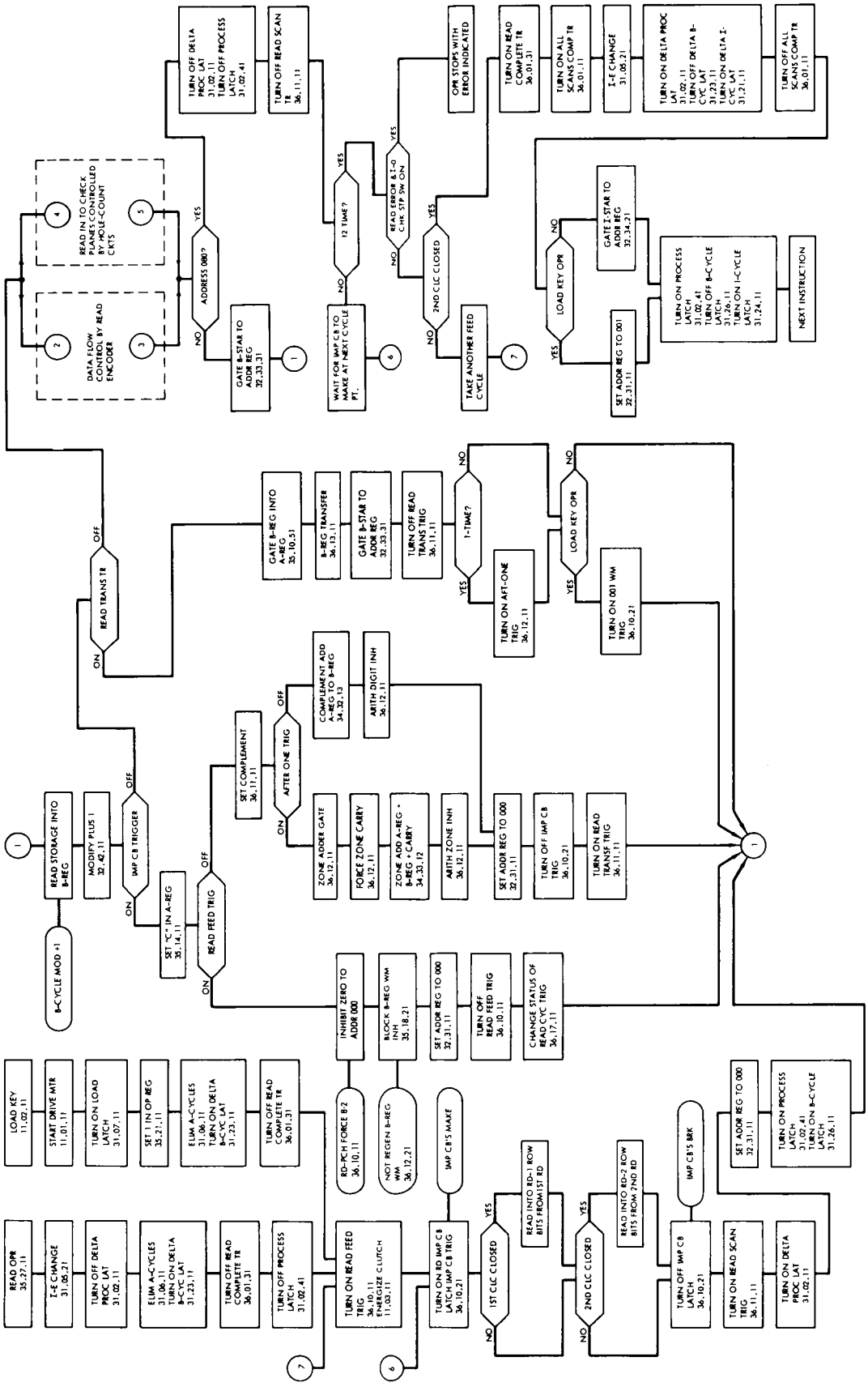


Figure 51. Read Operation, Load Key, Hole Count (Part 1 of 3)

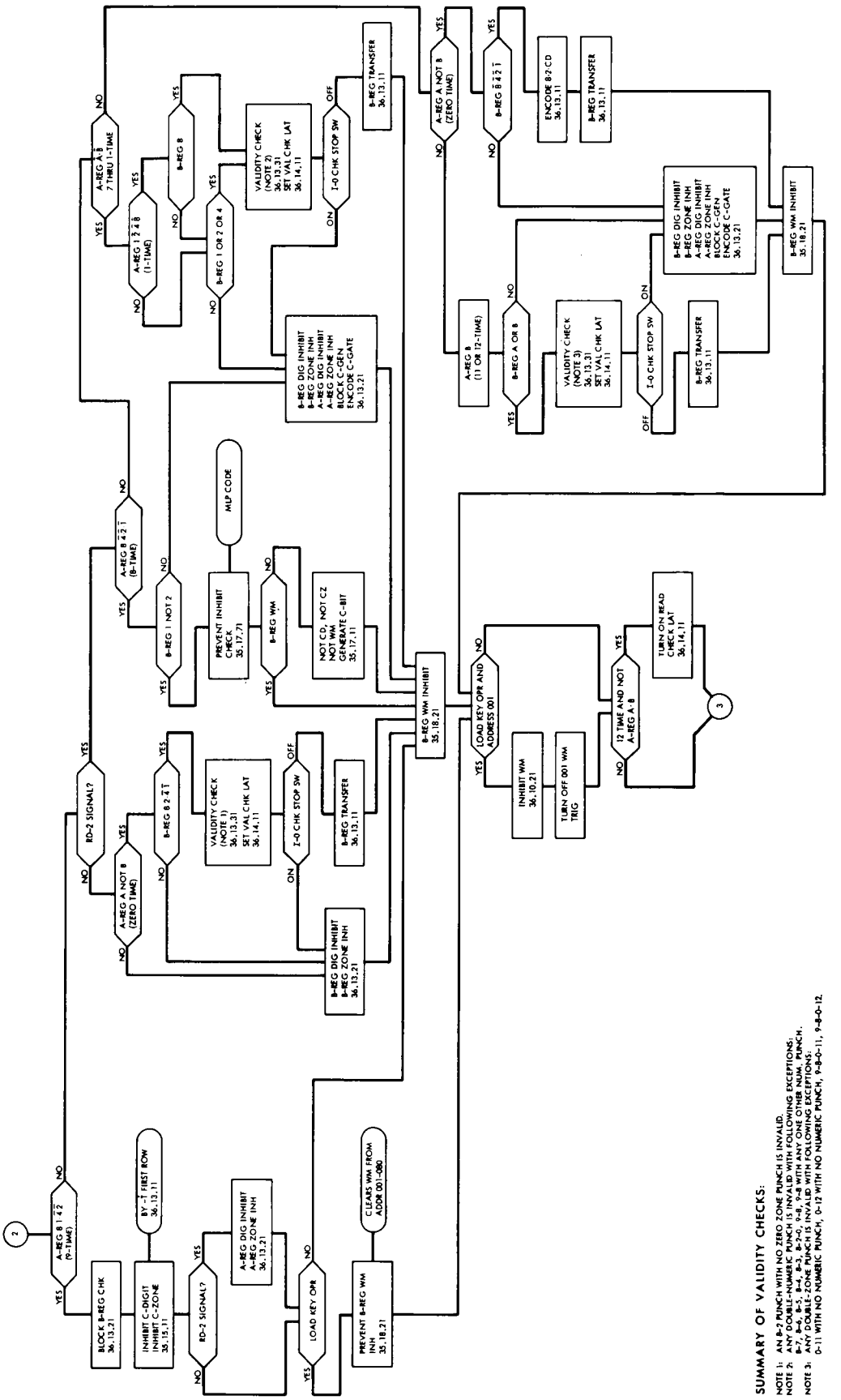


Figure 51. Read Operation, Load Key, Hole Count (Part 2 of 3)

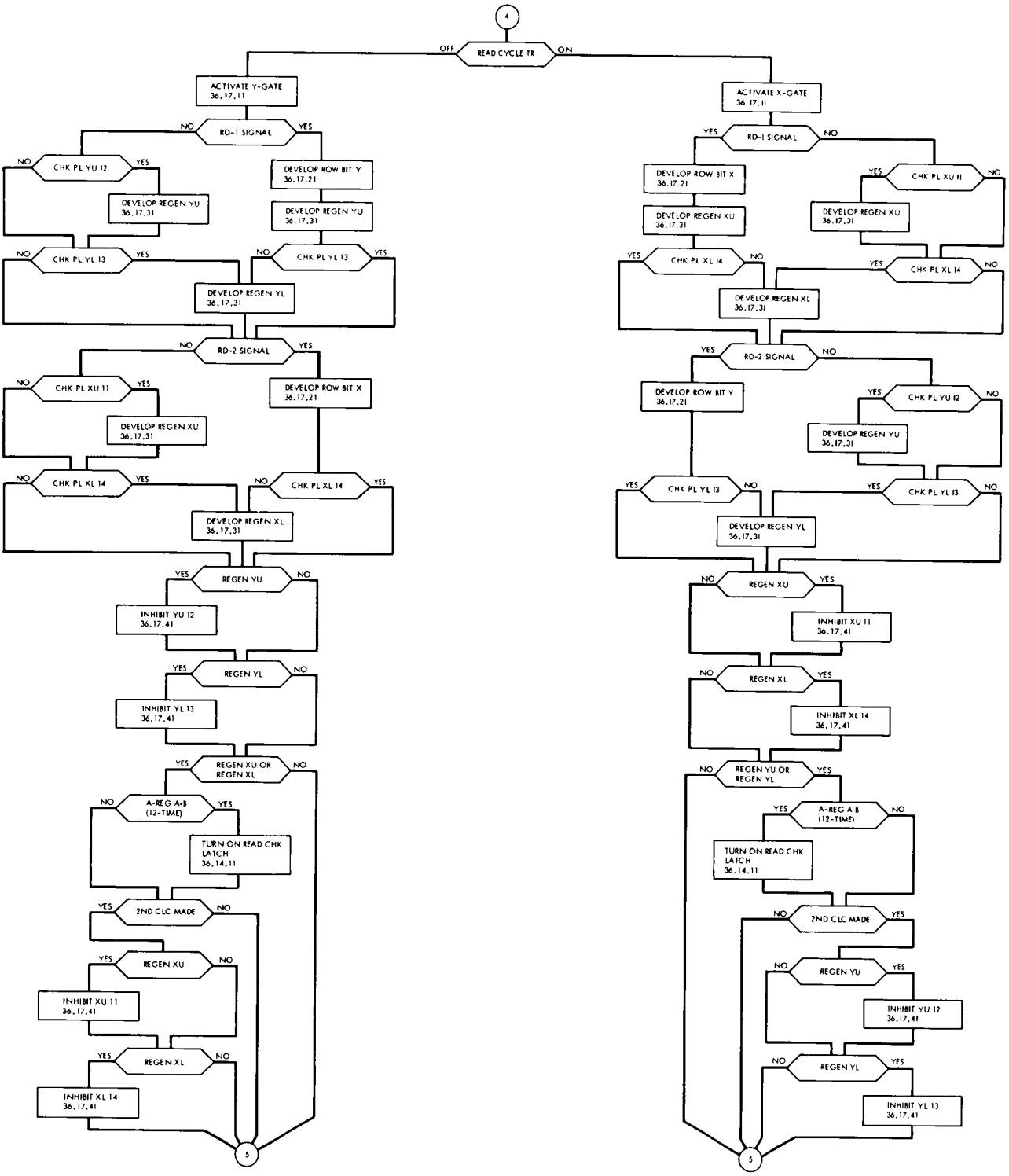


Figure 51. Read Operation, Load Key, Hole Count (Part 3 of 3)

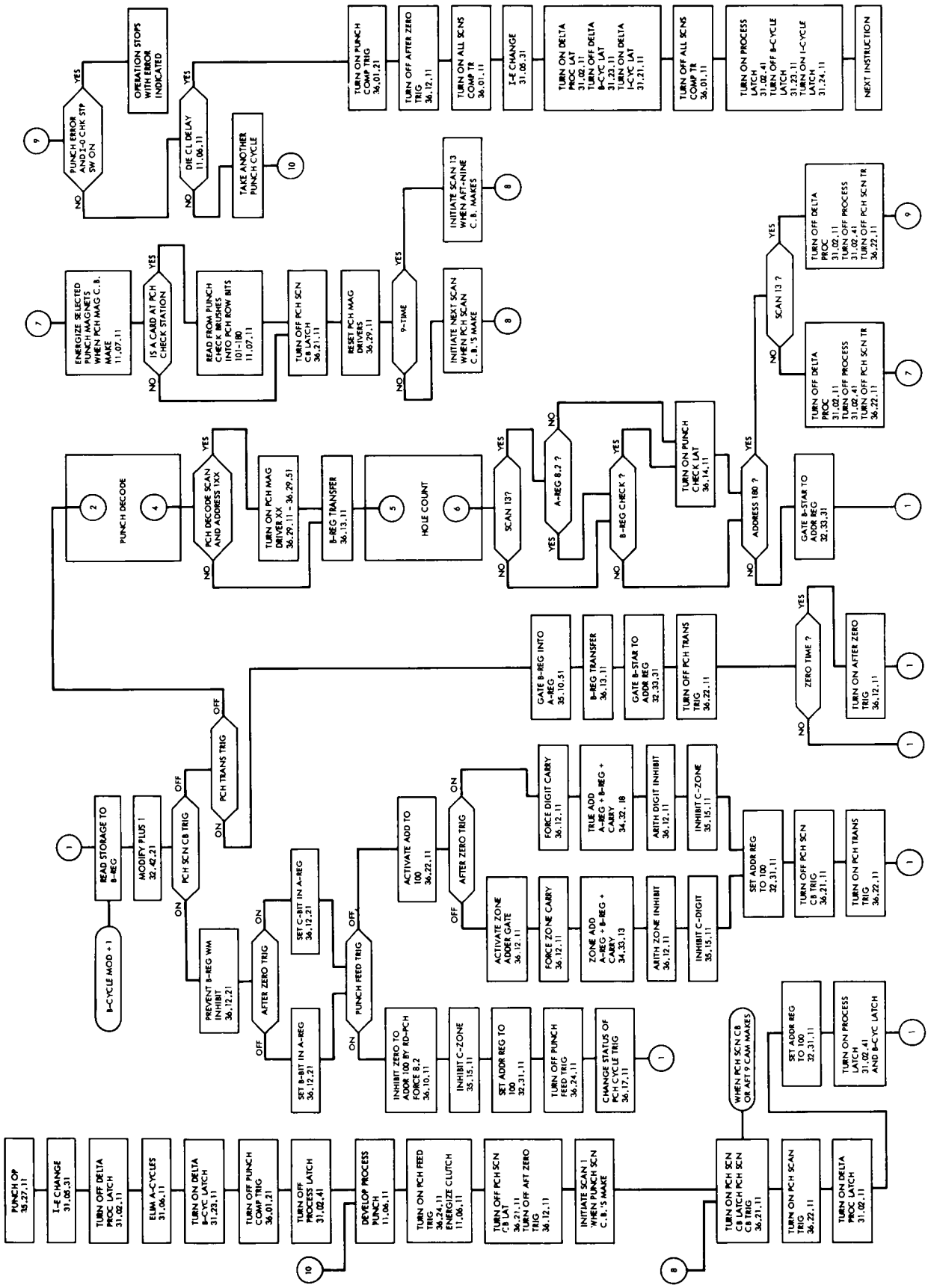
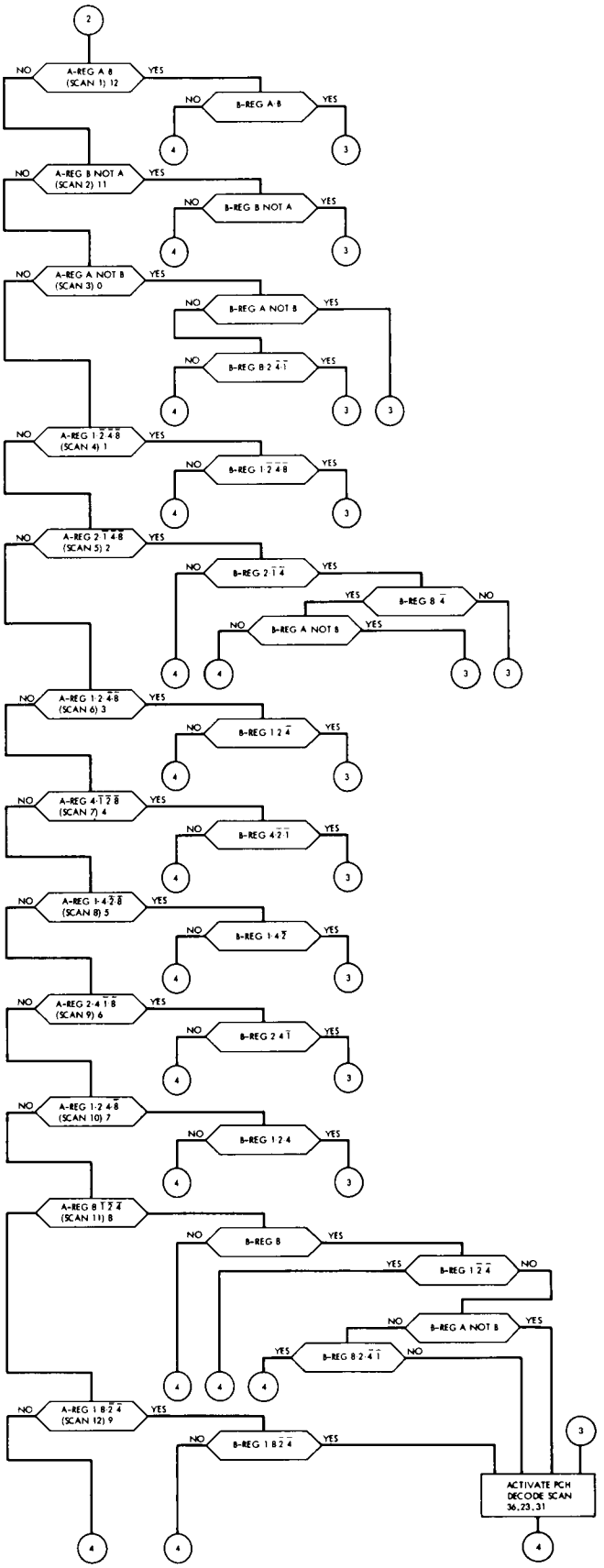


Figure 52. Punch Operation, Hole Count (Part 1 of 3)



BCD CODE						PUNCHED CARD CODE											
B	A	8	4	2	1	12	11	0	1	2	3	4	5	6	7	8	9
					1				1								
				2						2							
				2	1						3						
			4									4					
			4		1								5				
			4	2										6			
			4	2	1										7		
		8														8	
		8			1												9
		8		2				0									
		8		2	1						3					8	
		8	4									4				8	
		8	4		1								5			8	
		8	4	2										6		8	
		8	4	2	1										7	8	
	A							0									
	A				1			0	1								
	A			2				0		2							
	A			2	1			0			3						
	A		4					0				4					
	A		4		1			0					5				
	A		4	2				0						6			
	A		4	2	1			0							7		
	A	8						0								8	
	A	8			1			0									9
	A	8		2				0		2						8	
	A	8		2	1			0			3					8	
	A	8	4					0				4				8	
	A	8	4		1			0					5			8	
	A	8	4	2				0						6		8	
	A	8	4	2	1			0							7	8	
B							11										
B					1		11		1								
B				2			11			2							
B				2	1		11				3						
B			4				11					4					
B			4		1		11						5				
B			4	2			11							6			
B			4	2	1		11								7		
B		8					11									8	
B		8			1		11										9
B		8		2			11	0									
B		8		2	1		11				3					8	
B		8	4				11					4				8	
B		8	4		1		11						5			8	
B		8	4	2			11							6		8	
B		8	4	2	1		11								7	8	
B	A					12											
B	A				1	12			1								
B	A			2		12				2							
B	A			2	1	12					3						
B	A		4			12						4					
B	A		4		1	12							5				
B	A		4	2		12								6			
B	A		4	2	1	12									7		
B	A	8				12										8	
B	A	8			1	12											9
B	A	8		2		12		0									
B	A	8		2	1	12					3					8	
B	A	8	4			12						4				8	
B	A	8	4		1	12							5			8	
B	A	8	4	2		12								6		8	
B	A	8	4	2	1	12									7	8	

Figure 52. Punch Operation, Hole Count (Part 2 of 3)

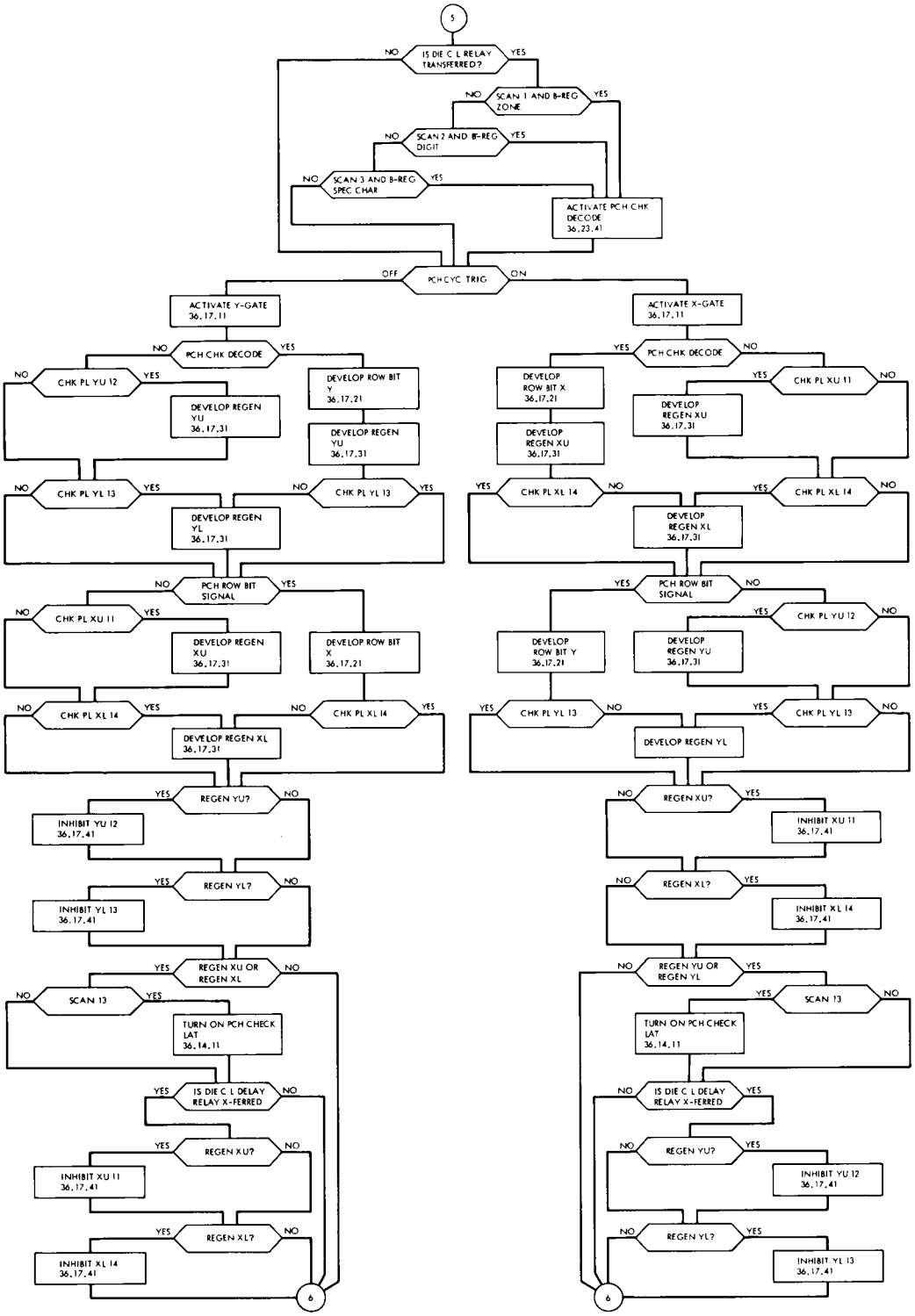


Figure 52. Punch Operation, Hole Count (Part 3 of 3)

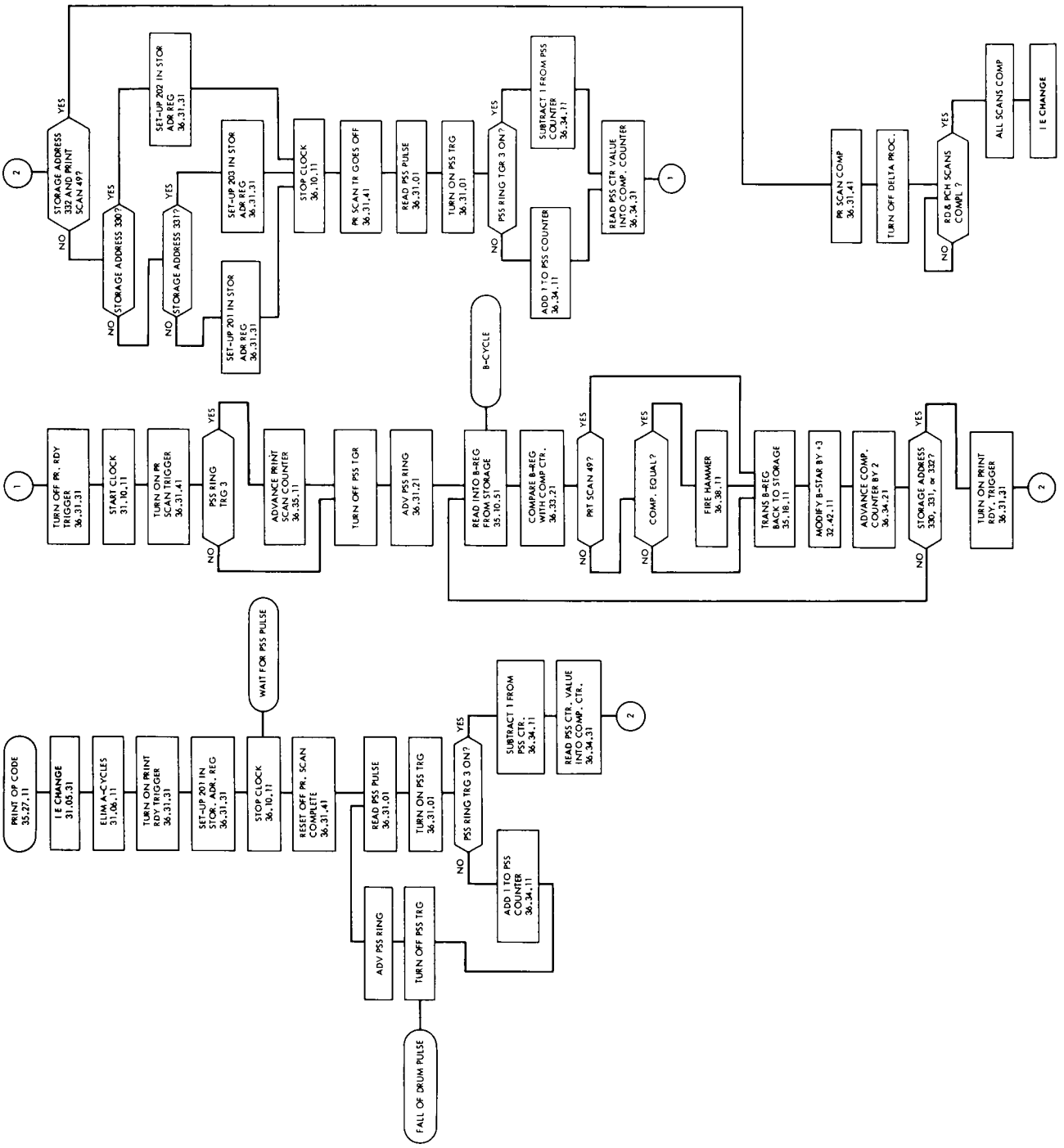


Figure 53. Print Operation

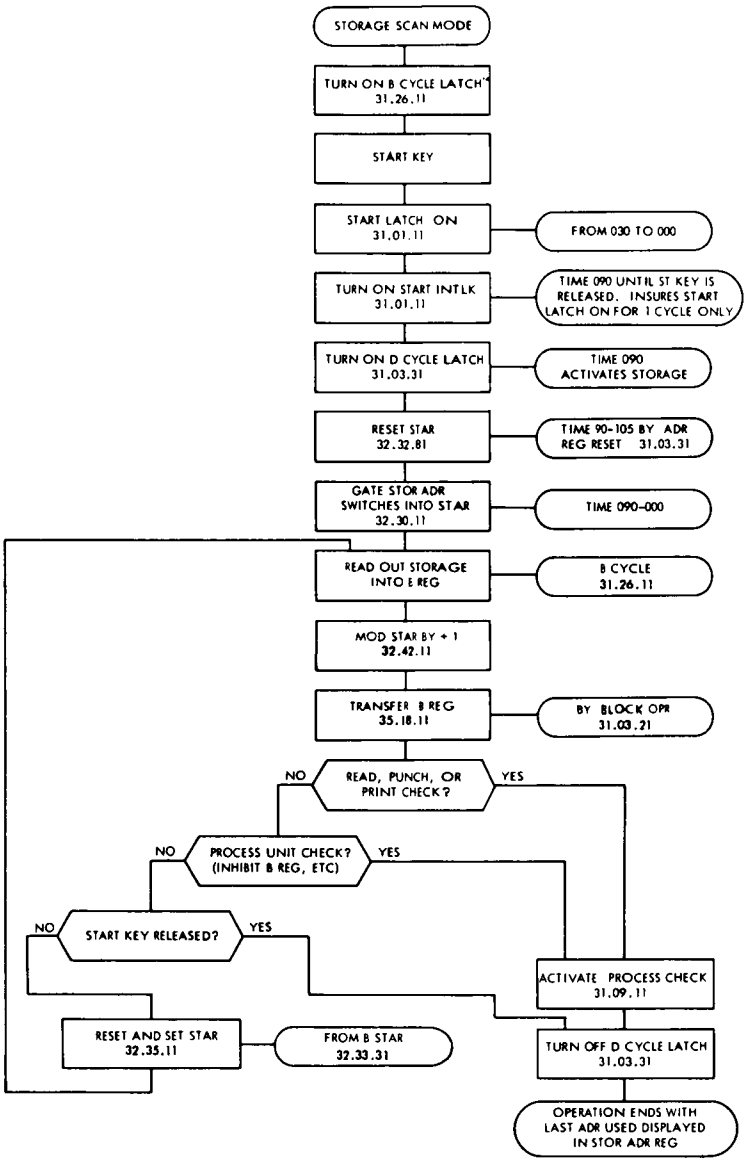


Figure 54. Storage Scan

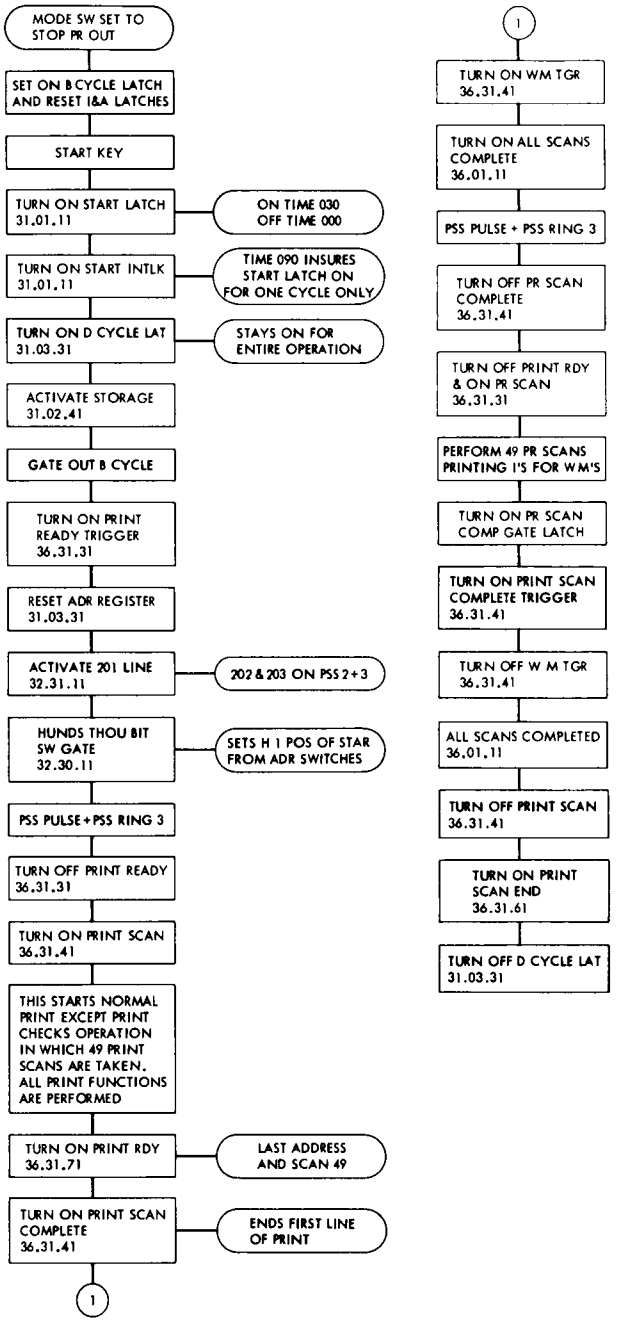


Figure 55. Storage Print-Out

Figure 56. Print Buffer Storage

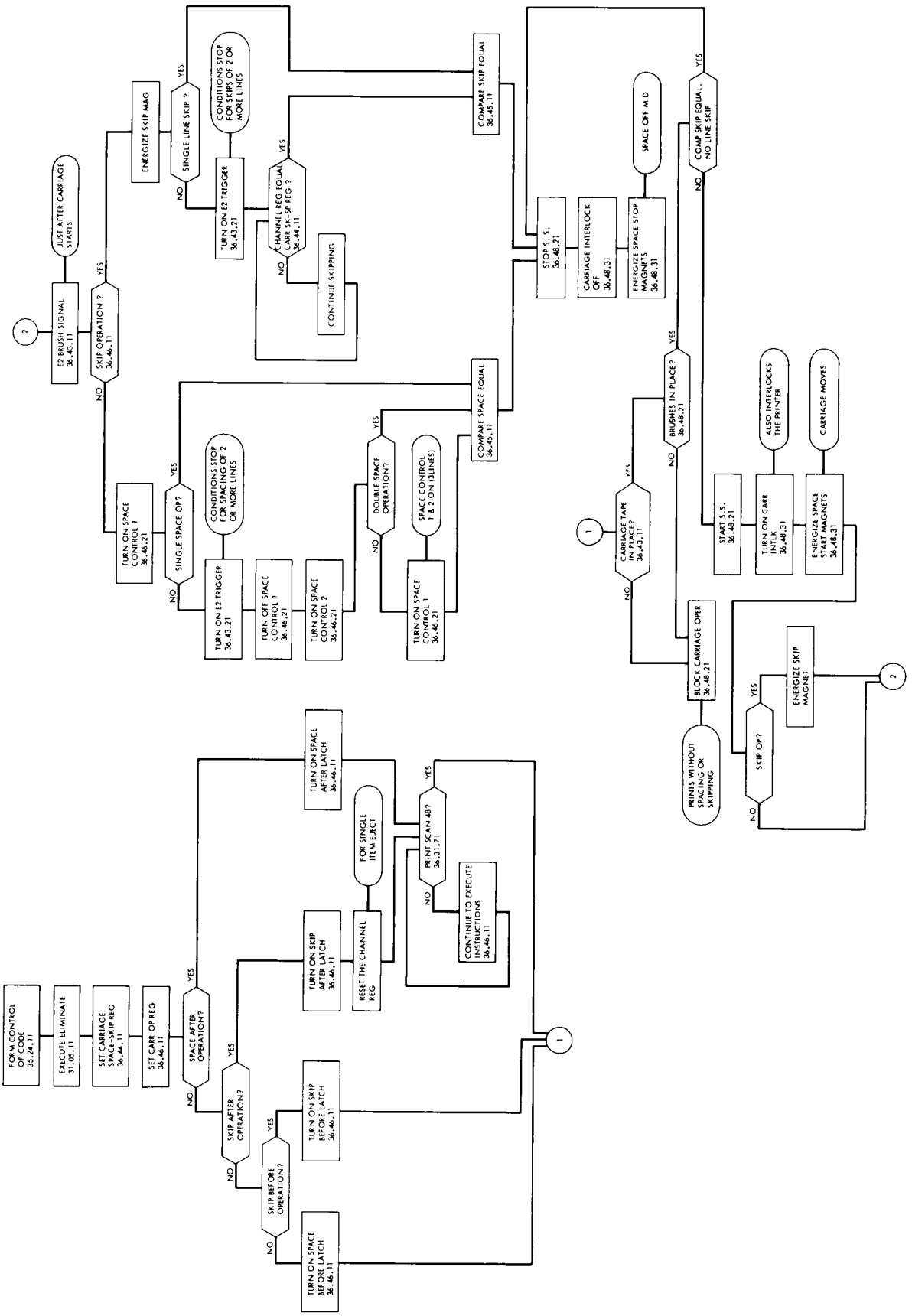


Figure 57. Forms Control

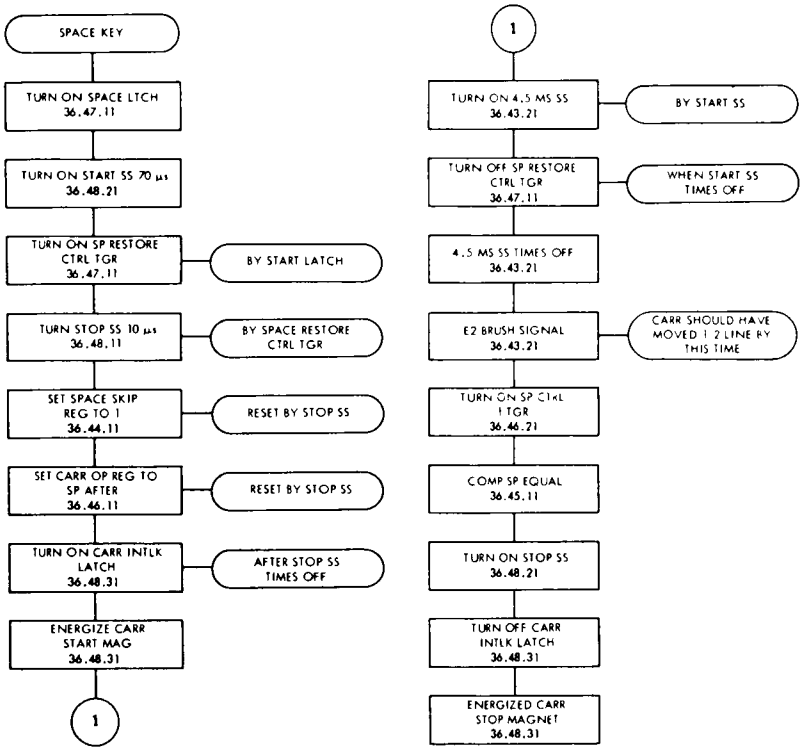


Figure 58. Space Key

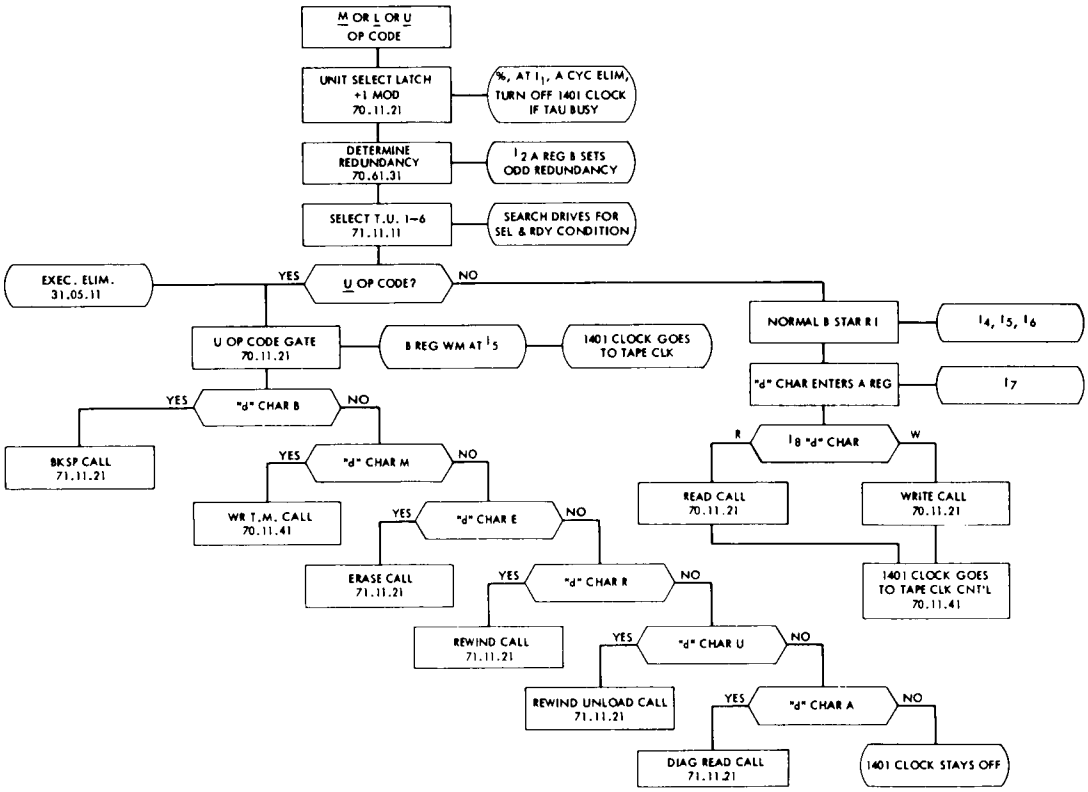


Figure 59. Move and Load Tape

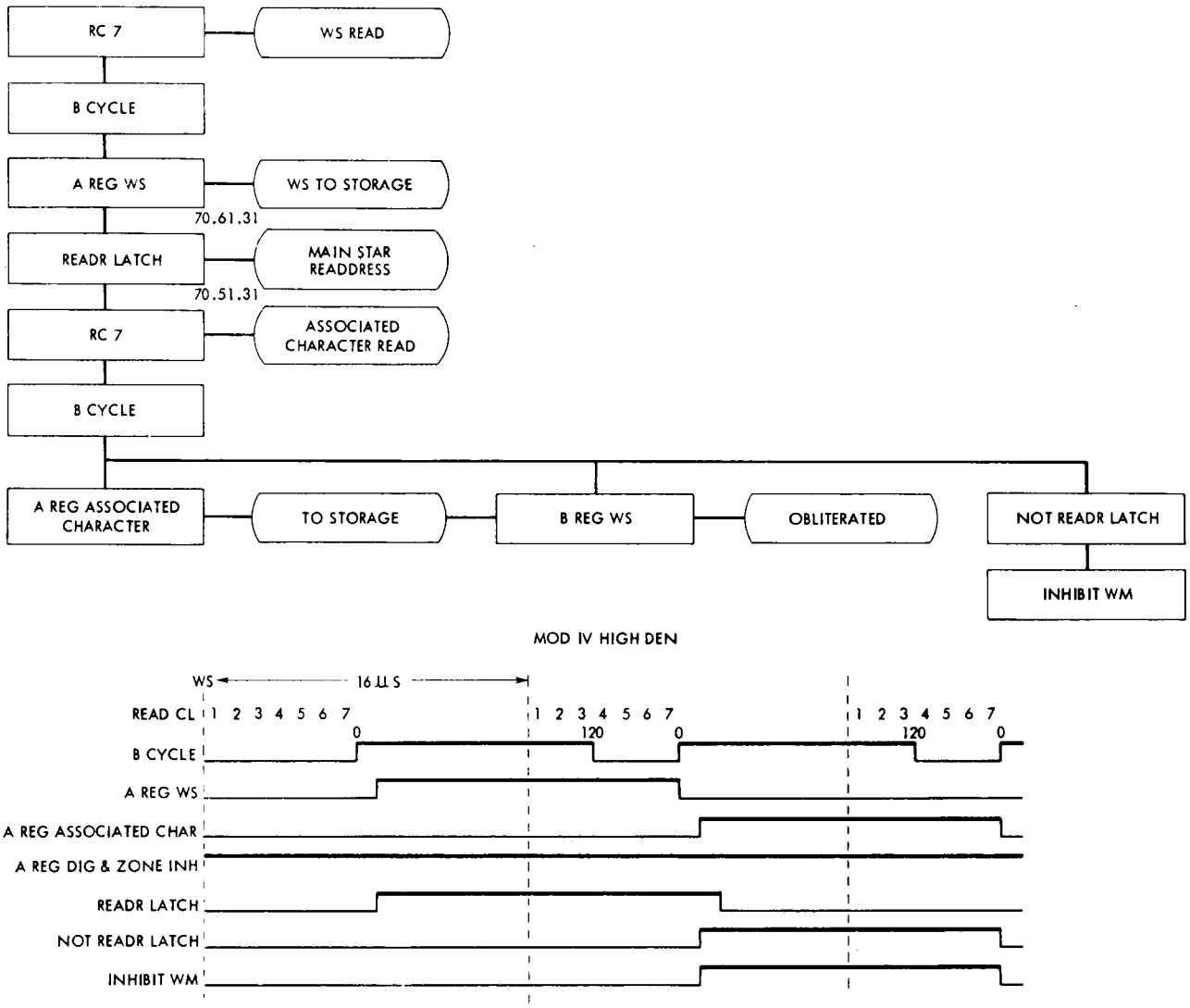


Figure 60. Load Read Tape

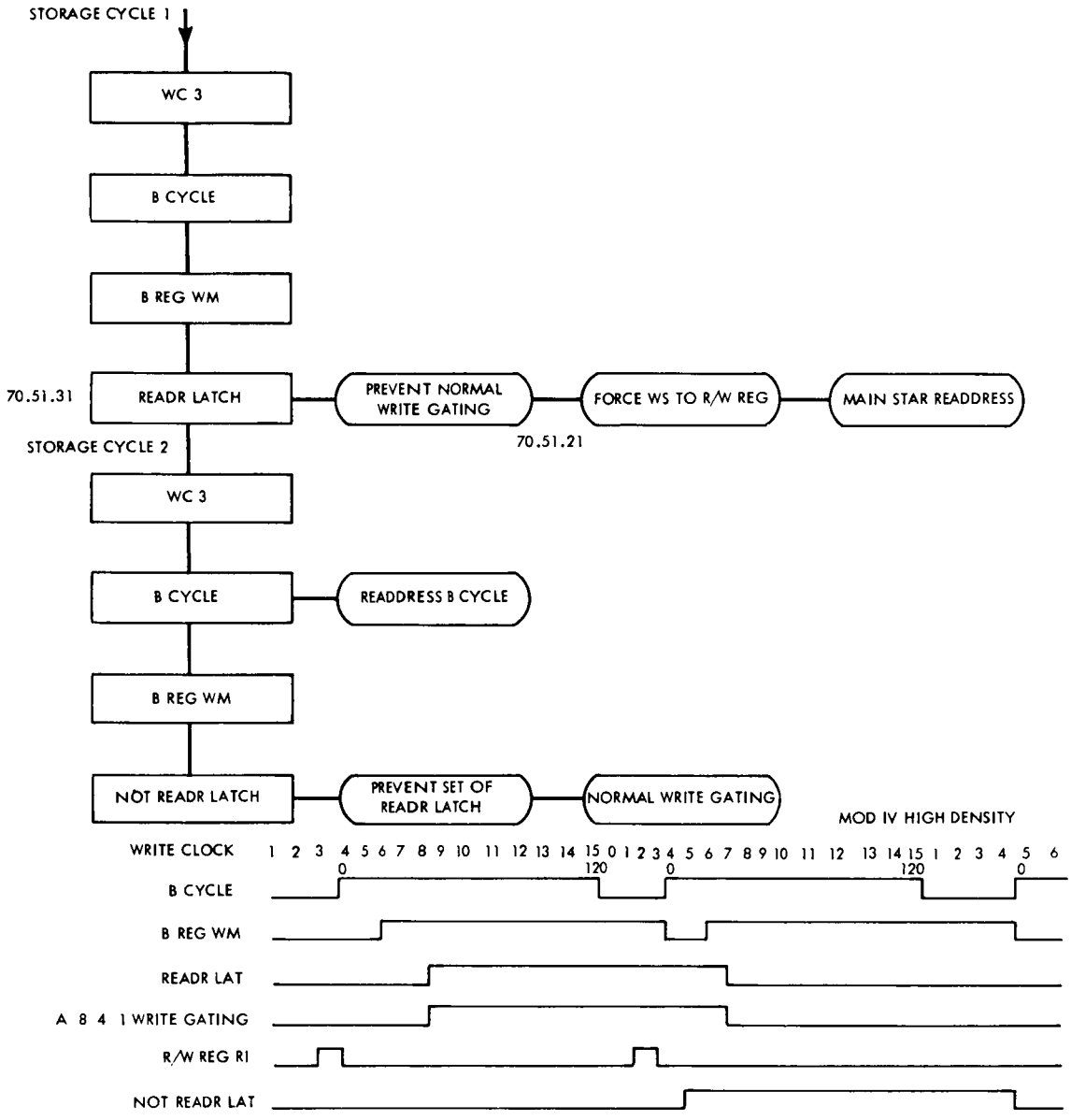


Figure 61. Load Write Tape

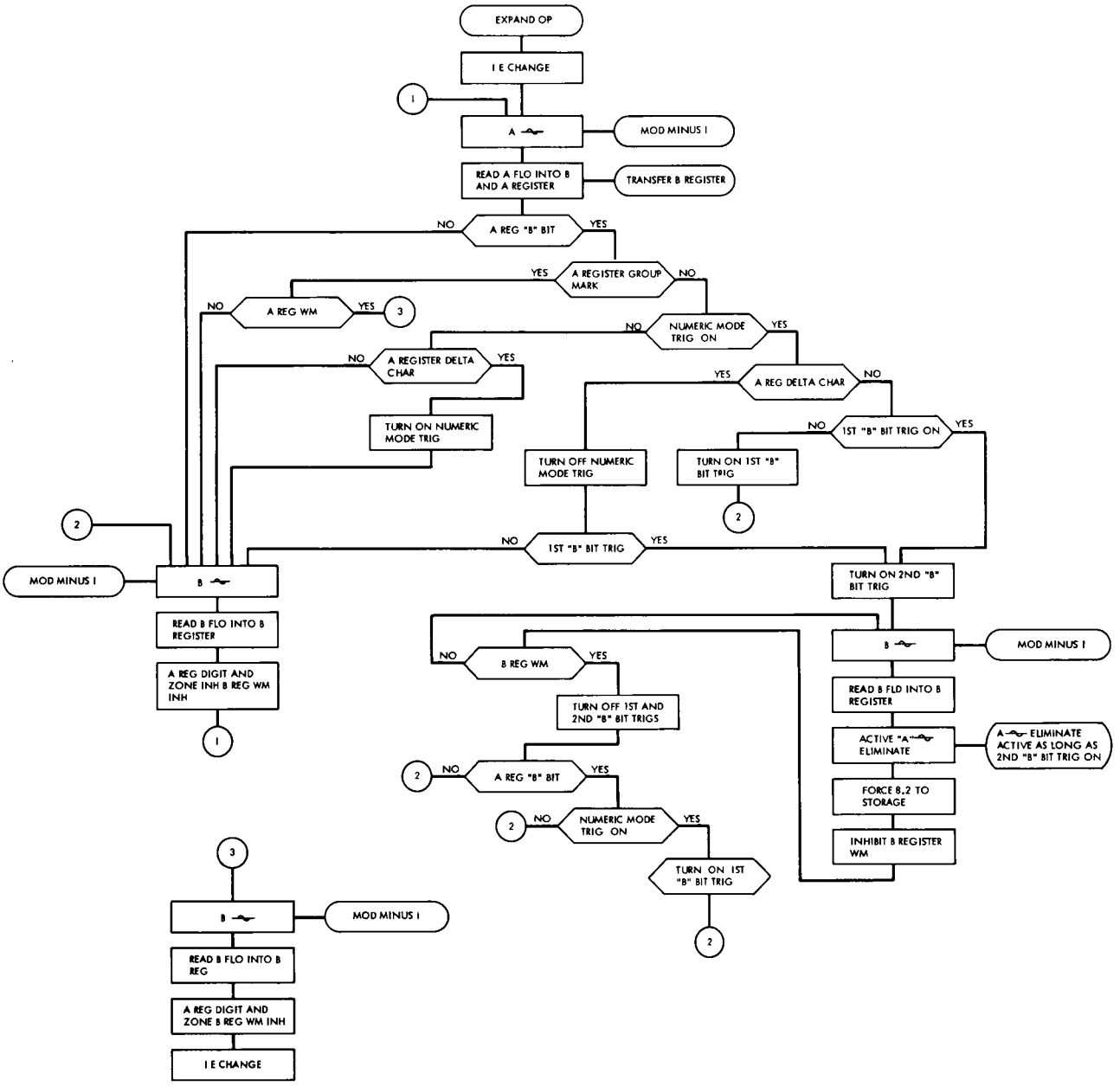


Figure 62. Expand Compressed Tape

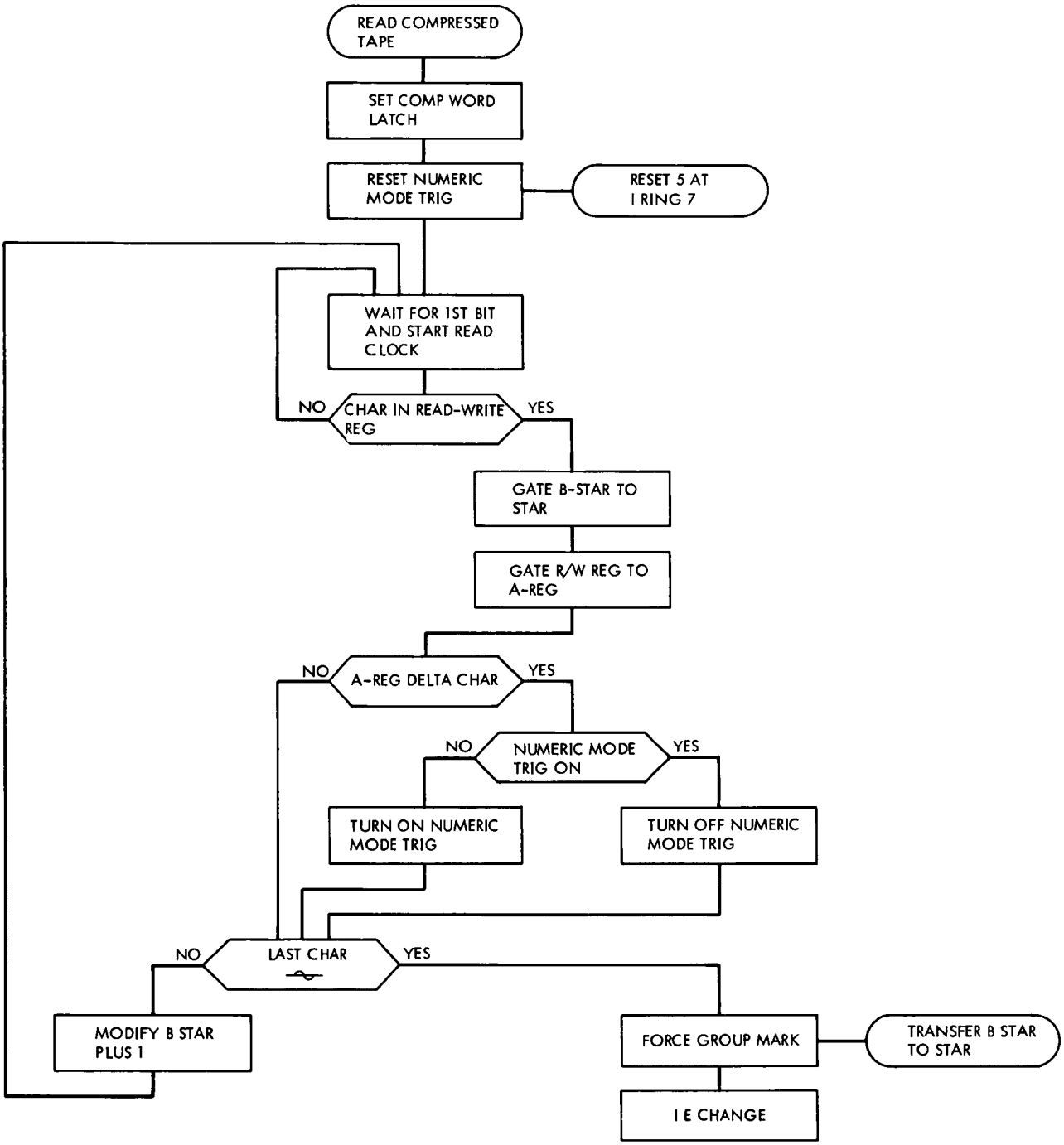


Figure 63. Read Compressed Tape

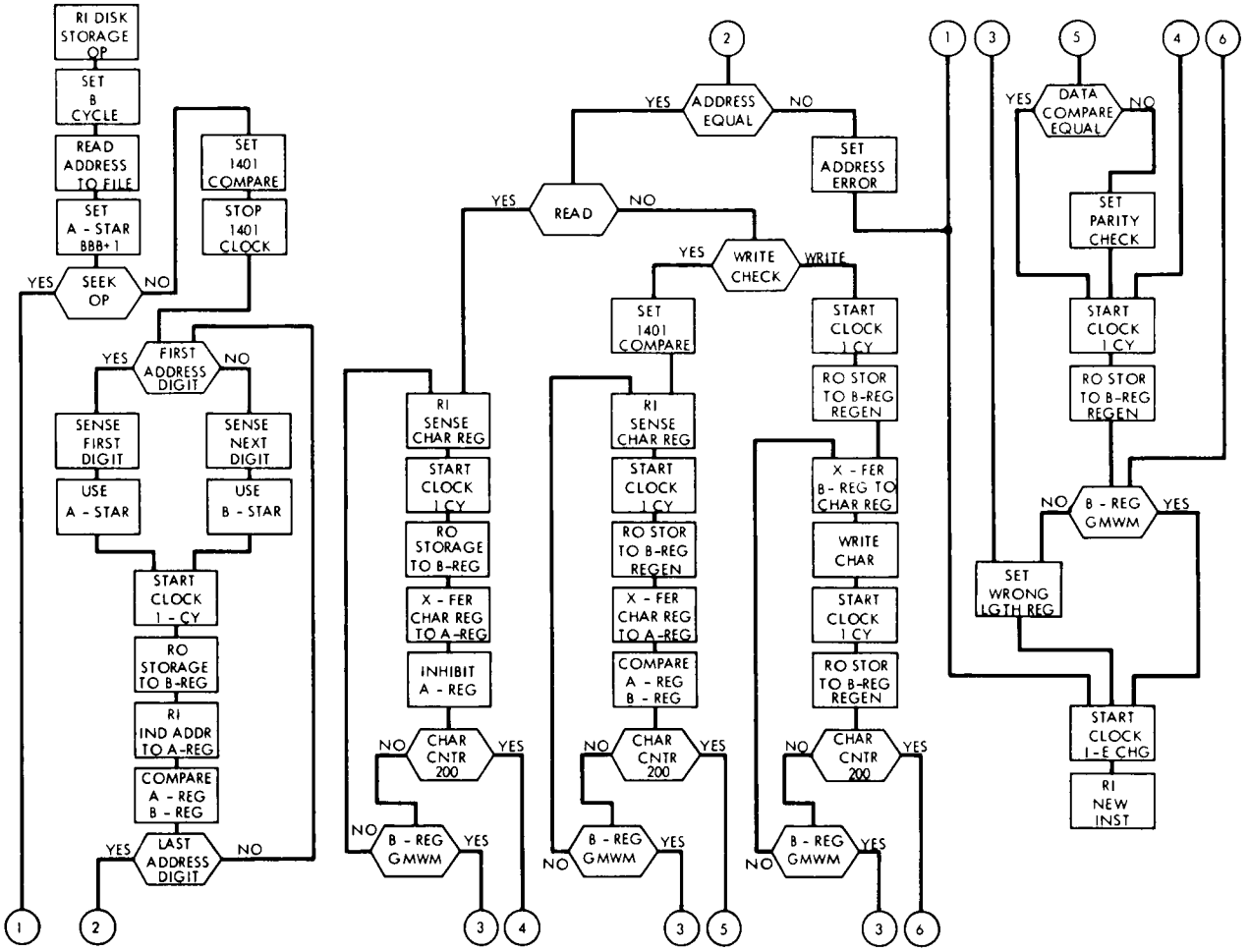


Figure 64. File Operation

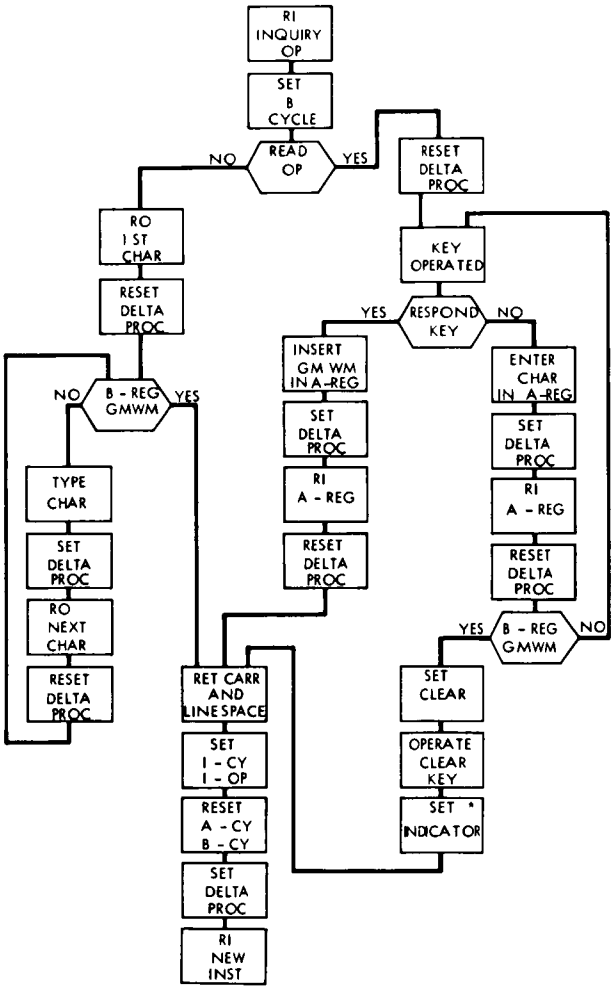


Figure 65. Inquiry Operation

General Service Hints

Diagnostic Procedure

Consult with the customer to determine what he has observed. Find out what the correct output should have been. See if he can demonstrate the failure.

Run the diagnostic function tests to see if they will fail. When they show the trouble, this is the best way to analyze the failure. If the machine does not fail, you must use accentuating methods: marginal checking, stopping blowers on gates, locking in program loops, etc.

When you get failures, compare correct and incorrect results, what tests failed, what effect varying data has, what is common to these results. Determine what unit of the machine is failing from this analysis.

Select and simplify the operation that causes failure; then lock the machine in a loop: switch B or D on diagnostic function tests, hand-enter the program loop, change the customer's program to loop, etc. Use the scope to trace down why your objective is not working. When you have determined where the trouble is, swap cards or substitute units to prove you are right.

D.F.T. on Tape

If you have a tape system, be sure to place the diagnostic function tests on tape soon after installation. Write the test tape and stop the program before rewinding. Unload tape, add a second load-point sticker, and rewrite the tests. This will give you a spare if one gets damaged.

The tests can be run from tape much faster than they can from cards.

Console Lamps

Burned out bulbs can cause circuit failures and be misleading in analyzing troubles from the console. Testing the bulbs also tests the error circuits. Tape console bulbs can all be lighted by grounding the jumper at the top of the panel.

Tape console lamps on TAU-2 machines make good sync points.

Muffin Fans

Fans should be checked at least once a week or on a service call. Some fans have been found to be running slow.

Thermal, Core

Power OFF can occur due to the thermal element in 01A1 opening because of a faulty fan or switch. This thermal should be checked at maximum two-month intervals for correct operation. This can be done by turning the power OFF and connecting an ohmmeter across the switch. Heat the element with a soldering iron and the meter circuit should open. This, however, does not determine the exact temperature setting at which the thermal element operates.

Clock Pulses

On intermittent and hard-to-analyze troubles, do not discount the possibility of incorrect levels or timing pulses from the clock. These pulses are very critical and should be checked at the edge connectors on their source chassis.

Observing a Latch Set Pulse

It is difficult to determine what sets a latch. When it latches back, the set line is up solid. The following procedure can be used to observe the set pulse to the latch:

Remove the card with the latch reset pin on it. Using an extender, remove the reset line, and tie the reset input pin on the card to the reset voltage level. This will prevent the latch from latching back, and therefore, enable the set pulse to be scoped easily.

CAUTION: Do not use this procedure on the print reset check latch unless the print area has C-bits only.

Example: A WM latch 31.06.11 3B-4B
Extend the card at 4B. Remove the wire on pin C and connect pin C to +6v.

SMS Voltage Shunt

The following service techniques help save scoping time and point out what to look for when tieing lines to voltages.

Figure 66A shows typical +A block. Notice extender input pin G goes directly to the base of the transistor. Scoping this point alone tells whether the block is switching or not. This saves scoping of inputs D, E, and F. This is especially helpful when a number of

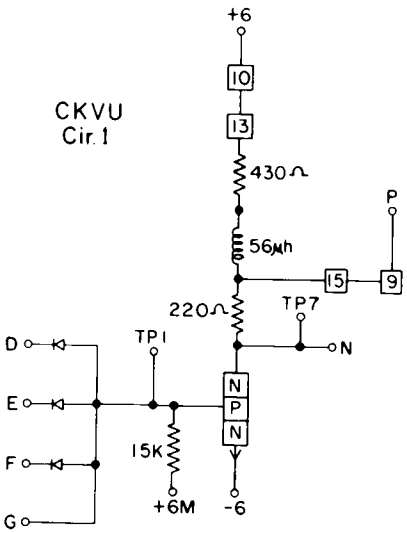


Figure 66A. +AND Voltage Shunt

blocks are dot-ORed together to determine which one is switching. If the block does not have extender input, an appropriate test point can be used. In this example, it would be TP1.

This block can safely be tied on. If output pin N is jumpered to —6v, the transistor is safely shunted out of circuit and no damage results. If pin N was jumpered to +6v, load would be shunted and a total of 12v would be across the transistor. With no current limiting the load, the transistor would burn out.

Figure 66B shows —A followed by a DE. The —A block can be tied ON but not tied OFF for the same reasons explained in the example. Notice the DE block following it is just the reverse. Output pin A can be tied to —12v, not to ground. The 20-ohm resistor in the collector circuit is negligible.

If the DE block is a high-speed one with diode from emitter to base (Figure 66B), it would not be safe to

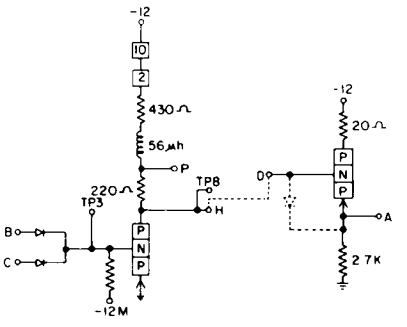


Figure 66B. —AND to DE Voltage Shunt

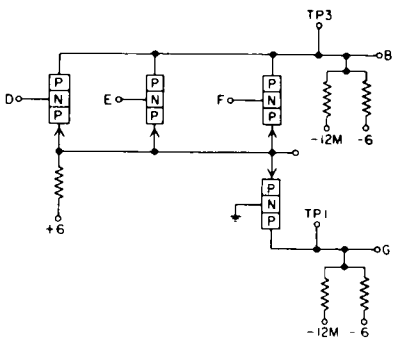


Figure 67. Current Mode Voltage Shunt

tie it OFF because of the possibility of destroying the preceding block.

Triggers can be tied ON or OFF. For example, the CW trigger can be tied ON by jumpering pin E to ground, and it can be tied OFF by tieing pin H to ground.

The foregoing refers to CTDL circuitry. Using extender to isolate circuitry, the following suggestions can be safely used in both CTDL and current mode. Placing a card in the extender and removing the input lines safely removes the preceding blocks from the circuit. Inputs can then be jumpered to the appropriate voltage to turn the block ON or OFF.

In current mode, swing is nominally ±0.8 volts; however, it is safe to tie isolated inputs to appropriate gate voltage. For example, in Figure 67, which is typical —0 or +A with U-line inputs, isolated input pins can be jumpered to 0v or to —12 volts.

Use proper probes and leads. Safe jumper wires and sync leads can be made by using terminal P/N 364471. As added precaution, the terminal on the end of the lead or jumper should be insulated with plastic electrical tape to prevent shorting between pins.

CAUTION: Securely fasten sync leads to scope the sync terminal before placing the other end of the SMS card pin. A sync lead coming loose at the scope can touch the scope case and ground out, possibly resulting in a destroyed card.

CE Panel Diodes

The diodes on the CE panel can be used as extender diodes for any AND switch or driver emitter in the 1401 (systems above 20000). For a —AND, use diodes on the right, and tie the common point to the base of the transistor in the AND block used.

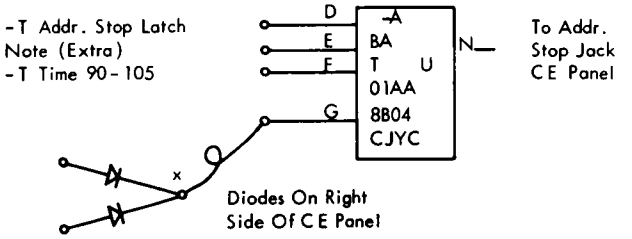


Figure 68. CE Panel Diode Wiring

Examples: 32.45.31.2 (Figure 68).

The diodes do not have a load resistor, nor are they tied down to any voltage. Therefore, they cannot be used as independent AND/OR circuits unless loading is provided.

Component Testing

Most defective components can be located by using an ohmmeter to check for an open or shorted condition. Be sure to consider parallel components when testing with an ohmmeter. An excellent method of determining the correct readings is to compare the readings of an identical, good card with those of the defective card.

The transistor is considered as a back-to-back diode. Check the forward and reverse resistance of each diode with an ohmmeter adjusted to $\times 100$ ohm scale. The forward-to-reverse resistance ratio should be 10. Emitter-to-collector resistance should be the same as the reverse resistance (Figure 69).

MINIMUM INPUT VOLTAGES TO CONTROL TRANSISTORS

C, V and Z Lines Undefined

AND's and OR's
Plus N 0.4 Minus N -0.4
Plus P -5.6 Minus P -6.4
Plus R 5.6 Minus R 0.2
Plus S -0.2 Minus S -5.6
Plus T 1.4 Minus T -0.7
Plus U -5.3 Minus U -7.4
Plus Y -0.6 Minus Y -5.8

CW and JZ Triggers
Plus T 1.4 Minus T -0.7
Plus U -0.5 Minus U -7.4

AR and AS Triggers
Plus S -0.2 Minus S -5.6
Set Pulse 2.6 Volt Shift

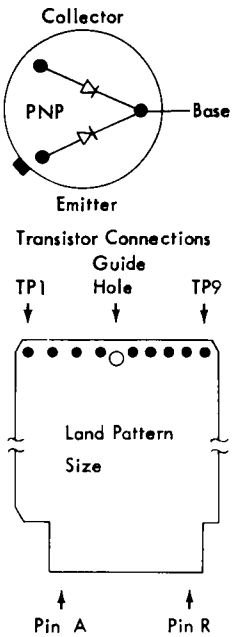


Figure 69. Transistor Connections

Test diodes with an ohmmeter in the same way transistors are tested.

OPEN COLLECTOR LOAD EFFECTS

Generally speaking, open collector circuits have the effect of removing the circuit control from the following stage.

External circuit connections to the logic block can sometimes provide a load resistance for the block when its own load resistor opens. This produces a weak output from the block and can produce highly intermittent failures that are hard to analyze.

The only positive method for checking the load resistor is to remove the output connection on the unit, either by taping the pin or using a card extender. The unit still switches correctly with the output disconnected if the load resistor is good.

Field Replacement SMS Cards

FIELD INVENTORY REDUCTION

Twenty-one field replacement cards, which are capable of replacing 122 standard production cards (Figure 70), are now supplied on 1401 initial spare parts orders. The flexibility of field replacement cards allows the stock of standard cards to be reduced, yet provides the the same number of card types.

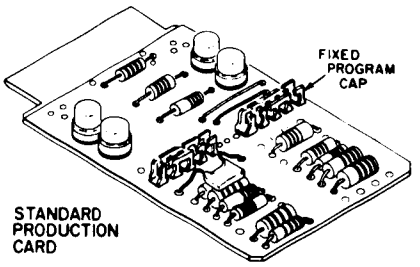


Figure 70. Standard Production Card

DEFINITION

A field replacement card (Figure 71) is a multipurpose card especially engineered for field use and contains a new *barrel-type* program receptacle. By manual pro-

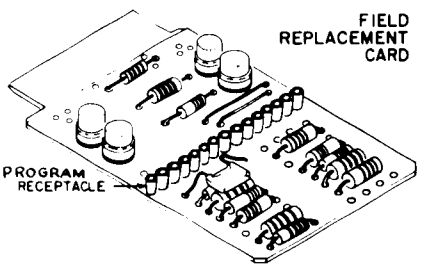


Figure 71. Field Replacement Card

gramming (plugging a contact strip into the receptacle), one card substitutes for 3 to 14 types of standard production cards. The contact strip, P/N 216259, is a group of 17 tapered plugs connected by a common strip.

USE

Programming a field replacement card is made easy by a new cap kit, B/M 451271. The kit contains simple step-by-step instructions, card indexes, which identify the field replacement card to use for a standard card, and templates. The templates are cut out to fit over the program receptacle and make programming a card practically foolproof. The following are the primary steps for using the kit, contact strip, and field replacement cards:

1. Refer to the kit index to find the part number of the field replacement card that can replace a troublesome standard card.
2. Select the proper cap-code template from the kit and place it over the program receptacle of the field replacement card.
3. Using a pair of diagonals, cut the contact strip, P/N 216259, according to the template pattern and insert the contacts into the receptacle, finger-tight.
4. Double-check the strip against the template pattern, remove the template, and insert the strip into the receptacles, using longnose pliers. Bend the common bar back.

The field replacement card is now ready for use as shown in Figure 72.

Note: Field replacement cards are authorized for use on 1401 systems and are now included on the initial spare parts lists. IBM Mechanicsburg cannot substitute field replacement cards for standard production card orders.

SMS Service Pointers

A CTDL single-shot card can be used to provide a delay for the 310 scope. Two SMS cards are available,

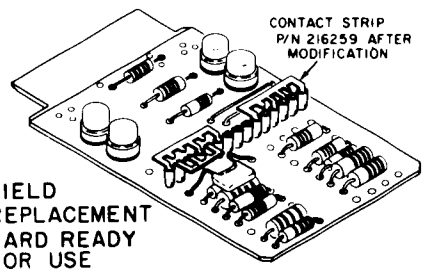


Figure 72. Field Replacement Card

one for +U lines (NC—, 371592) and one for —T lines (NB—, 371591). These cards will provide delays between 7.5 microseconds and 90 milliseconds. They can be plugged into any wired location.

CTDL triggers can easily be flipped by grounding one or the other of the output pins to aid in scoping circuits.

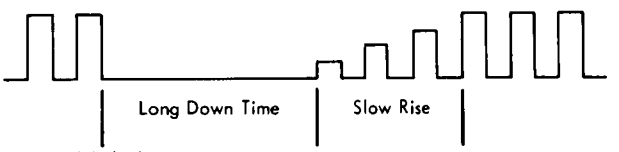
Care must be used when cleaning SMS card contacts. If the lubricant comes in contact with the clear plastic coating on the component portion of the card, the solvents in the lubricant can dissolve the plastic coating, which will act as an insulator if rubbed on the contacts. The following steps should be used to clean the contacts:

1. Apply the lubricant either directly to the contacts or indirectly by saturating any lint-free cloth or tissue.
2. Clean and lubricate the contacts by wiping with a moistened cloth from the leading edge toward the component section of the card.
3. Rub the contacts with a clean piece of cloth until there is no visible trace of lubricant. The cloth will darken if the contacts have not been properly cleaned.
4. Repeat the steps, if necessary, until the contacts are clean.
5. If you suspect that the contacts have been contaminated with the coating used on the back of the card, rub a pencil eraser over the contact. The clean contact will be bright, and the contaminated area very dull.

SMS back-panel wires are frequently routed around but not attached to an intermediate terminal. If the wire is pulled too tightly, or if undue pressure is exerted at the point of contact with the intermediate terminal, insulation damage or "cold flow" may result, shorting the wire to the terminal. This possibility should be considered when diagnosing hard-to-analyze troubles.

All removed SMS cards must be returned to the plants for analysis. Field return envelope, Form 920-8137, should be completed by the customer engineer for each SMS card replaced.

Many timing pulses are not square as one would believe. If trouble is encountered, square up the pulse as much as possible with card substitution. If trouble still exists, leave timing pulse and pursue other possibilities. *Sliver pulses* (very short pulses) that can flip triggers can be developed by slow transistors. Very close observance of scope pulses is needed to observe the presence and cause of these.



a. Works fine on core worst pattern.
b. Fails on some tape operation.

Figure 73. STAR Output Rise Time

Slow rise or fall after a circuit has been in one state or another for a long period should be considered on intermittent failures.

Example: Outputs of Main-star (Figure 73)

1. Works fine on core worst pattern.
2. Fails on some tape operation.

Voltage variation on the system varies the transit time of weak transistors. Use it to accentuate failures because of switching noise or timing.

Error Retention or Error Stop

A CTDL trigger (CW—PN 371543) installed in any spare socket can be used as an error- or condition-retention device by proper wiring of the set and gate pins. Because voltage wiring is already in place, many applications require only two jumper wires to turn on the trigger. In other cases, additional wiring and an additional card may be necessary to cause the proper condition to turn on the trigger.

The trigger output can be left unwired for interrogation by scope or can be jumper-wired to cause a machine stop.

In some cases, localizing the cause of an error can be retained by using a jumper wire and a diode from a given error latch to reset the delta-process latch. This prevents the machine from advancing to the next program step, and thereby preserves the machine conditions when the error is sensed.

Single-Cycle Mode

Many troubles do not allow you to set up a program loop and have to be approached in single-cycle mode. Although some troubles can be analyzed statically, many involve cycle or time controls.

When scoping in single cycle, use the delta-process latch rather than the start key as a sync. It is more stable.

To prove that a given block conducts, set up the scope as follows: + or — internal, depending upon the output level of the line you are checking, that is, + for a +U output. Set time/div. in the ms range, and stability to stop the trace from free running. Turn the intensity control to get a spot on the screen. Set the vertical amperes to keep full range on the scope face. With the vertical input probe free, adjust the trigger level so that as you move the vertical-position knob up or down (up for a +output), you get a sweep at a few volts less than the maximum of the line you want. Return the vertical-position knob to the base line, and connect the vertical probe to signal line. As you single-cycle to the point of failure, look for a trace on the scope. The slower the sweep time, the better the chance to see the sweep.

Branch-on Error

To facilitate checking the branch-on I/O error without running the reader, punch, printer, or tape; tie the error trigger or latch to its ON condition and run the branch program. These circuits can then be checked at 1401 speed.

Logic Errors

When troubleshooting logic or arithmetic errors, the B-field is usually altered and extra program steps are necessary to restore the B-field. For a tight loop, force a block operation as in single-cycle non-process in the run position. This insures the digit configuration remaining the same in a very tight loop. It can be checked in logic 31.03.21.

Repeat Cycle

Preventing the 1401 from advancing to the next cycle and repeating the same cycle can be useful when shooting main-frame troubles. The procedure is done by bringing up modifier control transfer and preventing the cycle latches from resetting. The program must be single cycled to the cycle preceding the cycle that is to be locked. The jumpers must be connected with power ON and the mode switch set to RUN. The start key then starts it looping. The circuits that have to be altered can be found on logics 32.44.31 and 31.20.11.

Repeat Instruction

To set up the 1401 so a single instruction can be repeated indefinitely without an intervening branch, the load latch can be forced on at the end of E-phase. The op code of the instruction to be repeated must be in 001. The load latch forces 001 into the address register, and then goes to 001 for the instruction. When errors occur that prevent a loop of the 1401, the error indication can also be used to turn on the load latch. The error indication always occurs after the error, so the circuit can be readily scoped. It may be necessary to prevent the 1 from being placed into the operation register.

Single Load

When a circuit is analyzed, sometimes multiple cards are tied to a single load card. Cards cannot normally be pulled to isolate the circuits. By adding a 500-ohm resistor, any card can be made a load card by tieing the output pin to the same voltage as the load card through this resistor. All cards in the dot function can now be pulled for isolation. CAUTION: Anytime a card or connector is pulled or inserted, power should be turned off.

Bias Checking

Always use a meter when bias checking. If the 3v buckboost rheostat is turned ON (or if the plug is not in a socket when power is turned ON or OFF), the circuit breaker for the marginal voltage can trip and no voltage indication is evident.

IBM 1402 Reader-Punch Service Hints

Reader Error Diagnosis

When analyzing reader-error conditions, refer to Figures 20, 74, and 75 for a quick recall on the functions of the error indicators and the possible causes for being set.

Checking Speed of I/O Units

The following procedure allows a check of the speed of the card reader, punch or printer on the 1401 system:

1. Set the bit switches on the lower console panel to the desired op code plus WM.
2. Enter this bit configuration into the entire storage area by using the enter key in storage-scan mode.
3. Select and record starting address, then alter Mainstar to this address.
4. Allow the 1401 to perform this operation for exactly one minute.
5. Stop the 1401. The difference between the starting address and the one now in I-Star is the number of operations performed.

Example:

Run Punch OPS in 1 minute	
Address at Stop	1250
Address at Start	1000
Speed of Punch	250

Read Checking

An anlysis of read checking follows. Use it as a review or for reference.

Because two cards are being read simultaneously (one at first read and one at second read), provide duplicate sets of check planes and associated circuitry (Figures 76 and 77).

An alternate-cycle trigger alternately brings up the X-gate and the Y-gate in the following manner (Figure 76).

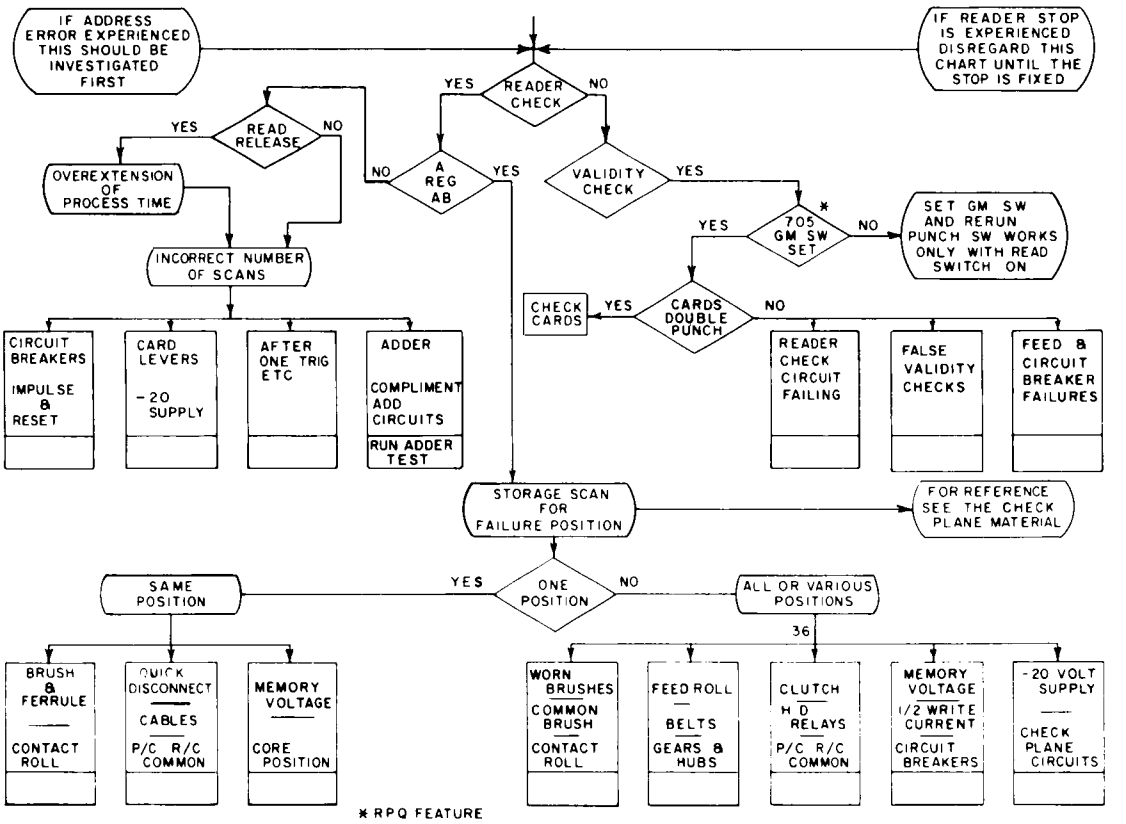


Figure 74. Reader Check Flow Chart

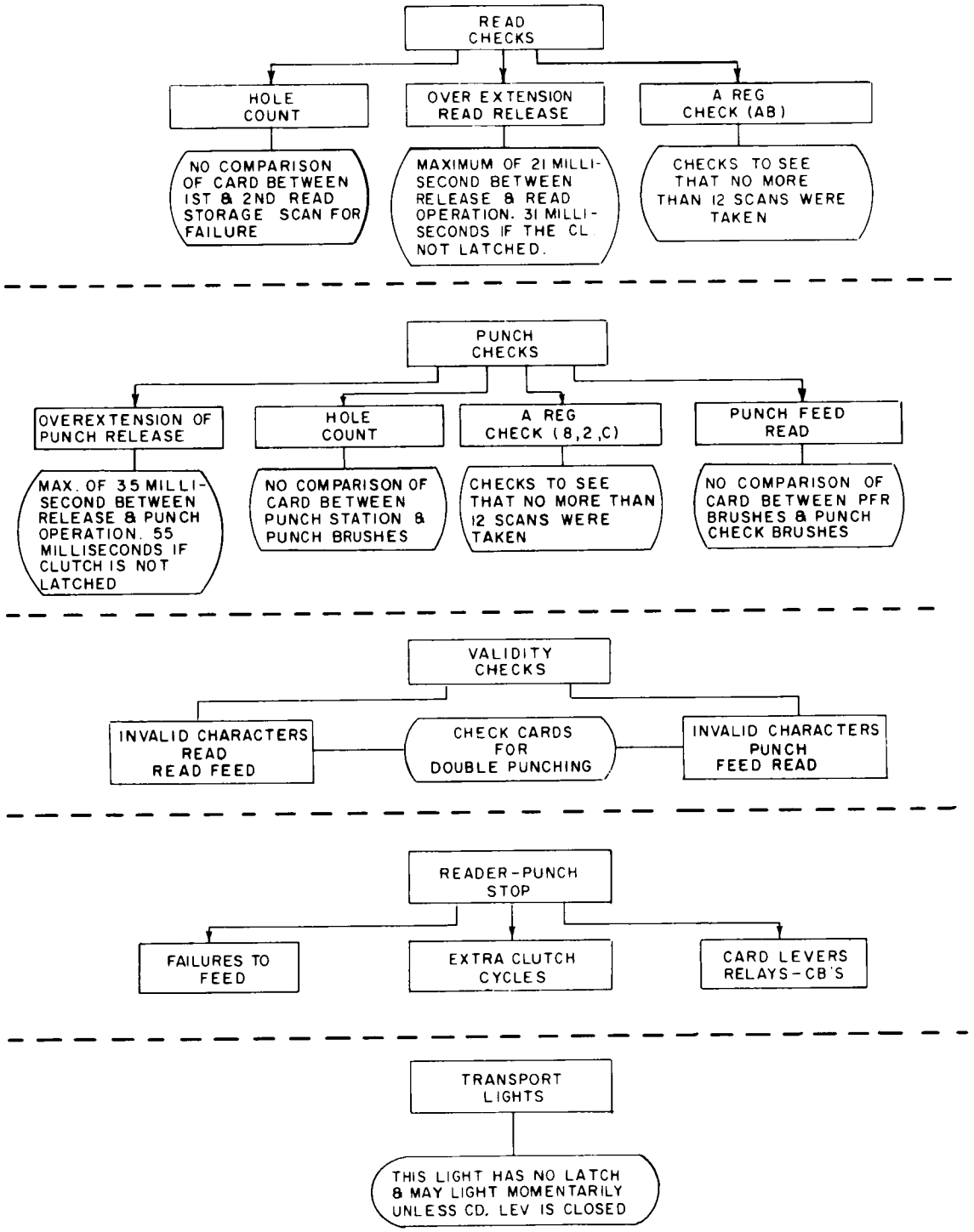


Figure 75. IBM 1402 Error Light

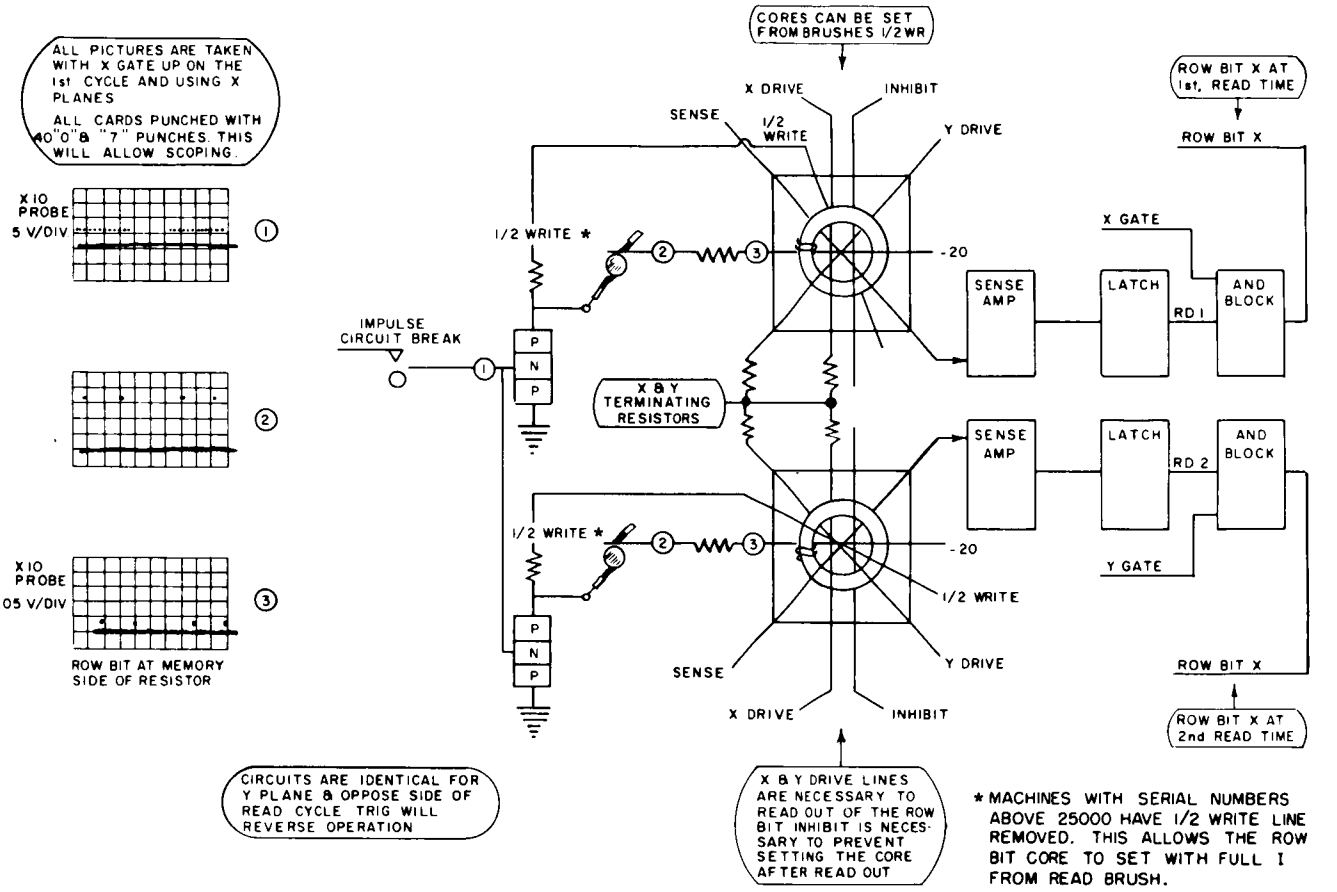


Figure 76. Row Bit Composite

There are two sets of X planes (X_u and X_L) and two sets of Y planes (Y_u and Y_L). If a card enters first read while the X-gate is up, it is checked by the X_u and X_L planes. If it enters first read while the Y-gate is up, it is checked by the Y_u and Y_L planes.

To simplify analysis, let us follow one card through first and second read. Let us further assume that the X-gate is up when it passes first read. It follows then that the Y-gate will be up when the card passes second read.

Analyzing the following piece of logic, we are concerned only with RBX (Figure 77). A core will be set in the X_L 14-plane the first time a row bit is sensed and will be regenerated until a second row bit is sensed (Figure 78). If a card has one punch in a particular column, the core in the X_L plane at the address corresponding to that column will be set to 1 on the scan in which the RBX is sensed. Each time this position is addressed on succeeding scans, it will be regenerated until another RBX is sensed. With one punch in the column, this would occur when the hole was sensed at second-read brushes.

A multipunched column results in the core in the X_L plane being set to 1 on sensing the first RBX. On sensing the second RBX, it is prevented from regenerating, returning the core to 0. A third RBX sets it to 1 again. Thus, the X_L plane alternates between 1 and 0 for each hole read. Because it is read at both read stations, it always ends up at 0.

The X_u plane is gated differently than the X_L plane. Note the following piece of logic (Figure 77). For any punched column in a card, the first hole that is read results in the corresponding X_u core being set to 1. Also, the core is regenerated each time it is re-addressed while passing first read. This is true whether a particular column has one or more holes. When the card is passing second read and the Y-gate is up, the core continues to be regenerated until an RBX is sensed. No further regeneration can then occur.

Summarizing this, the following conditions are true during proper operation:

If the X-gate is up when the card passes first read, the Y-gate is up when it passes second read.

For each hole read at first and second read, an RBX is sensed.

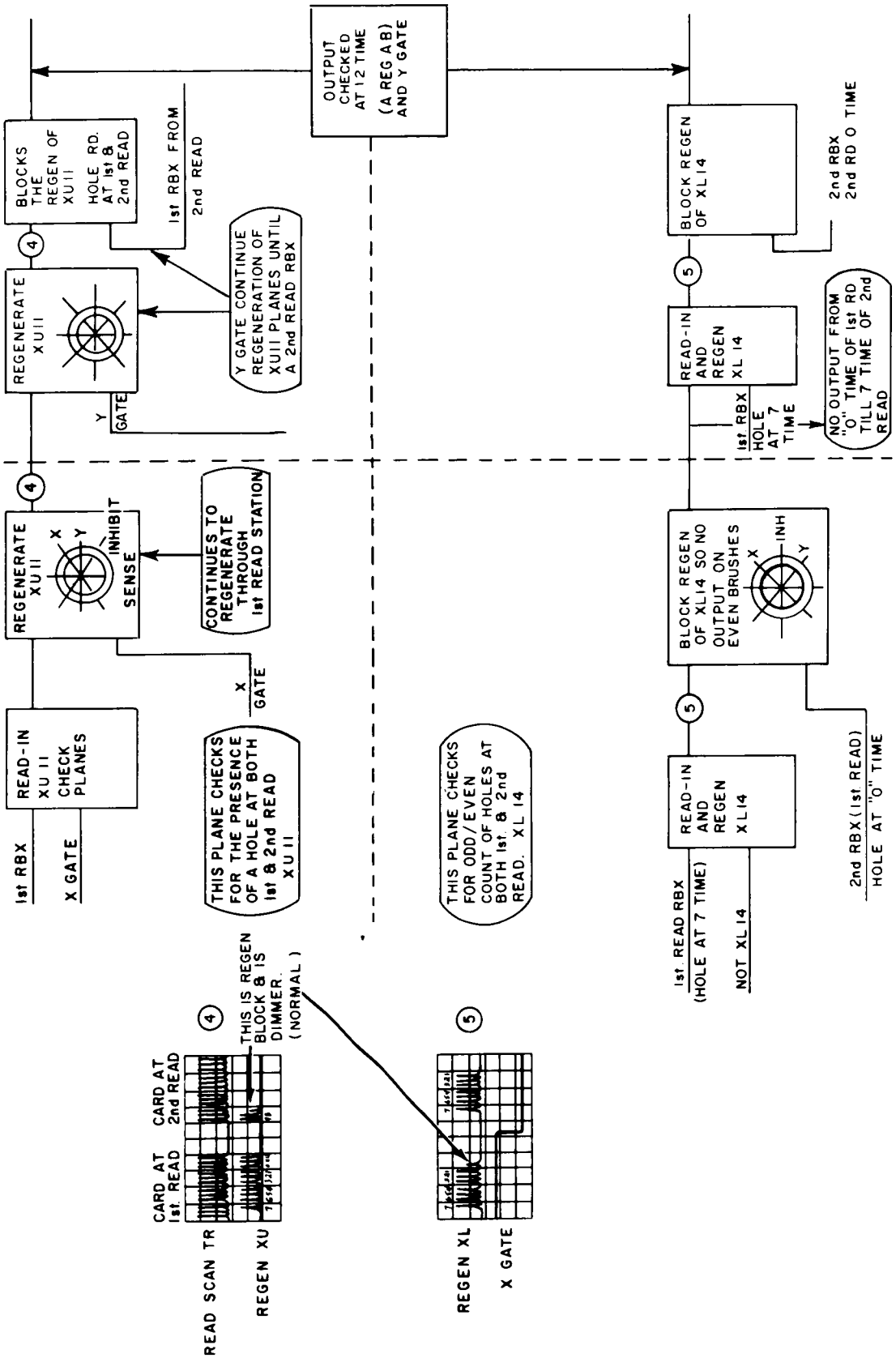


Figure 77. Row Bit Composite

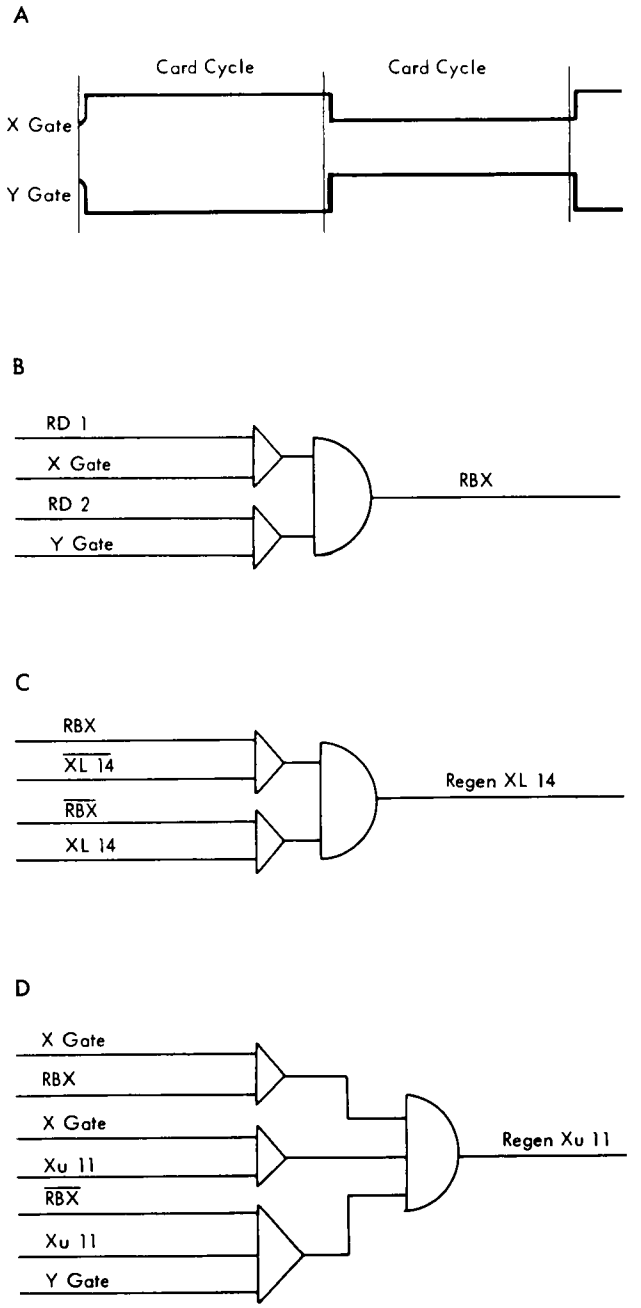


Figure 78. Read Checking Composite

A position in the X_L plane is alternately at 1 and 0 for each hole read in the corresponding column of the card.

A position in the X_u plane is set to 1 for the first hole read at first read and is regenerated until the first hole is read at second read. It then remains at 0 for the remainder of the card.

If either the X_u or X_L plane is regenerating during the last scan when the Y-gate is up, an error condition exists (Figure 79). This means that either a hole was misread or the circuitry is not functioning properly.

A card entering first read when the Y-gate is up is checked in a similar manner. However, it is checked by Y_u and Y_L planes.

Proper regeneration can be checked by syncing on the X- or Y-gate. The cards used should all contain the same character and should be run on a read-and-branch operation.

Reader Fails to Read Certain Columns of the Card

This quite often is an open between the brush and the row bit core in storage.

Raise the brush assembly from the contact roll, and, with the power on, measure the voltage between the brush in question and the ground. A normal brush should read —20v while an open line will be zero.

Reader or Punch Does Not Respond to Control of the Process Unit, and Feeds Cards Continuously

Check the off-line switch for correct position. For machines having ON and OFF labels, this switch should be in the OFF position. For machines labeled ON LINE and OFF LINE, the switch should be in the ON LINE position.

Suggested Syncs for Reader, Punch

MINUS T READ 2 (35.15.51) can be used in combination with ADDRESS COMPARE to initiate a scope sweep during read or punch operation.

Example: Assume that a 6 is failing to read in column 50. Punch a 6 in column 49 and use the CE sync hub with the ADDRESS SWITCH set to 0049, and —T READ 2 jumpered to the wirable input. This provides a sweep start just before scanning column 50 at 6-digit time. A similar method can be used for punching failures or for punch-brush-reading failures by using addresses 0100 through 0180.

Reader Punch Sync Start

A-register-combined bits (reader punch cycle point) in combination with ADDRESS COMPARE EQUAL provides an excellent sync start for localizing card reading or punching failures.

The purpose of this service hint is to point out that A-register combined bits for digits 2 through 7 can be obtained from the SENSE-SWITCH TEST-CIRCUIT-ON logic 34.22.11. SENSE-SWITCH-ON provides a —T output when there is a 2 in the A-register. Sense switches C through G likewise provide —T outputs on digits 3 through 7.

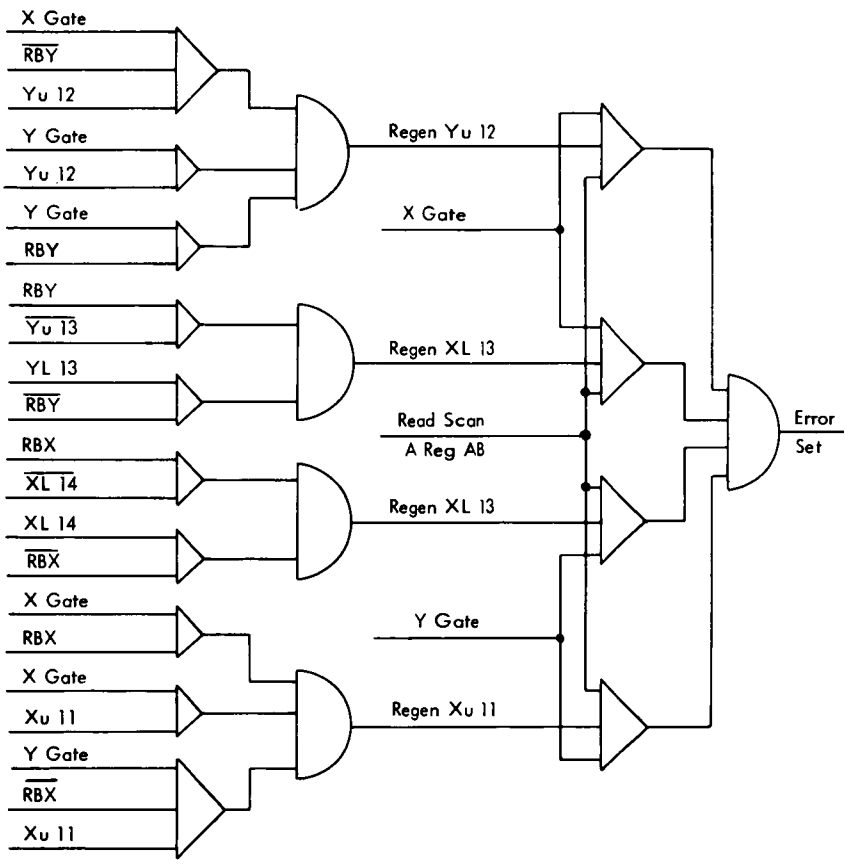


Figure 79. Read Error Composite

Reader Fails to Feed a Card When Op Appears in Op Register

Possible causes:

1. The read feed trigger is ON, but there is no signal to the clutch magnet. There may be a bad connection between the 1401 and the 1402, or a bad magnet driver or convert block in the driver circuit.
2. The read feed trigger is OFF. The rise time of the read process pulse may be too slow, or should be 8v in 1.5 μs maximum at the feed trigger set. Slow rise at this point may also cause the reader to hesitate. The feed trigger may not be gated because of failure of one of the required signals.
3. Mechanical clutch adjustment is incorrect.

No Information Is Being Read from the Card into Storage — Usually Causes a Reader Check

Possible causes:

1. The second read brush is raised off the contact roll.
2. A loose or broken common brush at the second contact roll.
3. A bad IBM 022 transistor in the second-read common-brush circuit.
4. The read-scan trigger fails to turn on. There may be several bad cards in the gate or set circuit. Sync the scope on the turn-on of the read-feed trigger, and examine these circuits for difficulty.
5. A bad sense amplifier or a preamplifier on the RD 2 row bit output.
6. A failure in the A-register digit and zone-inhibit gating circuits in the read encoder.
7. Failure in the A-register setup circuitry and no setup occurs.

The procedure for scoping in 5, 6, and 7 is the same as in 4.

Incorrect Information Is Being Read into Storage from the Card — Usually Causes a Reader Validity and/or a Reader Check

Possible causes:

1. An intermittent make of read 2 common brush.
2. Cards are feeding late in such a way that the brush-time spans two-makes of the impulse CB's.
3. Cards are feeding skewed in such a way that one brush reads two columns. This is usually confined to one end of the card, depending on which way the skew occurs.

4. Card failure occurs in the read-encoder circuitry. This usually affects only certain characters, or digits, or zones.
5. Card failure occurs in the A-register setup. This is indicated by storage position 000 having other than CAB address when the reader stops.

False Read Check or Punch Check

Possible causes:

1. If a single column is involved, check for loose or broken wire or check the brush at the first read station. Also check for an open line to the row bit core in storage.
2. If all columns or those with punches only are involved, use Figure 80 and examine checking circuits. The upper portion of the chart is read as follows:
   a. If the read cycle trigger is on (Y-gate) the PFR brush count enters the X-planes, the first read count enters the Y-plane, etc.

		PFR READ BRUSHES	PUNCH CK DECODE	PUNCH CK BRUSHES	1ST READ BRUSHES	2ND READ BRUSHES
READ CYCLE TRIGGER OFF (Y GATE)		X PLANES			Y PLANES	X PLANES
READ CYCLE TRIGGER ON (X GATE)		Y PLANES			X PLANES	Y PLANES
PUNCH CYCLE TRIGGER ON (Y GATE)			Y PLANES	X PLANES		
PUNCH CYCLE TRIGGER OFF (X GATE)			X PLANES	Y PLANES		
				CHECK CYCLE		CHECK CYCLE
ONE PUNCH	UPPER Single Bit	0-1	0-1	1-0	0-1	1-0
	LOWER Binary Bit	0-1	0-1	1-0	0-1	1-0
TWO PUNCHES	UPPER Single Bit	0-1	0-1	1-0	0-1	1-0
	LOWER Binary Bit	0-1-0	0-1-0	0-1-0	0-1-0	0-1-0
THREE PUNCHES	UPPER Single Bit	0-1	0-1	1-0	0-1	1-0
	LOWER Binary Bit	0-1-0-1	0-1-0-1	1-0-1-0	0-1-0-1	1-0-1-0

Figure 80. Reader Punch Brush Plane Chart

   b. The lower portion shows the number of times the check-plane cores switch for the various numbers of holes per column.

   Sync the scope on X- or Y-gate. Then checking circuits can be examined at any point in cycle. Use the chart to determine which phase of the entire checking cycle is being examined.

No Information Is Punched in the Card — Usually Causes Punch Check

Possible causes:

1. A bad card in the output of the punch decode circuit.
2. Punch magnet drivers are held reset by a defective driver card.
3. There is mechanical failure in punch feed.

Incorrect or Partial Information Is Punched in the Card — Usually Causes Punch Check

Possible causes:

1. A card failure in PUNCH DECODE.
2. The A-register setup control is not functioning correctly. The procedure is the same as described for reader problems.

Isolation of Bad Punch-Magnet Suppression Diodes

1. Manually enter a diagonal pattern into the punch area. For example, a 1 in column 1, 2 in column 2, 3 in column 3, etc., up to 0 in column 10. Repeat this sequence starting with column 11 and continue through column 80. This pattern produces 8 punches at 1 time, 8 punches at 2 time, etc.
2. Sync the scope on the turn-off signal of the punch-feed trigger, and set a sweep time to sufficient length to view an entire punch cycle, about 200 milliseconds.
3. Place the scope probe on any punch-magnet driver output, and observe the spikes that go more negative than —20v. All will overshoot normally for a very short interval. The bad diode causes the overshoot to increase noticeably in amplitude and duration. Observe the punch time that the large spike occurs; then, one by one, blank the punch area for that digit. For example, if the spike occurs at 1 time, there are 8 1's in columns 1, 11, 21, 31, 41, 51, 61, 71. When the bad column is discovered, the abnormal spike will disappear and the corresponding diode should be changed.

Immediate Stop on Reader Punch Error

The +U process check signal can be used to hold off the read-scan trigger by using the collector pull-over. The machine then stops with an address displayed. This is the address following the error address. The A-register contains the digit or zone that corresponds to the cycle point during which the error occurred.

Isolation of 1401 Reader Punch Error Checks

Reader or punch error checks can sometimes be caused by failures of circuitry or of components that are associated with only the X or Y set of check planes. This failure can sometimes be localized by isolating the various blocks in the RD-PCH error set net on 36.17.41.2. This may isolate the error to one set of check planes.

First and Second Read-Brush Check

Both the first and second read brushes can be quickly checked by punching cards with zeros in columns 1-10, ones in columns 11-20, etc. Observe the 1402

read-brush display while running these cards with the reader switch in off-line position and reader cables plugged in. By noting which digit time has an early or late make or break time, a worn brush can be isolated to within ten positions.

Brush Signal Checking

Resistors on paddle cards that terminate the brush cables change the brush signal from voltage to current mode. On the reader or cable side, the 20v brush signal can be observed. After passing through the resistor, only a very small pulse occurs at the leading and trailing edge of the 20v brush pulse. A current probe should be used to check these signals.

Back Circuits

Back circuits through the 1401 core array usually necessitate removal of 1401 shoe connectors when timing 1402 brushes or CB's. Do not disconnect shoe connectors when checking the first and second read brushes.

Read Errors When Reading Same Digit

Where read errors are experienced when processing cards punched with the same digit, check the one-half write current and fuse number 7 in the 1402. A heavier wire to the common brush assists in correcting this problem.

Isolation of Intermittent Read Errors

The following procedure can be used to help isolate IBM 1402 intermittent read errors. Pull the edge connector at 01A3 A24 (Logic 35.15.51.2) and plug an extender into the receptacle. Swap the edge-connector pins for sense RD1 and sense RD2 line. The first-read row bits now read into the read area of storage. The trouble can now be isolated to either the 1401 or the 1402.

Sporadic Read-In Failures

During the first-read scan the B-register is blocked from entering storage to clear the storage read-in area. Failure of the reset cam in the 1402 can result in blocking the B-register for the entire card and the storage read-in area will be filled with C-bits. Intermittent failure of this cam at any digit time can result in sporadic read-in failures. Check for this condition.

Continuous Read Scans

Continuous read scans can be obtained without cards on 1401's before serial 20000 by holding down the load key.

1401 I/O Error Stop

To stop the 1401 during an I/O error, connect a diode between +U PROCESS CHECK and +U DELTA PROCESS RESET. This holds DELTA PROCESS RESET and allows examination of conditions that caused the error. Attempts to stop the 1401 clock during an error can result in misleading conditions and can blow hammer-driver fuses.

Read and Punch Check on 12's and 9's

Read checks on 12's only and punch checks on 9's only can be caused by failures in the check-plane regen circuits.

The following items are much more critical on the IBM 1402 than they are on similar feeds and should be given extra attention:

1. Belts. Check for cracks, stretching, etc. Lubricate with IBM 70, or equivalent.
2. Pulleys and Gears. Poor bonding, loose screws, cracks.
3. Common Brushes. Clean, proper tension, grounds.
4. Card Levers. Adjustment, loose contacts.
5. Hopper and File Feed. Loose screws, lubrication.
6. Punch-Unit Die and Stripper Wick. Maintain proper lubrication.
7. Fuses. Check for loose clips.
8. Reading Brushes. Wear, tension, short strands.

A bouncing number 1 Read-Card Lever can cause missing or improper read scans especially at 11 read time.

Continuous-Core Read Out

Continuous-core read out of RD1 RD2 XU XL YU YL can be obtained by pulling inhibit driver and doing a clear and branch through read area.

Example: Starting in 082 / 082 080 __

This enables scoping the entire loop from read-out to read-in. Any addressing problems also show up in general storage.

Card Feeds Past Read Brushes Without Being Read

Failure to pick card lever 2 or relay 3 can cause cards to feed without reading. No Read Stop occurs under this condition.

Incorrect Reading

Digits read in low starting in the middle of the card.

Example: 9's and 8's read in, but 7's read in as 6's, 6's as 5's, etc.

Bouncing Impulse CB on RL 5, 6, 7, or 8.
If there are extra bits (extra RD2's), run blank cards and scope RD2 line. You should not have any RD2's with blank cards.

Manual Cranking of 1402 to Observe Setup Cycles

Cranking the machine by hand is a quick way to test the setup of the A-register. You should be able to see the A-register step from 9 to 12. Be sure that the motor is unplugged and the brushes are raised.

1. Manual setup of program: 401 1 401 __
2. Unlatch read-brush assemblies.
3. Run blank cards into read side.
4. Unplug read drive motor.
5. Turn on interlock override in 1402.
6. Set 1401 to I/E mode.
7. Press 1402 start key.
8. Observe A-register setup as you crank the 1402 through by hand.

Noise on the —20v supply can be caused by HD3 bouncing when the machine is bumped or cards are joggled. A change is being made to increase tension of HD3.

Continuous Read Scans

Continuous read scans without cards can be obtained on systems below 20000 by holding down the load key.

Read Hole-Count Troubles

To locate read-check troubles, first determine whether the trouble is common to the X and Y check planes. Therefore, enter a program to read a card and branch.

Example: 082 1082 Use an instruction that keeps the star from all addressing other than the hundreds 0 positions. Now run the suspected card into and through the machine using this program. The I/O stop switch is ON. Continue this procedure until you can tell whether the failure occurs every other time or every time.

Every-other-time-failure is an indication that the trouble is in only one of the check planes or associated circuits. To determine which circuit is failing, scope the X- or Y-gate. If the Y-gate is up, the trouble is in the X-circuits. Doing a storage scan, you can determine if this is common to only one position.

Assume that the trouble has been isolated to the Y-plane only, and it is not common to one position. With the I/O switch OFF, use a deck of cards with the first five columns punched with fives and the rest of the columns blank.

Sync on the Y-gate and set the scope to display one Y-gate time and one X-gate time. First, make sure the trouble is not the Y- or X-gate. With cards running through the machine, scope the YU and YL regen lines. You should see twelve pulses on each line. Any more or less is your trouble (Figure 81).

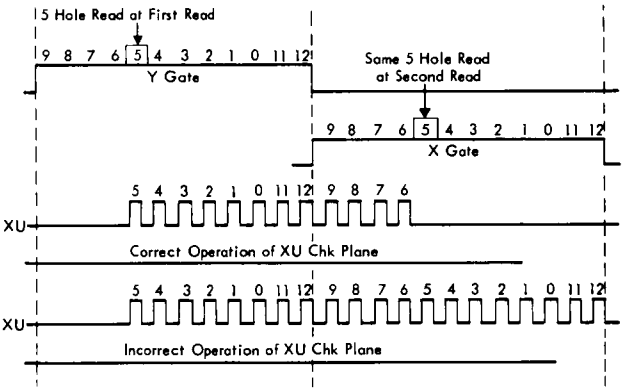


Figure 81. Read Hole-Count Timing

If the failure is something to do with the turn off of the regen line, you can AND the X-gate and the output of the sense switches, with sense switch E ON, all others OFF, for a sync to get a closer look at the trouble area.

With a little further checking into the circuits, you can adapt this technique to almost any failure. Some modification of this procedure may be necessary.

Read Scan Sync Points

To obtain a sync for a failing position:

1. Punch a deck of cards with the A-punch in the failing column and an identical punch in the preceding column. Sync on RD2 for second read or RD1 for first read.
2. A convenient sync for observing a particular read scan is to use the sense-switch circuitry on 34.22.11. Sense switch B makes it possible to scope the 8th scan (2nd digit time) because the A-register is now set to A2. The sense switches take care of scans for digit times 7 through 2. Others are:

9 digit time	01B4 A06H	4	Not read feed
8	Build sync by ANDing A-register 8 not 4 not 21		
7			
6			
5			
4			
3			
2			
1	01B4 D18H		After one trigger gate
0	01A3 D06A		+U A-register A not B
11	01A3 D06N		+U A-register B not A
12	01A3 D06H		+U A-register AB

3. To scope the first three B-cycles of scan, sync on —T encode 82 C digit 01B4 A08N 36.10.11 6E. The only things you cannot see with this sync are those items that occur before B-cycles.

Punch Scans

The same techniques used for read scan can be applied to punch scans. At the end of each punch operation the Main-star should be at address 180, the B-star light should be ON, the A-register should contain a 0 (C82), and the op register should contain a 4.

One method to check A-register setup is to manually crank a card through the punch. To do this:

1. *Clear punch area in core.*
2. Set up a punch instruction in core.
3. Set the mode switch to single-cycle process.
4. Unplug the punch drive motor.
5. Execute the I-phase of the punch instruction.
6. The punch clutch will unlatch, and card can now be cranked through by hand. The A-register setup can be observed one digit at a time.

To check the A-register setup at 12-time, sync the scope on the punch-feed trigger going OFF. This trigger should go OFF at the end of the first B-cycle.

The sense switches can be ANDed with an address in order to sync on a particular scan.

Example: You wish to observe the scan at 5 digit time when at address 104. Turn on sense switch E. Run a lead from sense switch common output (34.22.11) to address sync (32.45.31, 5E pin F). Set the manual address switches to 103. The output from address comp comes late in the cycle, so you must sync one address before the one you wish to observe.

An extra scan can be detected by observing the punch scan trigger. It should come on 13-time of each card. PACB's 1 and 2 can bounce and cause extra scan.

Punch-decode output can be checked by executing a move from the punch area to the punch area.

Example: M180180 . All that is necessary to have punch decode is equal A- and B-registers. Therefore, the A and B are equal each B-cycle. Observe pin A of 4H 36.23.31. You should see eighty pulses. A failure to decode appears as a missing pulse. A false decode can be indicated by any moving blanks that should not produce the decode pulses.

Over-all checking has a very definite place in punch-scan trouble analysis. For example, the punch-scan and punch-transfer triggers *must* come on 13 times per card. There is no need for an elaborate sync to observe this. Merely probe the trigger output and observe.

Punch Checks

A punch check can be common to both sets of error planes (Figures 75 and 82). When a check occurs on each card, the trouble is common. When a failure occurs every other card, the trouble is in a particular plane. To observe this, sync on X- or Y-gate and probe the output of the error line (36.17.41 6C pin N). If an output is seen while syncing on an X-gate, the failure is due to the Y-planes.

Be sure the X- and Y-gates are up for the correct time (approximately 240 ms per card).

To isolate failure to a particular plane:

1. Execute —4185 (4 in 185).
2. Sync the X- or Y-gate, and set the scope to display *both* the X- and Y-gates across the face of the scope.
3. While punching the same data in each card (5's), observe the regen lines (Figure 83).
4. Punch checks can be caused by loose drive belts.
5. PACB's can cause severe noise problems.
6. PA 3 and 6 are very critical in column-binary operation.

   Intermittent punch and reader checks can be caused by bad noise-suppression diodes. This usually shows up when punching a large number of holes.
7. Extra punches can be caused by loose punch bails or punch magnet armatures out of adjustment.

Punch CB Bouncing

CB's, especially the PA and RL must be maintained in perfect condition. Bouncing can be minimized by adjusting for approximately 200 grams to close the points.

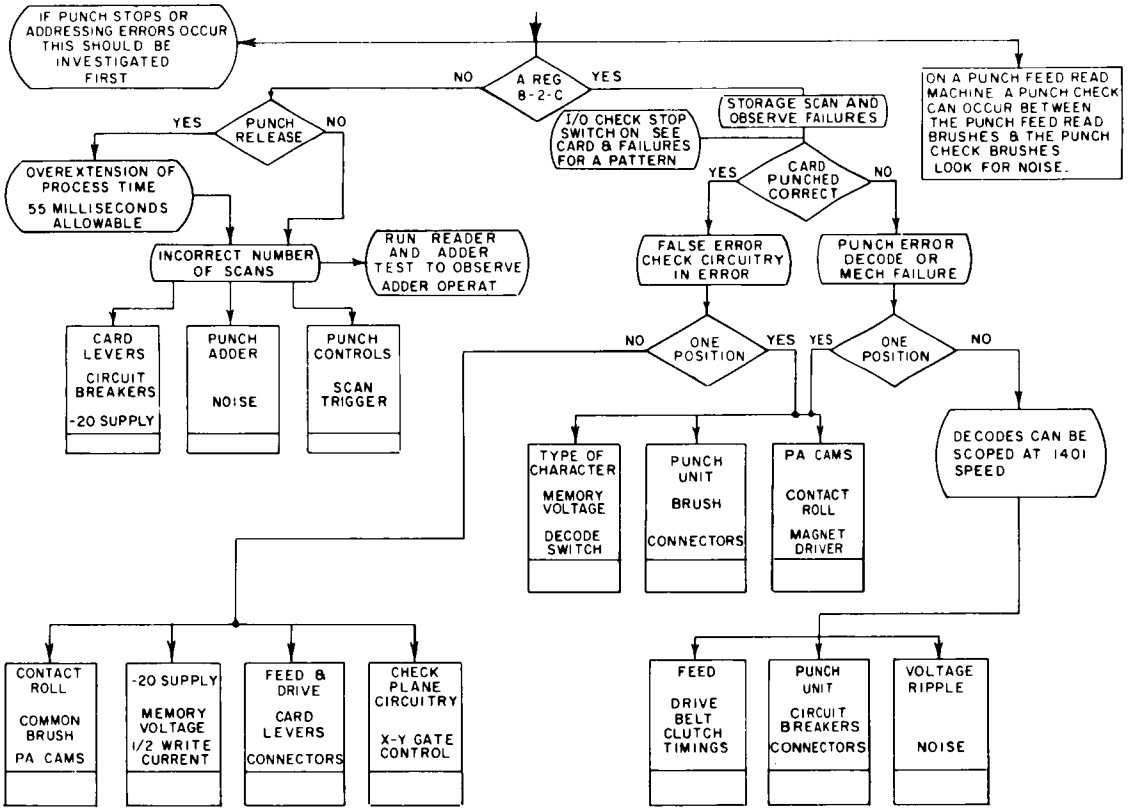


Figure 82. Punch Check Flow Chart

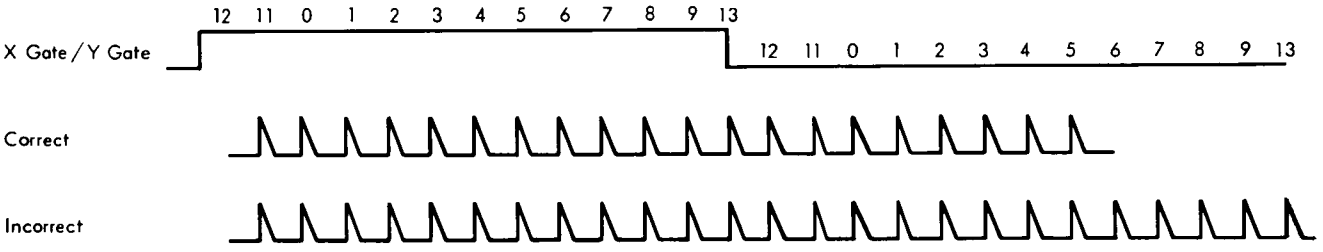


Figure 83. X- and Y-Gate Timing

Common CB troubles are:

PA 1 and 2	Extra or missing punch scans
PA 3 through 8	Extra or missing punches
PL 6	Punch stop lights (should not break before 320 degrees).
PL 13	Extra punch scan at 6 time can result if PL 13 makes at the same time that PA 2 breaks for a 6. If this condition exists, retime PL 13 to break at 182 degrees. Check its relationship to PL 14 and retime PL 14 if necessary.
RL 5 through 8	Extraneous row-bit output due to noise on one-half write line.

Punch-Decode Scoping

The punch-decode circuitry can be scoped at 1401 speed by using a load or move instruction and the combination of bits in the fields. The equal compare between bits in the A- or B-register activates the decode circuitry and facilitates scoping without running the punch.

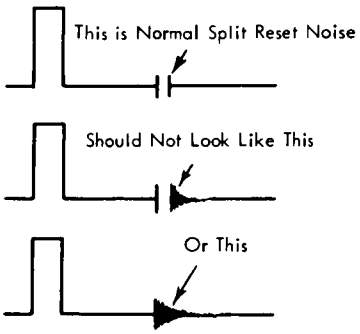


Figure 84. Punch Magnet Noise

Isolation of Mechanical or Electrical Punch Failures

To determine whether punching failures are mechanical or electrical, switch the punch-magnet cable connectors. The cables for one row punch columns 4, 8, 12, etc. If trouble follows the cable, it is electrical; trouble in the same position is mechanical.

Check for punch magnet noise.

1. Store columns 1-80 with 1's.
2. Sync the scope plus internal 1 ms/cm.
3. Probe any brush at the punch-check brush block. The scope picture should appear as shown in Figure 84.
4. To isolate the columns not being suppressed, clear the first forty columns and probe again.

Partial Punching of Holes

Partial punching of holes can be caused by weak QD driver cards. Worn genevas or a sheared output drive gear can cause intermittent out-of-place punching.

1403 Printer Service Hints

Printer Error Diagnosis

In analyzing the printer-error conditions, a quick recall on the error indicators, along with their function, can be obtained from Figures 22 and 85.

Cable Chafing

Chafing occurs when hammer-unit cables in early production machines cross over the top of the left side frame at the rear of the machine and on the lower edges of the hammer-unit blower housing. This blows the hammer driver-circuit fuses in the IBM 1401.

In current production machines, the cables pass through an opening near the top of the left side frame which positions the cables below the blower housing. A flexible sheet wrapped around the cables prevents chafing where they are tied to the frame.

On field machines that do not have the latest cable arrangement, wrap cables in affected areas with electrical tape, 450692. Relocate cables away from the blower housing and tie them to the frame with cable twine.

Visual Chain Inspection

Visually check the chain-drive gears frequently to be sure they are being lubricated and are not wearing excessively. If they are dry, check the wicks that supply these gears. Be sure there are no hard lumps in them and that they are positioned correctly. A worn drive gear can be shifted to put the machine back in operation until a new one can be obtained.

Occasional Sync Check

An occasional sync check is a possible early indication that the chain needs cleaning. The chain should be rotated by hand to determine if any tight spots exist. In many cases, vacuum-cleaning the chain and using type cleaner paper, 451529, are sufficient. If the chain continues to bind, the cartridge must be disassembled and cleaned in IBM 6 oil, or equivalent. Other possible causes of sync checks are a worn sprocket drive key, the chain being too tight because of improper adjustment of the idler pulley, and worn chain drive gears.

Timing-Drum Tolerance

The drum signal measured from either side of the drum head to ground should fall between 50 and 150 millivolts (Figure 86). An output of 200 millivolts or

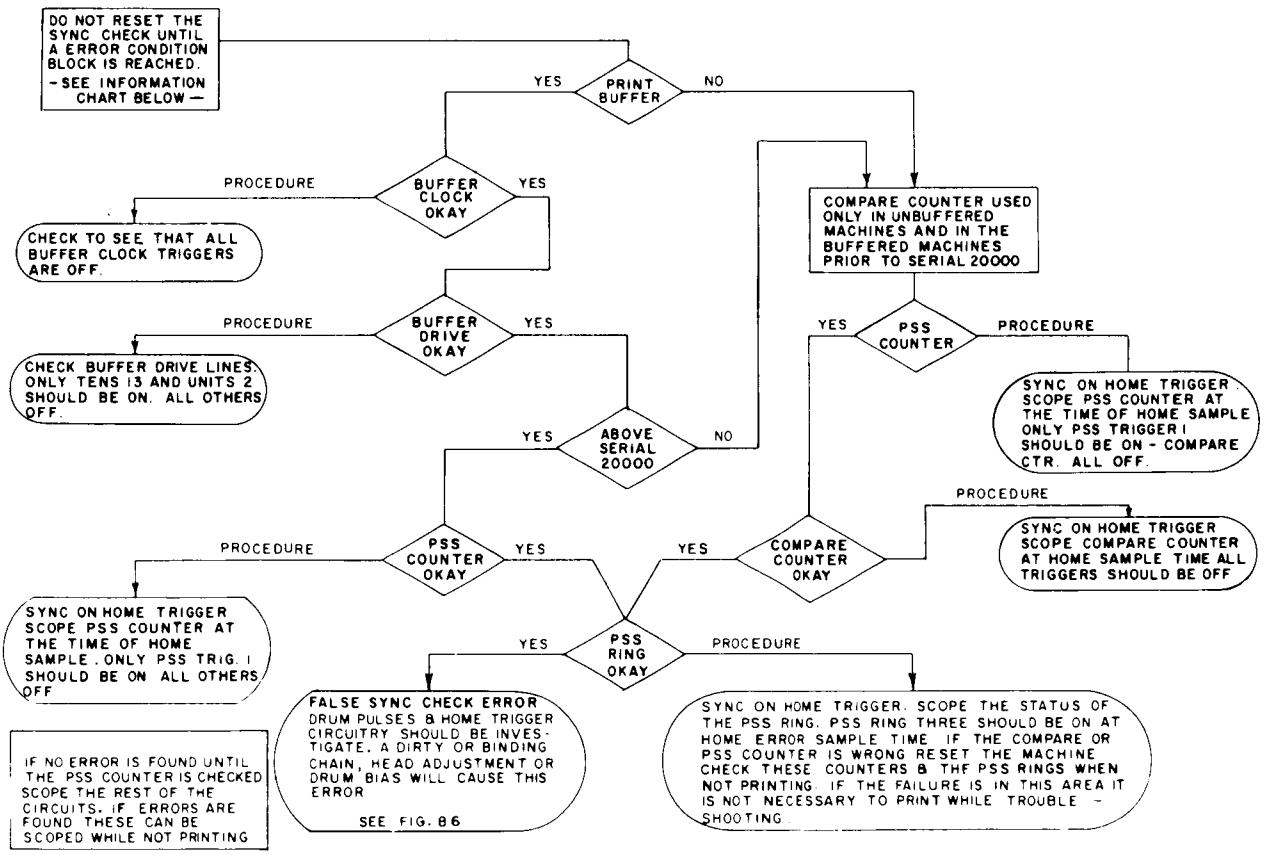


Figure 85. Printer Sync Checks

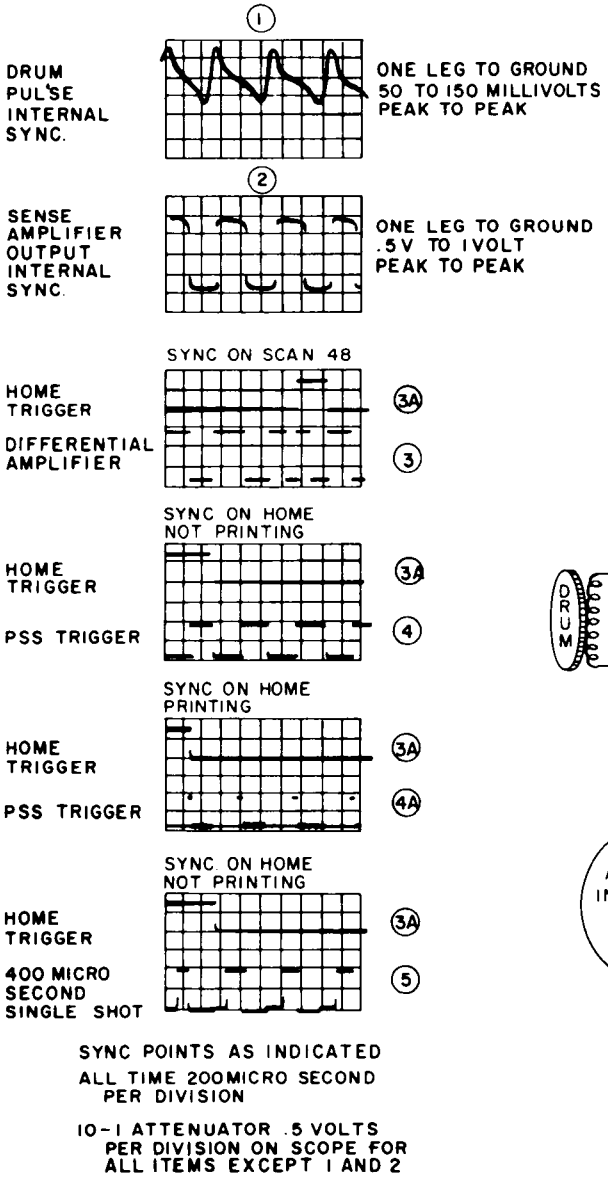
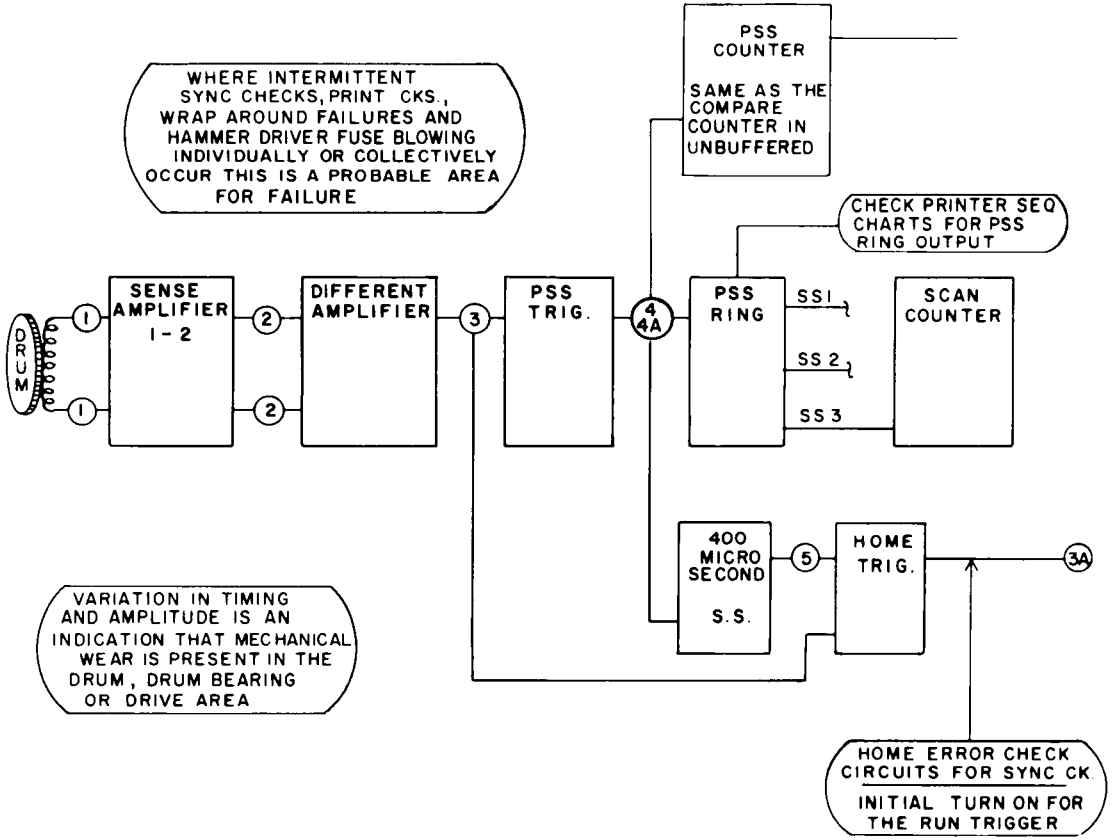


Figure 86. Printer Timing Controls



more should be questioned as this may indicate that the drum-to-read-head clearance is too small.

Intermittent 1403 Stopping

Intermittent stopping of the 1403 can be caused by play in the selection knob. The machine stops with 201 in star and I1 of print operation. It can be restarted by pressing the start key. The detents are held by four collars that slip if they are not properly tightened. Vibration causes the shift-interlock switch to break momentarily and the printer hangs up. Set the shift-interlock knob to each of the four positions and adjust the corresponding collars. Faulty microswitches give the same effect.

Sync for One Scan

A sync for any one scan of a print operation can be obtained by the insertion of a 6 input AND block in any blank position. The output of the scan counter triggers can be wired to this AND block to get an output during any one scan. This can then be used as a sync.

Continuous-Print Loop

To lock the printer in a tight loop so that the counters and rings may be checked, remove and float scans 16 and 32 from the block that develops scan 49. The printer restarts after one print scan.

Print Storage Troubleshooting

Troubleshooting can be difficult with print storage when printer-busy and and carriage-busy interlocks are effective. This difficulty can be virtually eliminated by using a branch-on-printer or carriage-busy.

On a print-storage machine, allow printing only at home time by tieing the home trigger output to the switch condition which turns off the print-ready trigger. It is also possible to single-cycle through the entire print-transfer operation.

When troubleshooting print storage, a current probe is of great assistance. The current probe part number is 451213 and the terminator, is part number 451214. CAUTION: The current probe head can be grounded when open. Take care to prevent damage to the print buffer cores.

Print-Storage Failures

To shoot print-storage failures, it often is advantageous to prevent printing and repeat only the print transfer. This can be accomplished by tieing print-scan-complete to print-transfer-complete. The print operation stops at the end of the print transfer. Removing the CR card in 01A4 C07 makes it possible to get an output from the presense amplifiers of the buffer during the transfer for the 1, 2, 4, and 8 bits. Removing the CR card in C08 provides outputs for the A, B, C, and WM bits.

Print Buffer Display

The following procedure is a convenient way of displaying the contents of print buffer.

1. Stop the machine following a print operation.
2. Manually alter the op-code character following any print operation in storage to an out of parity character.
3. Reset all system errors and alter the machine address to the address of the print operation preceding the out-of-parity character entered in Step 2.
4. Press start reset, check reset, and I/O reset. Put print-scan switch in the PRINT STORAGE SCAN position, and set the mode switch to SINGLE CYCLE PROCESS.
5. Advance with start key until the out-of-parity character enters the B-register. *Do not reset the error.*
6. Change the mode switch setting to the storage-scan position.
7. Press the start key. B-register will display the contents of location 201. A-register will display the contents of location 001 of print-buffer storage. This is the character that was printed on the previous print operation. Press the start key again, and 202 and 002 will be displayed. Continued pressing of the start key will advance to 332 and 132 of the print buffer. Another pressing of the start key will again display 201 and 001. This may be repeated as many times as desired. Figures 87 through 92 shows the PSS counter advance with or without printing.

Print Checks with Certain Print Patterns

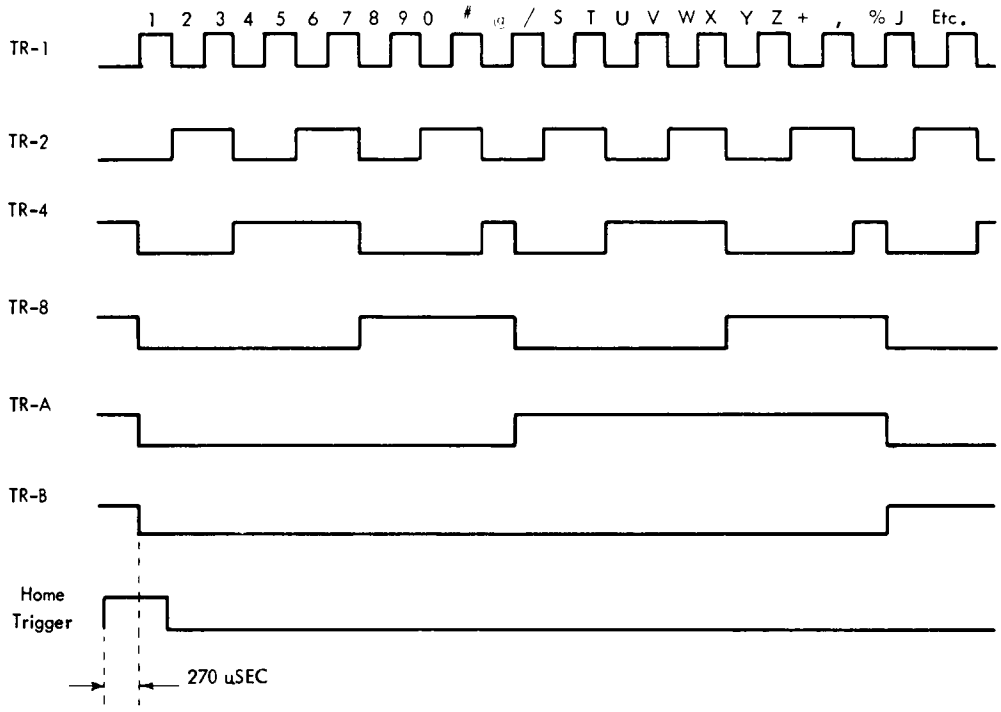
Print checks that occur on certain print patterns and in various positions are often caused by loss of the —60v return to hammer-response cores. The most common cause for loss of this voltage is blown fuses, located on 01A4 TB on A-models and 02A4 TB5 on other models. A method of checking this condition is to sync on NOT FIRST SCAN with 10 ms/cm and scope one of the failing hammer-position response outputs. All that should appear is a 60v level with small spikes. There should not be an indication of a shift of the —60v toward ground as print scans occur.

Counter and Ring Check

All counters and rings can be checked by wiring a timing pulse to drive them. This checks the rings at 1401 speed and all the triggers can be scoped. All CW triggers should be ON within 1.5 microseconds with overshoot.

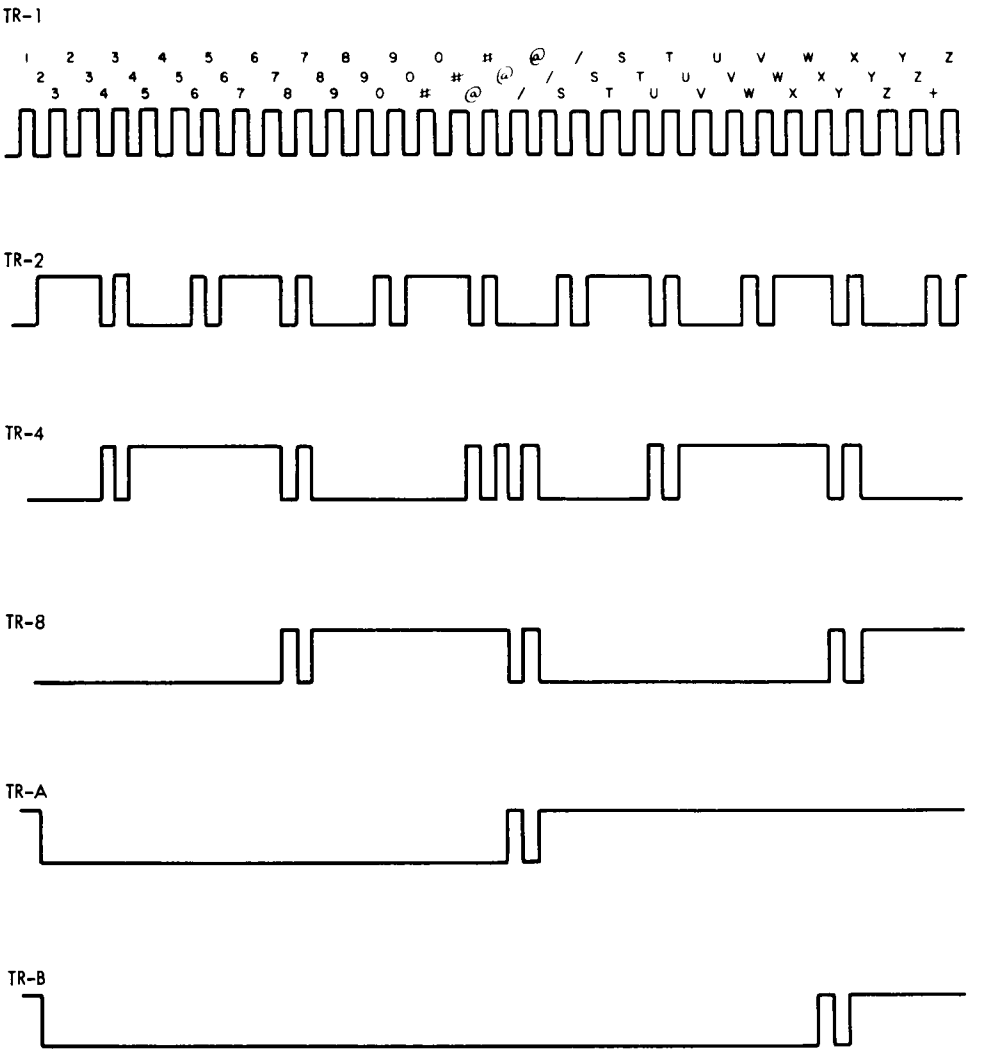
Charts are for systems above serial #20000 with Print Buffer

PSS Counter advanced by 1 9 (not printing)



1. DO NOT PRINT. Sync on home trigger going positive. Counter should advance by 1 every third PSS pulse (PSS pulse associated with a sub scan 1. Pattern should be as shown each divison represents 3 sub-scans (1.65Ms.)

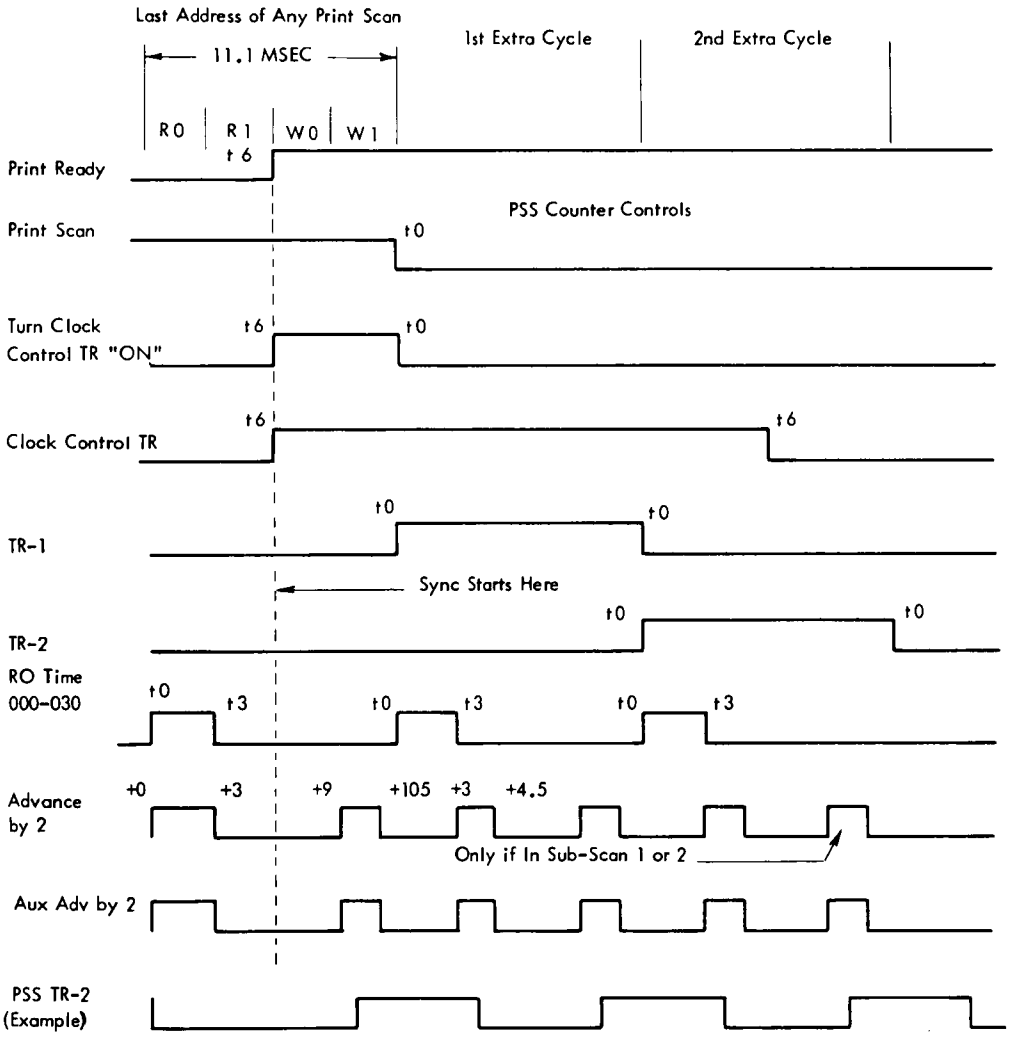
Figure 87. PSS Counter Advance by 1 (without Printing and with Print Buffer)



NOTE: Trigger B Now Drawn in step because of the duration of the pulse.

Without Print Buffer

Figure 88. PSS Counter Advance by 1 (without Printing and without Print Buffer)



1. Sync on Clock Control Trigger Going Positive and Print. Pattern Should be as Shown Above.

Figure 89. Print Pattern Timing

PSS Counter Advanced by 2 (Even) Scan 48

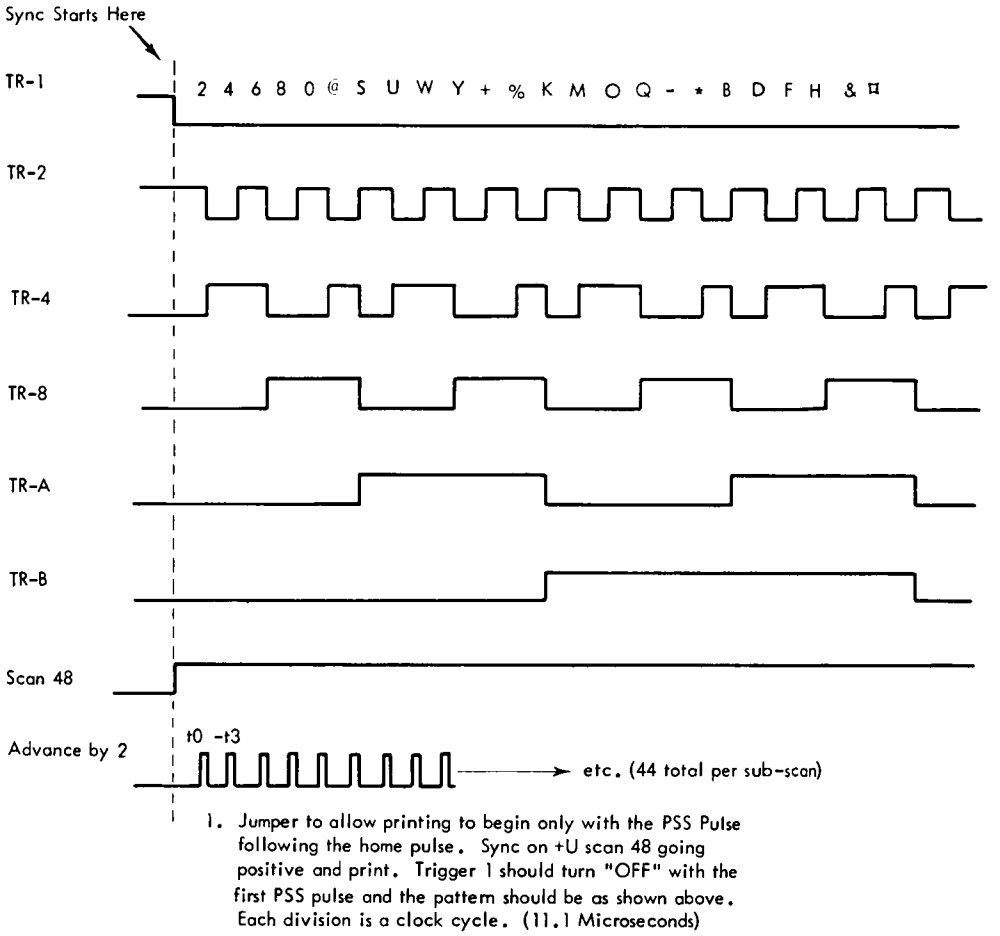


Figure 90. PSS Counter Advance by 2 (Even) Scan 48

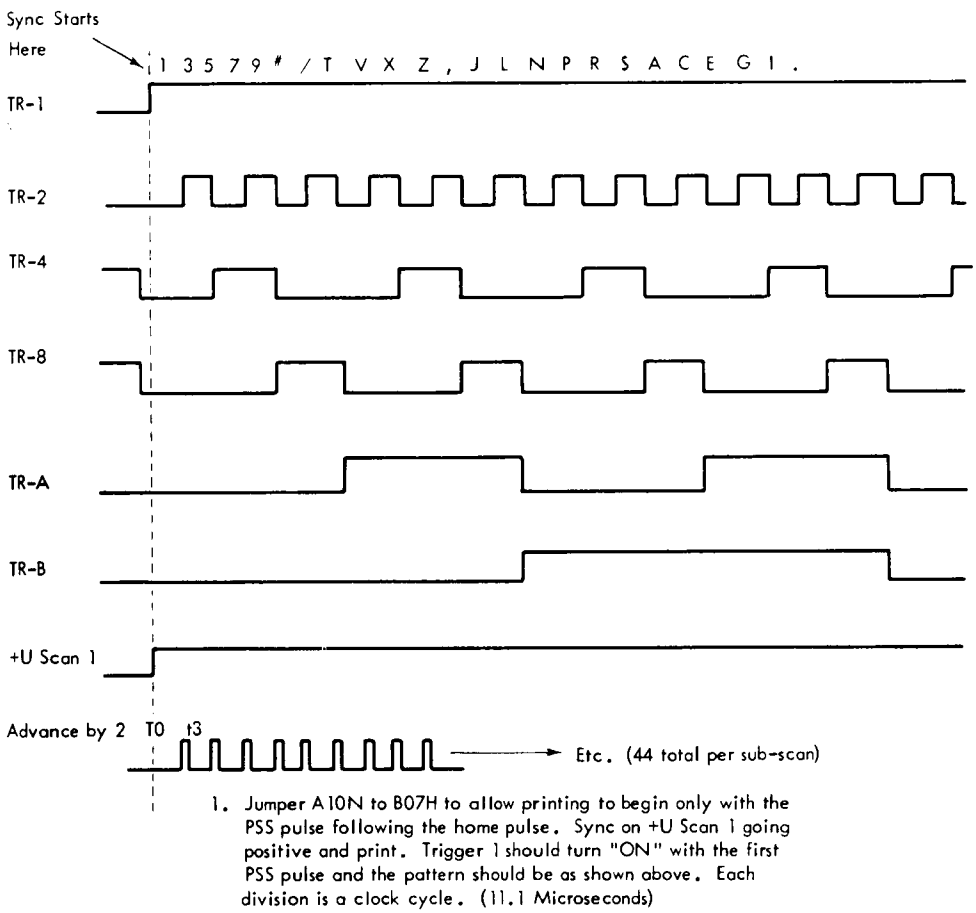
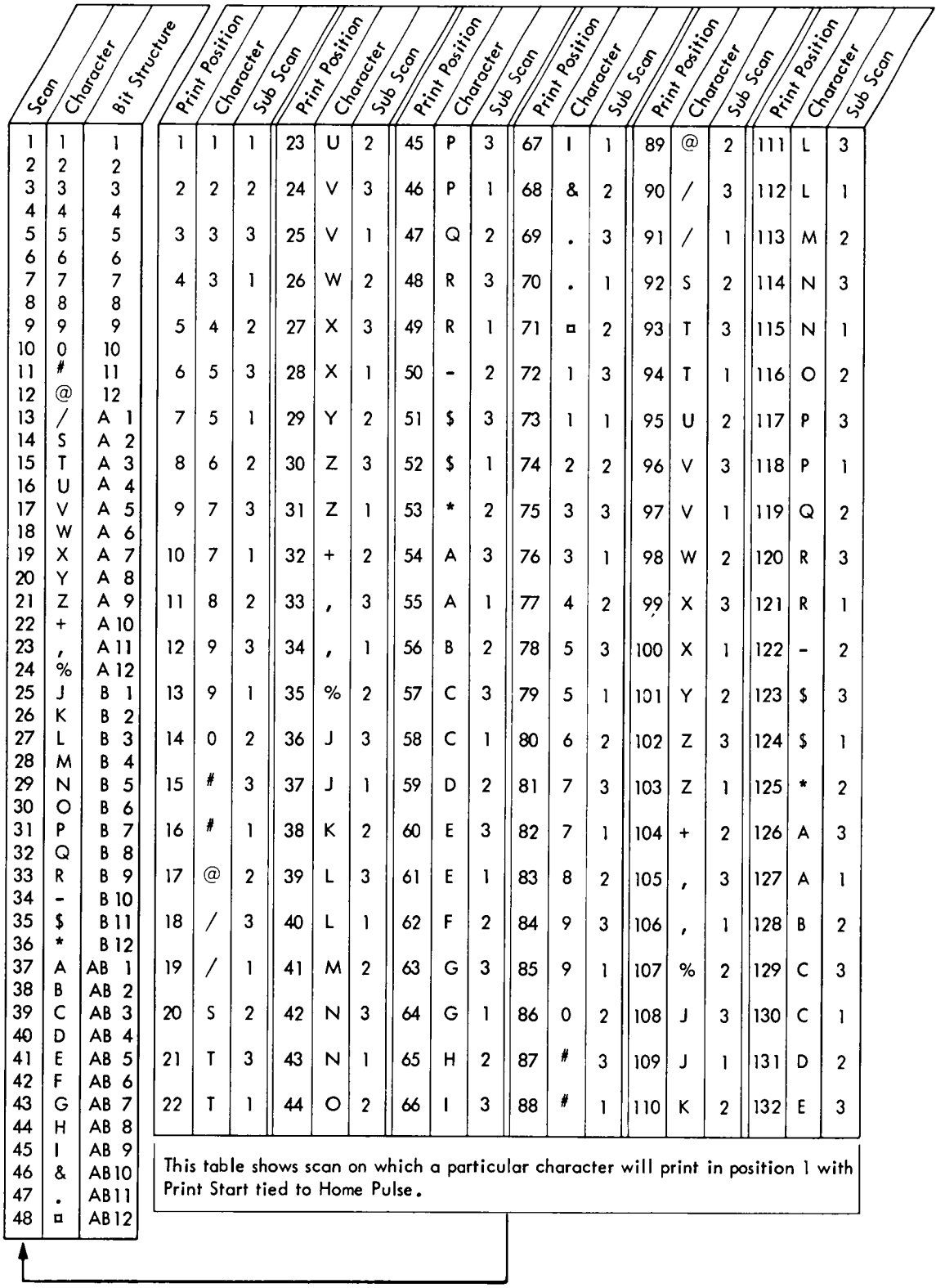


Figure 91. PSS Counter Advance by 2 (Odd) Scan 1



Scan	Character	Bit Structure
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	0	10
11	#	11
12	@	12
13	/	A 1
14	S	A 2
15	T	A 3
16	U	A 4
17	V	A 5
18	W	A 6
19	X	A 7
20	Y	A 8
21	Z	A 9
22	+	A 10
23	,	A 11
24	%	A 12
25	J	B 1
26	K	B 2
27	L	B 3
28	M	B 4
29	N	B 5
30	O	B 6
31	P	B 7
32	Q	B 8
33	R	B 9
34	-	B 10
35	$	B 11
36	*	B 12
37	A	AB 1
38	B	AB 2
39	C	AB 3
40	D	AB 4
41	E	AB 5
42	F	AB 6
43	G	AB 7
44	H	AB 8
45	I	AB 9
46	&	AB 10
47	.	AB 11
48	¤	AB 12

Print Position	Character	Sub Scan	Print Position	Character	Sub Scan	Print Position	Character	Sub Scan	Print Position	Character	Sub Scan	Print Position	Character	Sub Scan	Print Position	Character	Sub Scan	Print Position	Character	Sub Scan
1	1	1	23	U	2	45	P	3	67	I	1	89	@	2	111	L	3			
2	2	2	24	V	3	46	P	1	68	&	2	90	/	3	112	L	1			
3	3	3	25	V	1	47	Q	2	69	.	3	91	/	1	113	M	2			
4	3	1	26	W	2	48	R	3	70	.	1	92	S	2	114	N	3			
5	4	2	27	X	3	49	R	1	71	¤	2	93	T	3	115	N	1			
6	5	3	28	X	1	50	-	2	72	1	3	94	T	1	116	O	2			
7	5	1	29	Y	2	51	$	3	73	1	1	95	U	2	117	P	3			
8	6	2	30	Z	3	52	$	1	74	2	2	96	V	3	118	P	1			
9	7	3	31	Z	1	53	*	2	75	3	3	97	V	1	119	Q	2			
10	7	1	32	+	2	54	A	3	76	3	1	98	W	2	120	R	3			
11	8	2	33	,	3	55	A	1	77	4	2	99	X	3	121	R	1			
12	9	3	34	,	1	56	B	2	78	5	3	100	X	1	122	-	2			
13	9	1	35	%	2	57	C	3	79	5	1	101	Y	2	123	$	3			
14	0	2	36	J	3	58	C	1	80	6	2	102	Z	3	124	$	1			
15	#	3	37	J	1	59	D	2	81	7	3	103	Z	1	125	*	2			
16	#	1	38	K	2	60	E	3	82	7	1	104	+	2	126	A	3			
17	@	2	39	L	3	61	E	1	83	8	2	105	,	3	127	A	1			
18	/	3	40	L	1	62	F	2	84	9	3	106	,	1	128	B	2			
19	/	1	41	M	2	63	G	3	85	9	1	107	%	2	129	C	3			
20	S	2	42	N	3	64	G	1	86	0	2	108	J	3	130	C	1			
21	T	3	43	N	1	65	H	2	87	#	3	109	J	1	131	D	2			
22	T	1	44	O	2	66	I	3	88	#	1	110	K	2	132	E	3			

This table shows scan on which a particular character will print in position 1 with Print Start tied to Home Pulse.

Figure 92. Printable Characters during Subscan 1, 2, and 3 of Scan 2

Isolation of False Print Checks

Print Word Mark Test 1010B is a useful tool in determining which position is causing false print checks. With the error-check stop switch ON, the last position printed on the last print line is the error position.

Print-Magnet Check

A good print-magnet coil measures approximately 11 ohms. Coils will partially short causing printing to fail but no print check. Measure from the output pin of the hammer-drive card to pin P, which is the —60v return.

Intermittent Print Checks

Intermittent print checks can be caused by the absence of —60v on 01B5 Pin P of hammer-drive cards. This is a suppression diode return voltage for the hammer drivers. The print position, which is in error as indicated by storage scan, can point out which driver cards to check for missing —60v or bad suppress diodes. A hammer drive that is not being suppressed appears similar to that shown in Figure 93. Keep in mind that one or more hammer drivers not being suppressed can cause print checks in other positions that may be printing on different scans.

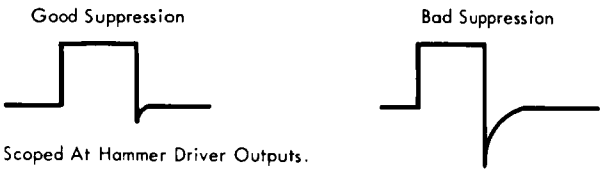


Figure 93. Hammer-Driver Suppression

Sync Checks When Hitting Printer Stop Key

Sync checks, when hitting the stop key on the printer, have been traced, in some cases, to noise on a wire from the stop key. This noise, coupled to the twisted pair of wires leading to the sense amplifiers, results in improper pulses to the PSS counter. A solution to this has been to switch the stop-key wire with a spare wire in the cable.

1403 Scoping

Better scope pictures are available in the IBM 1401 after the integrator scan than from the two test hubs on the 1403. The shoe-connector layout of the printer cables can be found under 01A2.

Intermittent Sync Checks

When intermittent sync checks are experienced, put the machine in a print-and-branch operation. Scope all the CW triggers in gates 01A5 and 01A6. All triggers should come ON within 1.5 microseconds with overshoot and remain at a down or up level until they are reset.

Hammer Flight Time

Individual hammer flight time can be checked by using four-part forms. The impression left by the hammer on the fourth copy should be centered on the printing. The hammer impression should frame the character.

CAUTION: *Do not force the machine to run by holding the I/O check-reset switch or the printer check-reset key on. This can cause damage by blowing core-storage decodes and drivers.*

CAUTION: *The loss of +6v to gate 01B5 burns out the print-magnet coils without blowing hammer-driver fuses.*

Print in Flight

If the operator should happen to push any of the start keys while a print operation is skip interlocked, it prints in flight.

Hammer-Driver Fuse

Some hammer-driver cards, 371940, might have wrong-size fuses. The proper fuse is 1½ amps and color coded purple and yellow. The incorrect size is ¾ amp and coded purple and orange.

Carriage Movement with Power Off

To check for carriage taking off when turning power on or off, and it is suspected that the hydraulic unit is not adjusted correctly, the low-speed start-magnet-driver output can be grounded. The carriage does not move when the hydraulic unit is adjusted correctly.

Carriage Controls

CARRIAGE-SPACE KEY

Hitting the carriage-space key (Figure 94) enables you to check out the following single shots (systems above 20000):

1. 01B1D14A	—U	10 μs
2. 01B1C17A	—U	10 ms
3. 01B1E24A	—U	70 μs
4. 01B1F12A	—U	4 to 9 ms

5. Sync internal to see the output of single shots.

CARRIAGE-RESTORE KEY

Hitting the carriage-restore key enables you to check out of the following single shots (systems above 20000):

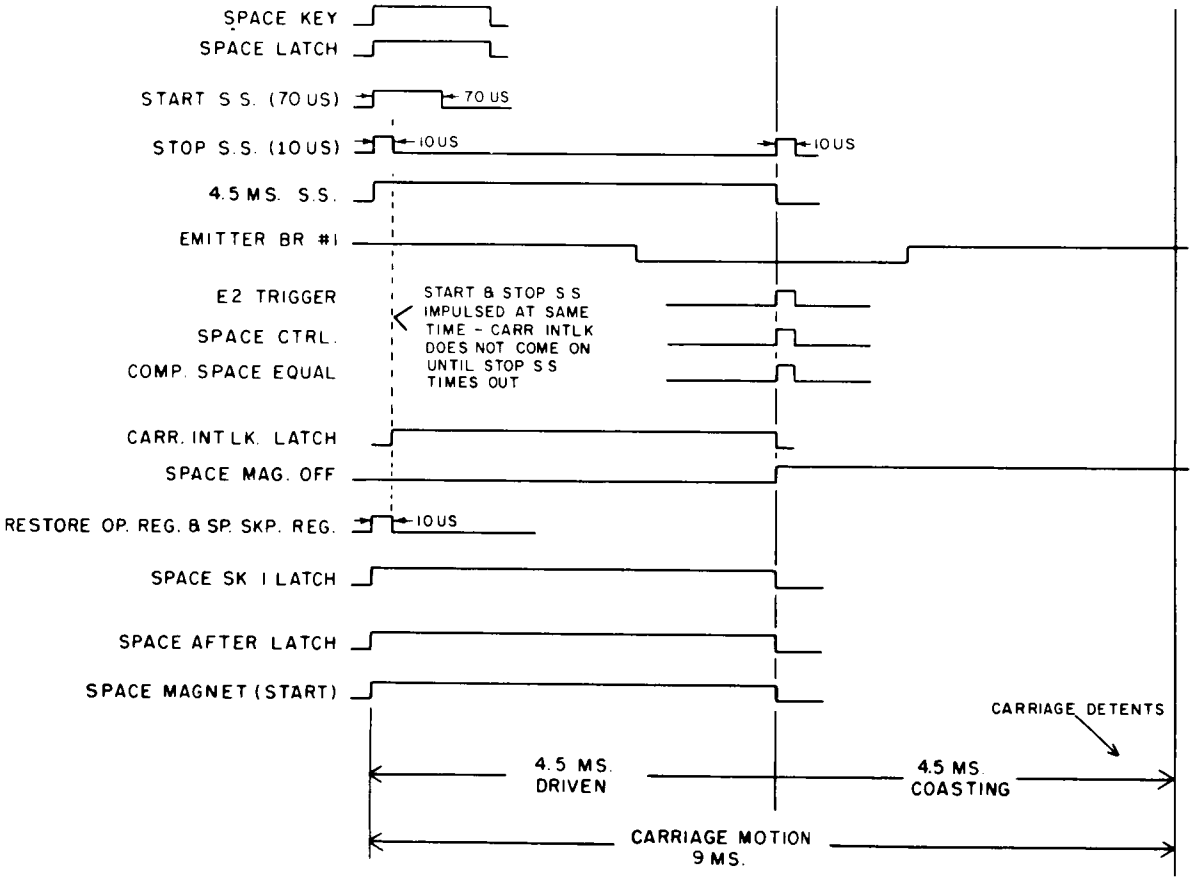


Figure 94. Space Key Operation Timing

1. 01B1E07A	—U	10 μs
2. 01B1E21A	—U	10 μs
3. 01B1D10B	—U	1 ms delay

4. Sync on input and look at the output to see the delays.

CARRIAGE-STOP KEY

Hitting of the carriage-stop key enables you to check out the delay unit at 01B1F09N —9 ms delay.

SYNC POINTS FOR CARRIAGE CIRCUITS

1. +U after space control (36.42.11) to check space or skip after printing.
2. +U space skip gate (36.42.11) to check setup of the space-skip register (36.42.11) and the carriage op register (36.41.11) on any programmed space-or-skip operation.
3. —T not start single shot (36.44.11) going positive to check the space counter (36.44.11).
4. —T stop brush signals (36.45.11) to check channel-brush encoder (36.45.21), and the setup of the channel register (36.45.31).

Rise Time of PSS Pulse After Timing Disk Magnetization

The following procedure can be used when magnetizing the 1403 timing disk to determine if the timing disk is biased to give the best possible rise time to the PSS pulse at the PSS trigger.

Refer to *Magnetize Timing Disk,* in the IBM 1403 CE Reference Manual for the magnetizing procedure. To perform steps 5 or 7, do the following:

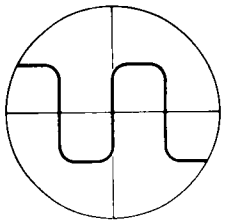
1. Use a 10 to 1 voltage probe.
2. Trigger 310 scope on external sync plus.
3. Sync on the PSS pulse at pin A of 01A6A23 (36.-31.01.2).
4. Set sweep speed to 100 μs per division.
5. Probe the PSS pulse and align the rise of the pulse on the center line.

Adjust the horizontal control so the rise of the PSS pulse is on the center line of the 310 scope face as shown in Figure 95a.

The wave shape shown in Figure 95b is a picture of the magnetic impulses directly from the timing-disk read head. The sharpest change in wave form at the center line gives the best rise time to the PSS pulse at the PSS trigger.

(A) SYNC PULSE

310 SCOPE



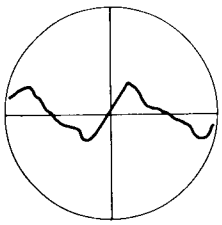
0.5 Volts/Division
100 μ sec./Division Sweep
10 to 1 Voltage Probe

At Disk Speed of 750 RPM

1. 15 - 150 MV from each leg.
2. 100 - 300 MV peak to peak across both legs.
3. 530 - 580 μ sec. between PSS pulses.
4. Rise time .5 μ sec. maximum. (Measurements taken at output of Differential Amplifier)
5. PSS pulse # 144 is 230 - 330 μ sec. from home pulse.

(B) CORRECT BIAS

310 SCOPE

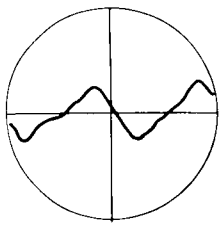


0.01 Volts/Division
100 μ sec./Division Sweep
10 to 1 Voltage Probe

Sync same as set up in Figure 70a Probe 1403 SA 1 pin B or D.

Wave shape shown in Figure 70b is a picture of the magnetic impulses directly from the timing disk read head. The sharpest change in wave form at the center line will give the best rise time to the PSS Pulse at the PSS Trigger.

(C) CORRECT BIAS

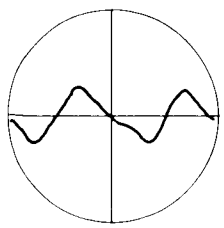


Same set up as in Figure 70b

Wave shape being the inverse of Figure 70b means only that the Read Head wires are reversed.

(D) INCORRECT BIAS

310 SCOPE

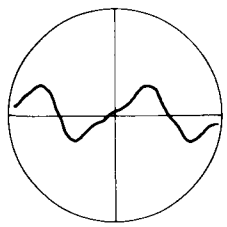


Same set up as in Figure 70b

The sharpest change in wave form is <u>not</u> on the center line of the 310 Scope face.

(E) INCORRECT BIAS

310 SCOPE



Same set up as in Figure 70b

Wave shape being the inverse of Figure 70d means only that the Read Head wires are reversed.

Figure 95. Read Head Wave Shapes

Storage Service Hints

When a complete core analysis is required, a quick recall of both the storage data flow (Figure 96) and the core addressing philosophy (Figures 97 and 98) may prove valuable in analyzing intermittent storage failures.

A quick analyzation of the data flow, along with the following check list, will enable a rapid diagnosis of storage problems.

1. Check storage power supplies as outlined in *Power Supply Hints.*
2. Check the storage clock and strobe pulses as explained under adjusting 1401 storage pulses.
3. Check current drivers, current source, and matrix switch outputs.
4. Check the decode switches, the matrix switch, secondary windings and core array X and Y drive lines.
5. Check the drive pulses at the terminating resistor board for current waveshapes (Figures 98 and 99).

1401 and 1406 Storage Analysis

The storage gate circuitry in the 1401 and 1406 operates at a high power level and, therefore, generates considerable heat. Adherence to the following items will improve storage reliability.

1. Always replace the storage gate card cover after changing the cards. The card cover is necessary to maintain correct airflow and cooling of the SMS cards.
2. Do not disrupt the airflow in the storage area by setting logic books or other items on top of the 1401.
3. Do not position the 1406 so that airflow is blocked at the rear of the machine.
4. Do not stop the 1401 clock within a memory cycle. Because the storage gate circuitry is not designed for a continuous duty cycle, the clock-stop latch is designed to stop the clock at 000, when no current is being driven.
5. Use the storage gate voltage adjustment procedure as explained in *Power Supply Hints* to set the storage gate voltages. Use of insulated tips for probes and meter leads will eliminate the possibility of shorting pins in the storage area.
6. Do not change the address-selection switches when the enter key is held up.
7. Never attempt to replace SMS cards in the storage gate while the power is on.
8. Do not pull the fuse in the 1402 to stop the fans in all gates. Individual gates, with the exception of 01A1, 01A4, 01B5, and 01B7, may be heated by disconnecting the ac plug mounted on the gate.

When a storage trouble develops, SMS card damage can be held to a minimum by observing a few precautions and use of the following service technique:

1. Do not swap cards or change the address switches until the current source and diverter cards have been checked with a scope.
2. Set up a scope as follows:
   Sync. External +U time 000-030, available at CE console.
   Sweep Speed. 1 microsecond per division.
   Volts Per Div. 10 volts unless specified otherwise on the wave form chart below.
3. Set a valid character in the bit switches.

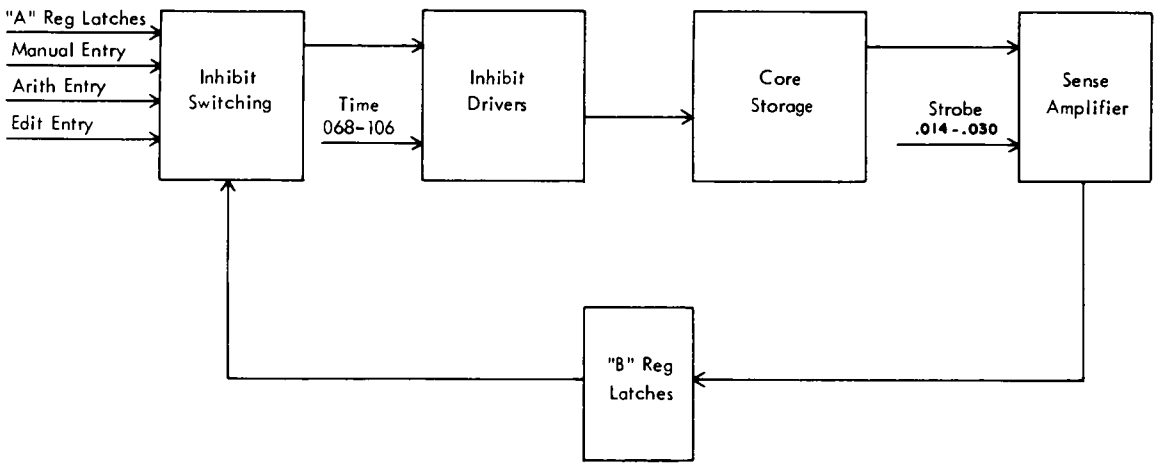


Figure 96. Basic Storage Path Flow

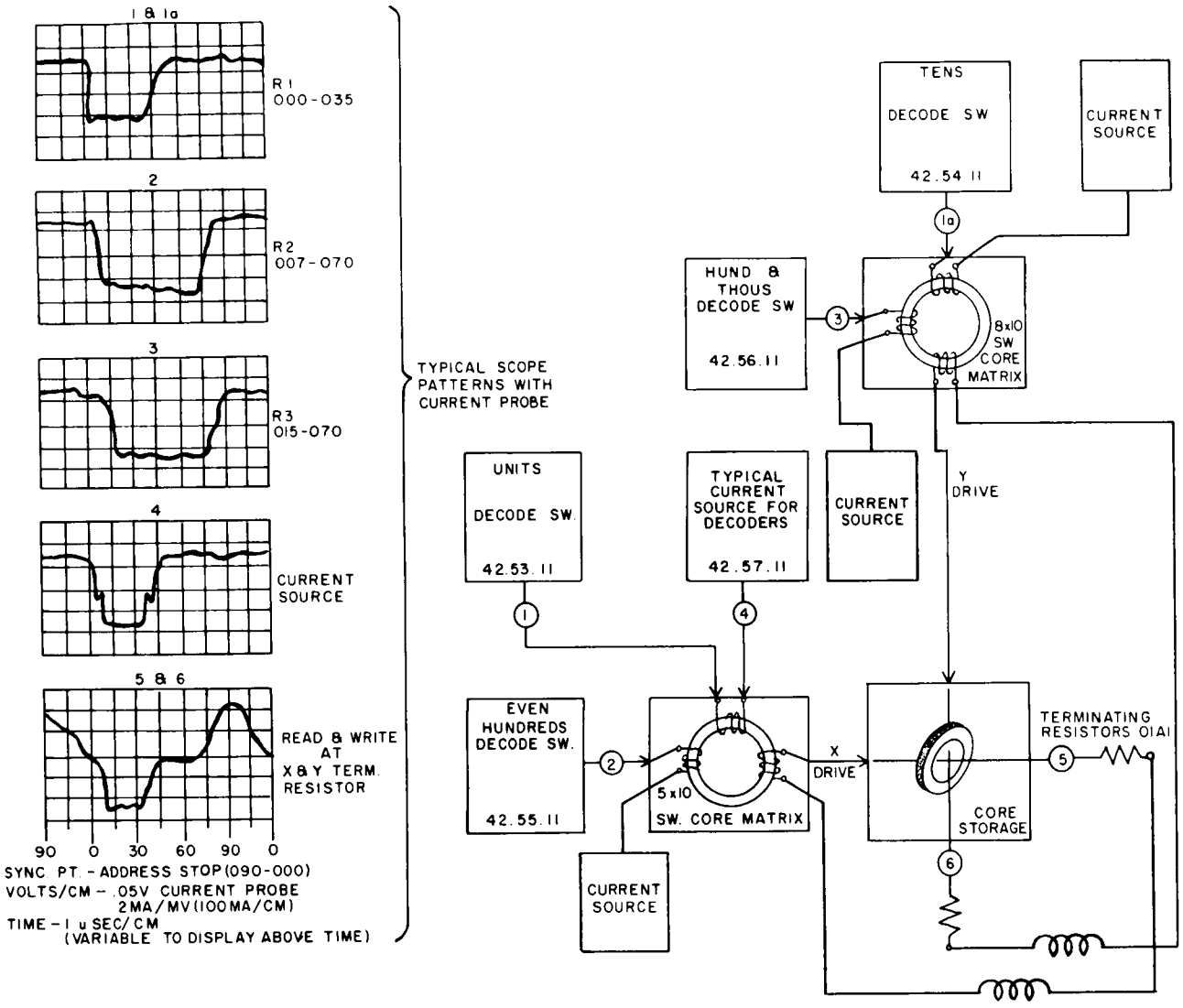


Figure 97. Core Addressing and Scoping Prints

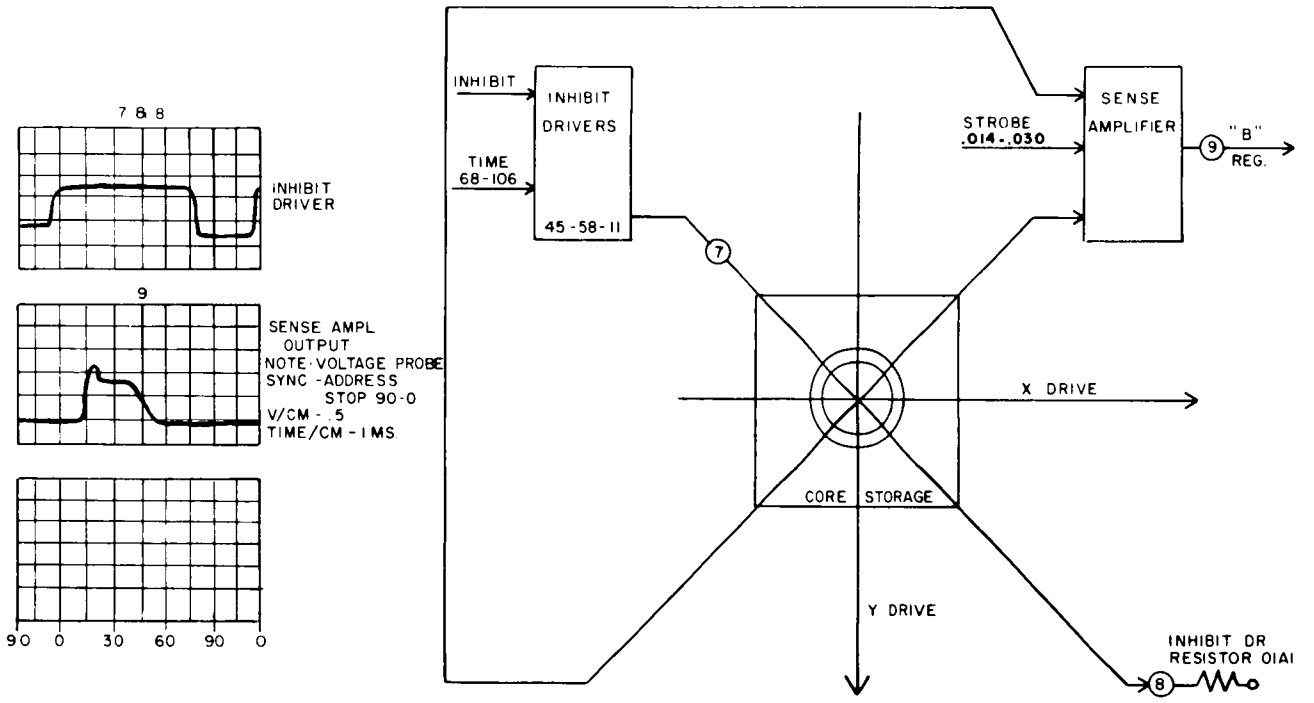


Figure 98. Inhibit and Sense Amplifier Scoping

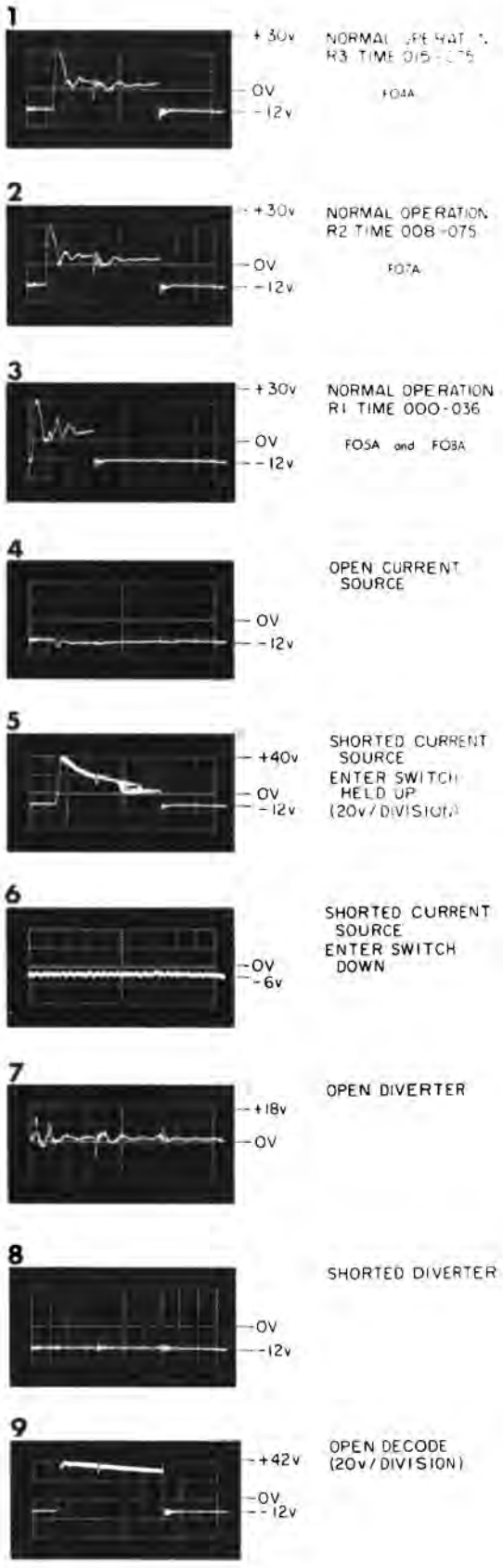


Figure 99. Memory Wave Forms

4. Scope pin locations F04A, F05A, F07A, and F08A in the storage gate that is failing while holding the enter key up.

Address	*Gate*	*Logic*
0000-3999	01A1	42.57.11
4000-11999	01B1	42.67.11
12000-15999	06B5	42.77.11

5. Only four points (F04A, F05A, F07A, F08A) need be scoped to determine if the current source, diverter, and decode cards are working correctly. Compare the wave forms (Figure 99) to the following:

Location	*Correct Wave Form*	*Pulse*
F04A	1	R3 015-075
F05A	3	R1 000-036
F07A	2	R2 008-075
F08A	3	R1 000-036

6. Scope pictures 4 through 8 represent what will be seen if the current source or diverter cards are damaged.

   The duration of the positive excursion in scope picture 5 will vary, depending on which point is being probed, because it represents timing pulse R1, R2, or R3. If source or diverter trouble is indicated, proceed as follows:

   a. Use the SMS card location charts (Figures 100 and 101) to locate the current source card that corresponds to the point being scoped and replace it.

   b. The diverter column is the location being scoped (F04, F07, F08). The current source companion for each diverter is labeled current source (F10, F14, etc.). All decodes receiving current from each set of source and diverter cards are listed along with controlling digit of address.

   c. Always replace the current source card first, even if the wave form observed indicates a bad diverter because most diverter card damage is caused by the source cards.

   d. Recheck the wave form after replacing the source card and if still wrong, replace the diverter.

7. Wave form 9 will occur if an addressed decode switch is open. Correlate the diverter location (the point being probed) with the address-selection switch setting to determine the location of the open decode.

   Note: Addressing the open decode switches can cause damage to the clamping diode in the current source card. Clamping diode or resistor damage in the source card can be recognized by a positive turn on the peak of approximately +42, instead of +30v, as shown in scope pictures 1, 2, and 3.

8000 - 11999 GATE 06B1

ADDRESS	DECODE	DIVERTER	CURRENT SOURCE	ADDRESS	DECODE	DIVERTER	CURRENT SOURCE
XXX0	E13			81XX			
XXX1	E13			83XX			
XXX2	E14			85XX	E09		
XXX3	E14			87XX			
XXX4	E15	F08	F16	89XX			
XXX5	E15			90XX			
XXX6	E16			92XX			
XXX7	E16			94XX	E10		
XXX8	E17			96XX			
XXX9	E17			98XX			
XX0X	E04			91XX			
XX1X	E04			93XX			
XX2X	E05			95XX	E10		
XX3X	E05			97XX			
XX4X	E06	F05	F12	99XX			
XX5X	E06			100XX			
XX6X	E07			102XX			
XX7X	E07			104XX	E11	F04	F10
XX8X	E08			106XX			
XX9X	E08			108XX			
X0XX	E23			101XX			
X1XX	E23			103XX			
X2XX	E24			105XX	E11		
X3XX				107XX			
X4XX	E24	F07	F14	109XX			
X5XX				110XX			
X6XX	E25			112XX			
X7XX				114XX	E12		
X8XX	E25			116XX			
X9XX				118XX			
80XX				111XX			
82XX				113XX			
84XX	E09	F04	F10	115XX	E12		
86XX				117XX			
88XX				119XX			

12000 - 15999 GATE 06B5

ADDRESS	DECODE	DIVERTER	CURRENT SOURCE	ADDRESS	DECODE	DIVERTER	CURRENT SOURCE
XXX0	E13			121XX			
XXX1	E13			123XX			
XXX2	E14			125XX	E09		
XXX3	E14			127XX			
XXX4	E15	F08	F16	129XX			
XXX5	E15			130XX			
XXX6	E16			132XX			
XXX7	E16			134XX	E10		
XXX8	E17			136XX			
XXX9	E17			138XX			
XX0X	E04			131XX			
XX1X	E04			133XX			
XX2X	E05			135XX	E10		
XX3X	E05			137XX			
XX4X	E06	F05	F12	139XX			
XX5X	E06			140XX			
XX6X	E07			142XX			
XX7X	E07			144XX	E11	F04	F10
XX8X	E08			146XX			
XX9X	E08			148XX			
X0XX	E18			141XX			
X1XX	E18			143XX			
X2XX	E19			145XX	E11		
X3XX				147XX			
X4XX	E19	F07	F14	149XX			
X5XX				150XX			
X6XX	E20			152XX			
X7XX				154XX	E12		
X8XX	E20			156XX			
X9XX				158XX			
120XX				151XX			
122XX				153XX			
124XX	E09	F04	F10	155XX	E12		
126XX				157XX			
128XX				159XX			

Figure 100. Current Source SMS Locations

0000 - 3999 GATE 01A1

ADDRESS	DECODE	DIVERTER	CURRENT SOURCE
XXX0	E13	F08	F16
XXX1	E13		
XXX2	E14		
XXX3	E14		
XXX4	E15		
XXX5	E15		
XXX6	E16		
XXX7	E16		
XXX8	E17		
XXX9	E17	(F22)	(F17)
XX0X	E04	F05	F12
XX1X	E04		
XX2X	E05		
XX3X	E05		
XX4X	E06		
XX5X	E06		
XX6X	E07		
XX7X	E07		
XX8X	E08		
XX9X	E08	(F12)	(F07)
X0XX	E18	F07	F14
X1XX	E18		
X2XX	E19		
X3XX			
X4XX	E19		
X5XX			
X6XX	E20		
X7XX			
X8XX	E20		
X9XX		(F20)	(F14)
00XX	E09	F04	F10
02XX			
04XX			
06XX			
08XX		(F10)	(F04)

ADDRESS	DECODE	DIVERTER	CURRENT SOURCE
01XX	E09	F04	F10
03XX			
05XX			
07XX			
09XX			
10XX	E10		
12XX			
14XX			
16XX			
18XX			
11XX	E10		
13XX			
15XX			
17XX			
19XX			
20XX	E11		
22XX			
24XX			
26XX			
28XX			
21XX	E11		
23XX			
25XX			
27XX			
29XX			
30XX	E12		
32XX			
34XX			
36XX			
38XX			
31XX	E12		
33XX			
35XX			
37XX			
39XX			

4000 - 7999 GATE 06B1

ADDRESS	DECODE	DIVERTER	CURRENT SOURCE
XXX0	E13	F08	F16
XXX1	E13		
XXX2	E14		
XXX3	E14		
XXX4	E15		
XXX5	E15		
XXX6	E16		
XXX7	E16		
XXX8	E17		
XXX9	E17		
XX0X	E04	F05	F12
XX1X	E04		
XX2X	E05		
XX3X	E05		
XX4X	E06		
XX5X	E06		
XX6X	E07		
XX7X	E07		
XX8X	E08		
XX9X	E08		
X0XX	E18	F07	F14
X1XX	E18		
X2XX	E19		
X3XX			
X4XX	E19		
X5XX			
X6XX	E20		
X7XX			
X8XX	E20		
X9XX			
40XX	E09	F04	F10
42XX			
44XX			
46XX			
48XX			

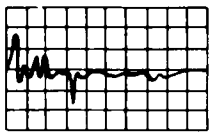
ADDRESS	DECODE	DIVERTER	CURRENT SOURCE
41XX	E09	F04	F10
43XX			
45XX			
47XX			
49XX			
50XX	E10		
52XX			
54XX			
56XX			
58XX			
51XX	E10		
53XX			
55XX			
57XX			
59XX			
60XX	E11		
62XX			
64XX			
66XX			
68XX			
61XX	E11		
63XX			
65XX			
67XX			
69XX			
70XX	E12		
72XX			
74XX			
76XX			
78XX			
71XX	E12		
73XX			
75XX			
77XX			
79XX			

SMS CARD LOCATIONS FOR 10000 SERIES: DIVERTER & SOURCE CARDS IN PARENTHESIS – SUBTRACT ONE FOR DECODES. EX.: E13 IS E12 ON 10000 SERIES

Figure 101. Current Source SMS Locations

A

Vert. Def. - 10V/Div.
Horiz. Def. - Approx 1 us/Div.
Sync. - Time 000 to 030
Test Point - 01A1-F05C or F08C
Logic - 42.57.11
Comment - Correct wave shape with one Decode switch conducting

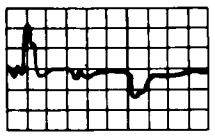


B

Vert. Def. - 10V/Div.
Horiz. Def.-Approx 1 us/Div.
Sync. - Time 000 to 030
Test Point - 01A1-F05C or F08C
Logic - 42.57.11
Comment - Incorrect wave shape, two decode switches conducting

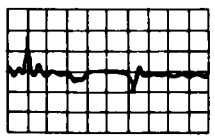
C

Vert. Def. - 10V/Div.
Horiz. Def. - Approx 1 us/Div.
Sync. - Time 000 to 030
Test Point - 01A1-F05C or F08C
Logic 42.57.11
Comment - Incorrect wave shape, no decode switches conducting



D

Vert. Def. - 10V/Div.
Horiz. Def.-Approx 1 us/Div.
Sync. Time 000 to 030
Test Point - 01A1-F04C or F07C
Logic - 42.57.11
Comment - Correct wave shape with one decode switch conducting



E

Vert. Def. - 10V/Div.
Horiz. Def. - Approx 1 us/Div.
Sync. - Time 000 to 030
Test Point - 01A1-F04C or F07C
Logic - 42.57.11
Comment - Incorrect wave shape, two decode switches conducting

F

Vert. Def. - 10V/Div.
Horiz. Def. - Approx 1 us/Div.
Sync. - Time 000 to 030
Test Point - 01A1-F04C or F07C
Logic - 42.57.11
Comment - Incorrect wave shape, no decode switch conducting

Figure 102. Decode Output Wave Forms

8. Shorted decodes have no effect on the wave forms. Current available to each decode matrix is controlled by the 18v differential setting. Shorted decodes conduct all the time and, therefore, cause a sharing of current except when the shorted decode is addressed. If all addresses except one for any current source fail, the decode address that is not failing is probably shorted.

This procedure and wave forms can be applied to 10000 Series 1401's even though SMS card locations vary. The diverter and source card locations for 10000 Series are in parentheses in their respective blocks. Subtract one from the decode switch location for 10000 Series.

Figure 102 shows the wave shape for a selected and unselected decode switch. When the machine is running, the selected decode must be at ground level 1 microsecond before time 0. The wave shape of an unselected decode switch and the output of the current diverter are the same, because electrically they are at the same point. Other decodes can be scoped to insure being off. Figure 102 shows the decode outputs with one or more decode switches conducting.

Interference

Highly intermittent storage failures can be caused by outside radiation such as a radar beam. This is unusual but merits consideration.

Presense-Amplifier Check

Checking core storage and presense amplifiers, it is possible to pull the inhibit driver for that bit. Each time the cores are addressed there should be an output on the amplifier. For checking row bits, remove the inhibit driver, logic 42.58.11, and the row bits can be checked at 1401 speed.

Changing Strobe Time

Before changing the strobe time, check the timing of R1, R2, and R3. The strobe can be varied by the delay card. Each step on the delay card gives a 0.2 microsecond variation.

Missing and Extra Bits

The current required to flip cores varies slightly according to room temperature. Therefore, if you are missing bits, increase the difference between the plus 30v and the plus 12v supply. If you are getting extra bits, decrease this difference. In any case, set the plus 30v supply first and then vary the plus 12v supply as it is referenced to the plus 30v. A more detailed explanation can be found under the storage gate voltages in the *Power Supply Service Aid* section.

Sense-Line Check

Sense lines for any one bit have two circuits just as the inhibit has two lines (above and below 2k). These two sense lines are common on the front of the storage and then go to the pre-amplifier for that bit.

Decode-Switch and Current-Driver Check

Decode switches can be damaged by changing address switches while entering information. After the decode switches have been checked and trouble is still pres-

ent, it is highly probable the trouble lies in the current drivers. If intermittent problems are experienced in one specific plane and changing cards does not clear up the trouble, try switching the terminating resistors. Also, check the plane in error for cold solder joints at input and output connections.

Address-Register Signals

Checking the address-register signals to the storage-decode switches can be accomplished in storage-scan mode. Sync on the address stop and look at the address-register signals that appear on the storage-gate edge connectors. All signals should be at solid ground (plus U) one microsecond before 000 time. Investigate any signals with poor rise time.

Picking Up and Dropping a Specific Bit

Picking up or dropping a specific bit in any location is likely to be caused by a poor sense amplifier.

Faulty Decodes

Troubles peculiar to a specific address are usually due to faulty decodes.

Faulty Current Source

Troubles that cannot be pinned down to a specific bit or location can be caused by a faulty current source or faulty driver cards.

Sense-Amplifier Check

Sense-amplifier outputs for read 1, read 2, and punch can be checked by pulling the read 12 inhibit driver in 01A1 F23. Each position can be checked by doing a clear and branch operation, through the read and punch area. The address stop can be used as a sync point. Hammer fire can be checked in the same way but there is no inhibit driver to pull.

Intermittent Storage Failures

Intermittent storage failures can be caused by faulty convert blocks or inverters between the storage address latches and the address decodes. The symptom of this trouble is usually that all or parts of bits fail to read out. It sometimes reads out manually. It can also be due to slow latches.

50 and 80 Addressing

Keep in mind when determining whether the 8 × 10 or the 5 × 10 matrix is failing, usually what appears to be working is actually failing. If 50 addresses are failing, the 8 × 10 matrix output is bad and if 80 addresses are failing, the 5 × 10 matrix output is at fault.

Clock and Control Pulses

R1 time	—U	000-036	F02A	
R2 time	—U	008-075	F02B	
R3 time	—U	015-075	F02C	All on Gate 01A1
Strobe	—T	014-030	F02D	
Z1 time	—U	068-105		
Z2 time	—U	068-105		

When troubleshooting in core, a current probe is of great assistance. The new current probe part number is 451213 and the terminator is 451214. Note that the probe head can be grounded when open. Take care to prevent damage to the core.

Procedure for Adjusting 1401 Storage Pulses

There are four delay cards that are located by chassis 01B3, logic 31.12.93.2, and that are used in developing the storage-clock pulses. The locations of these cards and their functions are:

1. C06 delays the rise of —U R1.
2. C07 delays the fall of —U R2.
3. C09 delays the rise of +T, time 068-105.

The delay card used is adjustable in 0.2 μs steps from 0.2 to 1 μs. The following delay block shows the delays at the right of its output pins.

To adjust the delay, change the output wire of the delay block to a pin location that will give the desired delay. Record the change on the systems logics.

When adjusting the delays, observe the following tolerances:

Storage	*Pulse*	*Time (μs) after TR 1*
—U	000-036 R1	3.7 ± .2 trailing edge
—U	068-105	6.8 ± .1 leading edge
	2000	6.8 ± .1 leading edge
—U	068-105	0.8 ± .2 leading edge
	not 2000	1.7 ± .2 leading edge
—U	008-075 R2	
—T	014-030 strobe	

These timings are referenced to the fall of —TR 1 on 01B3 pin B21F and the delays are measured at the 50% level. Figures 99 and 102 have several storage-scope patterns along with the locations from which they were taken.

Procedure for Removing the Core Assembly

The procedure suggested for removing the core-unit assembly is:

1. Remove all power from the machine.

2. Remove the edge connectors row G from the 1402 and 1403, if no print buffer is installed.
3. Remove the signal cables, rows D, E, and F.
4. Remove four screws from the top of the core-storage frame.
5. Remove the wires to the fan and the ground wire.
6. Remove the muffin-fan unit.
7. Facing the front of the machine (console side), remove the two screws on the lower right-hand side of the core-unit mounting bracket.
8. Remove each voltage wire from the terminal block on the bottom of the core unit. The unit can be tilted to the rear for access to the terminal blocks. CAUTION: Label the location of each wire that is removed to insure correct reconnecting. This is important because reversing the voltage leads can cause damage to the core array.
9. Remove the unit from the side of the cube.

After changing the storage sense amplifiers or driver cards, recheck the marginal check limits of storage to find the new limits.

CPU Service Hints

Addressing Service Hints

Because the storage address register validity check bypasses the process-check stop switch to turn off the delta process, a solid or highly repetitive failure in the addressing system may be difficult to scope.

1. Clear storage to blanks by using the appropriate clear-to-blanks card 2, 4, or 6 from CE test block 0001A. Repeat several times, if necessary.
2. Load the address service aid card (stops with STAR at 038) or key in the following instruction.
   197 B 197 204 5 — (WM in 205 to define the end of the instruction.)

Note: This card can be punched as follows: (Start in column 1.) 008015, 022026, 033037, 205 L 044 204/099 B 1972045

3. Start the program at 197. Any erroneous addressing or I-ring trouble will result in:
   a. STAR address errors or
   b. Stops occur at I1 time due to lack of an op code (program did not go to 197). An analysis of all STARS compared with what they should contain, can lead to helpful conclusions about the trouble. If the machine stops because of lack of an op code, the hundreds positions of the A- and B-stars will be blank because they read an I1.

   If this particular instruction does not fail, move it to another area of storage with appropriate address alterations; for example:
   S97 B S97 T04 5 — (clear the old instruction).

I-Phase Troubles

Generally the machine cannot run, but sometimes it is possible to program a loop that will go along with the trouble. As an example, if you fail to get an I-star restore gate, a simple B001 program can be used. This branch op ignores the need for I-star restore, but does give a running loop for scoping.

Another example: If you find the trouble is modifier —1 during I-phase, simply write your program backwards (_ 500B with your WM in 001 and B in 005). This produces a running loop for scoping.

Always try to produce a program that ignores or goes along with the error so that you can scope a running loop. Address stop is generally a very effective scope sync, but remember that it is time 090 to 105 and, therefore, the preceding address must be used to be effective.

If the machine does not run, determine whether delta process is needed to scope the trouble. As an example, if it is impossible to reset one of the I-ring triggers to find the trouble, delta process is not needed. Simply pressing the start-reset key should reset the trigger. If it does not, the scope can now be used as a voltmeter to find the trouble. If an external sync is needed, time can be used as an effective sync.

If delta process is required to find the trouble during single-cycle process, remember that delta process is on for one cycle only. Therefore, if we are looking for a set or a reset line to the trouble, and this set or reset line is mixed with delta process, seeing the trouble on the scope is almost impossible unless we use internal sync.

As an example, if the trouble was determined to be an I/E change at I1 time, remember that any gating out of the B-register on I-cycle is mixed with process, and the actual reset of delta I is mixed with process. Therefore, it is necessary to determine the origin of the trouble.

In some cases the extender can be used to isolate a suspected line causing a trouble. Here, the voltage level of the suspected line must be taken into consideration. Remember an open line is a plus U level. Also, T-level lines sometimes behave strangely when floated.

E-Phase Troubles

Usually E-phase bugs can be scoped in running loops if the check-stop switch is off. The tighter the program loop that you can produce to create the error, the more advantageous it will be. Alter data to narrow your field of error. Through proper alteration of data, it is sometimes possible to pin-point your failure without scoping. If you have done this, and conclude that this is the trouble, swap cards. If it corrects or at least alters the error condition, your conclusion is justified, so replace the suspected card. If the trouble is still present with a new card, start scoping. Do no overlook the possibility, however, that some new cards may be defective. If the first analysis was wrong, get the scope. Do not spend extra time swapping cards in the suspected area. Remember, there is always the possibility that you drew the wrong conclusion.

Check the A-field and B-field. See if the fields after programming are what they should be. Some errors can pass process check without doing the job called for by the program. For instance, in a move-digit operation, it is possible that the whole A-register might be inhibited back without error, because the C-bit generator is activated. This would produce erroneous results without possibly producing an error. Observe the star addresses and the data fields closely. Do not *assume* what the results should be; know what they are.

On E-phase bugs, a running loop can, in general, be used. Once again, address stop is a good scope sync. Do not forget that address stop can be ANDed with

some other condition to produce the results needed (refer to ALD 32.45.31). In complement add, one B-address might be called upon three times. Here address stop would be useless, because you would never know which cycle was on the scope. If your trouble occurred during re-address, as an example, then it would be possible to AND the re-address with address stop for a good scope sync. This would pick out the one B-cycle during re-address in which the trouble is occurring.

An extender can be used to eliminate a suspected cause of the trouble. Remember, however, the pitfalls of floating a line.

Items That Can Be Checked in Alter Mode

Several areas of the addressing system can be checked out without maintaining a run status.

Set the contents of the address switches into the storage address register by pressing the start key.

1. The address-stop-compare, the address-stop latch and the address sync can be checked because the clock is running and the serial gates are active. The scope sync to check this should be a timing pulse.

   Example: —T time 000-015, available at 01A8 D18F.

2. The storage-address decode switches on logics 42.53.11.2, 42.54.11.2, 42.55.11.2, and 42.56.11.2 can be checked for static response.

3. The storage-address register validity-check circuitry can be checked for dynamic response up to the output of the gate inverter at 01A8 C01P in location 3C, on logic 32.44.51.2. The scope sync could be +U time 000-060, available at 01A8 C03H. There should be no output on the inverter at 01A8 C01P. The input pin D should be at the —T level prior to the +U not-oscillator pulse on pin F for each of units, tens and hundreds check.

4. Because ALTER MODE forces the modifier-control transfer, a dynamic check of the modifier transfer function can be made.

5. To check for a transfer between the A-, B-, or I-star and the address register set to ALTER MODE, place the desired address in the manual address switches, press the desired star key and press the enter key. This places the desired address in the STAR and the address register and continuously loops the address from switches to ADDRESS REG and back to STAR through the modifier.

   To check the STAR, restore the enter key to normal. The serial gates, not-function generator, modifier output, set controls for star, and the star reset can be scoped with the above procedure.

To check the operation of the storage address registers:

1. Check the B-star and star.
   a. Place the mode switch in storage scan, and press and hold the start key.
   b. Sync, using CE sync point with address switches set to the appropriate address.

   The following functions can be checked:

   a. Reset pulses to B-star and star.
   b. Set pulse to B-star and star.
   c. Modification by plus one with units-tens-hundreds-carry.

2. Check the I-star and star.
   a. Program the 1401 with no op and branch op to keep in I-cycle.

   The following functions can be checked:

   a. Reset pulses to I-star and star.
   b. Set pulses to B-star and star.
   c. Restore cycle of I-star.
   d. Modification by plus one with units-tens-hundreds-carry.

3. Check the modifier.
   a. Program the 1401 with the following type of program: C III AAA.

   The following functions can be checked:

   a. Modification by minus one.
   b. Units-tens-hundreds-borrow.

4. Check the A-star and star.
   a. Program the 1401 with an operation of the following type: M I 99 I 98 and branch back.
   b. AND delta A-cycle with CE sync point to insure that the first complete cycle that appears on the scope will be an A-cycle of an address that appears on the console switches.

Add and Subtract Operations — A (AAA) (BBB) or S (AAA) (BBB)

On operations where recomplementing does not occur, there is only one forward scan, and the following signals can be used as sync points for scoping operations:

Signal	*To Display*
+U transfer star	First A + B
+U 2nd B Tr	Second A and B
CE test point in conjunction with the setting of the manual add switch, logic page 32.45.31.2	Any A or B other than the first or second.

During operations where recomplementing does occur, there is a reverse scan and a second forward scan, and the following signals can be used as sync points:

Signal	*To Display*
+U transfer star	First A and B
+U 2nd B	Second A and B
Second B Tr going OFF	Remainder of 1st For Scan
Arith Readdress	Reverse Scan
Wire —T CY CTRL RVS SCAN to condition CE test point, logic page 32.45.31.2	Individual A and B cycles occurring during the reverse scan
Reverse Scan Tr going OFF	Second forward scan

Because the original B-field is destroyed as a result of the A or S operation, the program loop used for testing should include a load operation to re-establish the B-field before the arithmetic operation takes place.

Add or subtract functions to observe are: first B-cycle Tr, second B-cycle Tr, complement latch, arithmetic re-address, a WM latch, reverse scan Tr, re-complement latch, reverse scan re-address, re-address Tr.

FIRST B-CYCLE TR

This is turned on during the last I-cycle of any A or S op, and turned off at 075 of the first B cycle. It can be turned on again in a recomplement operation by CYCLE CTRL RVS SCAN DELAY.

SECOND B-CYCLE TR

This is turned on when first B-cycle Tr goes off and the recomplement latch is not on.

COMPLEMENT LATCH

This is turned on by an odd combination of minus signs. This is considering the SUB OP as a minus sign and the ADD OP as a + sign in combination with the A- and B-field signs.

ARITMETIC RE-ADDRESS

This is brought up by gated WM, if the operation is a complement operation and there is no adder-carry.

A WM LATCH

This is set by ARITH RE-ADDRESS.

REVERSE SCAN TR

This is set by ARITH RE-ADDRESS.

RECOMPLEMENT LATCH

This is set by CYC CTRL RVS SCAN.

REVERSE SCAN RE-ADDRESS

This is brought up by B-reg — B, during the reverse scan. It turns off REVERSE SCAN TR.

RE-ADDRESS TR

This turns on and off on alternate B-cycles, when recomplement latch is on, and cycle control reverse scan is off (second forward scan).

Edit

The following control signals are used during the edit operation.

EDIT A ELIMINATE

This is brought up on any B, during an edit operation when the B-register contains other than a blank or a zero.

EDIT FIRST A

This is brought up during the first B when the B-register contains a blank or a zero. It is the low-order blank position of the control word and is used to establish the body condition.

BODY TR

This is turned on by EDIT FIRST A and turned off by the coincidence of A WM latch, B, and B-REG FL or zero. The BODY TR defines the body portion of the edited word.

SET WM LATCH

This is turned on by the low-order zero in the control word.

ZERO SUPP LATCH

This is turned on by SET WM LATCH. It is turned off when a significant numerical digit enters the B-REG during the reverse scan. It can also be turned on by an alphabetic character encountered during the reverse scan.

FIRST EDIT RE-ADDRESS

This is brought up by B REG WM during the forward scan.

REVERSE SCAN TR

This is turned on by FIRST EDIT RE-ADDRESS. It is turned off at I-op.

Scope Loops

It is always advisable to scope a bug in a running loop whenever possible to produce a good scope sync. This provides an external sync for scoping a machine problem. External sync has the one big advantage over internal sync in that it produces a trace on the scope related to a known time. For instance, if the trouble was modifier +1 on *all* cycles, by using a simple program of M 111 222 B 001 __ with M in 001 and G in 111, there would be 2 cycles where modifier —1 would be normal.

If internal sync were used, nothing but dual traces would appear on the scope face. On the other hand, by using address stop set at 111 and sync time of 000, and by setting the scope time so that time 000 is produced at the beginning and ending of the scope face, anything scoped will be during the B-cycle only. Now

modifier +1 can be scoped, and the cause for its being up during a B-cycle can be found. External sync has now produced *one* cycle when modifier −1 is normal.

Inserting Loops in Customers' Programs

Sometimes diagnostic function tests pass, but a customer's program fails. If such is the case, pick out the trouble area in the customer's program. Here, reading the CE console will give you a clue where the trouble occurred. For instance, if a storage light occurred during an A-cycle, I-star would contain the last address +1 of the instruction, creating this error. At this point, it is necessary to get the customer's program and find the high-order position of the operation causing the failure. Now by re-addressing and single cycling on through the program, it is possible to determine whether it is a machine or program error.

If the trouble is an error under conditions peculiar to the customer's program, insert a branch in the customer's program at the end of the operation, branching back to the beginning of the operation. Use a no op to delete any portion of the program that could change the condition producing the error. Be sure to note *all* changes, and return the program to *normal* when you are finished.

Patch Routine

On certain intermittent troubles it is sometimes desirable for the customer to continue to operate while the symptoms are further investigated or parts are being obtained. This procedure is general and depends upon the customer's having the necessary unused storage space.

Assume that the printer is giving very intermittent sync checks. If this is a print buffer machine, new information is in the print area before the system stops. Reprinting the line that failed can require rerunning if it, for instance, was an accumulated total. One method that can prevent this rerun is to transfer the information to be printed into an unused area of storage in addition to putting it into the print area. If a failure was experienced, the customer can do a storage printout of the information that failed from the alternate area and then resume normal operation. The following is an example of how the program can be patched to accomplish this.

(Section from original program)

Core Location	*Op Code & Address*	*Description*
400	1	Read card
401	A AAA BBB	Add to existing totals
408	M AAA BBB	Move totals to print area
415	2	Print
416	Etc.	

(Patch routine)

Core Location	*Op Code & Address*	*Description*
400	1	Read Card
401	A AAA BBB	Add to existing totals
408	B 600	Branch to patch routine
415	2	Print
416	Etc.	
600	M AAA BBB	Move totals to print area
607	M AAA BBB	Move totals to alternate area
614	B 415	Return to main routine

Power-Supply Service Hints

Protection Circuits

A normal machine-power-off sequence or any machine fault that interrupts the sensing circuits in the 1401 causes the ac power to go off on all power supplies.

Line voltage remains on the following components or circuits:

1. Main-line circuit breakers
2. The primary side of the main-line contactor
3. Convenience outlets and associated circuitry
4. 115v ac and 24v ac step-down transformer primaries and associated circuitry
5. Tape connector
6. Terminal block TB1 (01B8).

When the emergency-off button is operated, the machine is in the same status as in the foregoing paragraph except that one leg of the ac input opens to the 115v ac step-down transformer, and voltage to the convenience outlets and associated circuitry is removed.

Power-Supply Troubleshooting Procedure

SYSTEMS BELOW 20,000

Power-supply problems can normally be divided into two groups. The most common is when one or more power-supply circuit breakers flip to the OFF position. In the second, no circuit breaker flips, but power does not hold up. With the first problem, go to *Step 4;* otherwise, proceed with *Step 1.*

Note: In the following steps, an asterisk indicates quick-check points.

STEP 1

1. With the power-on key held down, check to see if duo 11 on gate 02A4 and duo 12 on gate 02A6 close when power comes on. *Note:* If the customer engineer is working alone, the power can be held on by putting a jumper across the N/O and the common point of the power-on switch. If this does not hold the power on, check the storage array thermal switch, the output of the —20v supply, or the HD4 relay that is housed in the reader punch on A, B, and C models below 20150.
2. If duo 11 does not close, proceed to *Step 2.*
3. If duo 12 does not close, proceed to *Step 3.*

STEP 2

Duo 11 depends upon the folowing:

	Function Necessary	*Check Points*	
A	—6v dc	Gate 02A4	TB5-5, 6
*B	HD 10 closed	Gate 02A4	
C_1	From —5 to —7v dc (—12 supply output)	Gate 02A4	TB6-4
C_2	—20v dc direct	Gate 02A4	TB5-6
*D	HD 12 closed	Gate 02A4	
E_1	+30v dc direct	Gate 02A4	TB5-1
E_2	+6v dc	Gate 02A4	TB6-3
F	133v ac	Gate 02A4	TB9-18
		Gate 02A4	TB10-18
G	208v ac	See 1402 drawings for A, B, and C models.	

STEP 3

Duo 12 depends upon the following (for systems below 20253):

	Function Necessary	*Check Points*	
A	—36v dc	Gate 02A6	TB7-10
B	HD 13 closed	Gate 02A6	
C	—6v dc	Gate 02A6	TB8-2
D	HD14 closed	Gate 02A6	
E	From —5 to —5v dc (—12 supply output)	Gate 02A6	TB8-4
F	HD15 closed	Gate 02A6	
G	+6v dc	Gate 02A6	TB8-3
H	133v ac	Gate 02A3	585W REG TB1&4
I	208v ac	Gate 02A3	585W REG TB6&8
J	208v fuses	Gate 02A3	

STEP 4

If one or more circuit breakers flip to the OFF position when the power is applied, check their outputs for shorts to other voltage levels, as well as to ground.

Note: A good ohmmeter that can peg to zero resistance on the R × 1 scale must be used, because of the very low total resistance of the circuits. Look for dead shorts. The minimum resistance to be expected can be found by dividing the supply voltage by the maximum output current.

If the supplies on gate 02A3 or 02A6 flip, skip to *Step 5.* For supplies on 02A4 or 02A5, continue with *Step 4.*

Measure for shorts between the following points:

dc common ground	02A4	TB6-1
—6v	02A4	TB6-2
+6v	02A4	TB6-3
—12v	02A4	TB6-4
+30v direct	02A4	TB5-1
+30v sequence	02A4	TB5-2
—20v direct	02A4	TB5-6
—20v sequence	02A5	TB2-1

+6 and —12 can be shorted to any point in Step 5.

STEP 5

The check points for supplies on gates 02A3 and 02A6:

dc common ground	Gate 02A6	TB8-1
−6v	Gate 02A6	TB8-2
+6v	Gate 02A6	TB8-3
−12v	Gate 02A6	TB8-4
+30v direct	Gate 02A6	TB7-5
+30v sequence	Gate 02A4	TB5-1
−20v direct	Gate 01A6	TB7-6
−36v	Gate 02A6	TB7-10

All Step 5 voltages can be shorted to +6 and −12 check points in Step 4.

STEP 6

If a short is found on the output of a particular supply, remove two wires from the supply output. One wire goes directly to the laminated bus. The other goes to the assembly sequence. In most cases, this removes the laminated bus from the rest of the circuit. The exceptions are:

1. 6B on gate 02A4. An additional orange wire must be removed from TB9-4 on 02A4.
2. +6v on gate 02A5. An additional blue wire must be removed from TB9-1 on 02A4.
3. −12v on gate 02A5. An additional violet wire must be removed from TB10-1.

Note: The supplies in gates 02A3 and 6 serve the gates in frame 2. The supplies in gates 02A4 and 5 serve the gates in frame 1. Except for the +6v and −12v on 02A5, these supply their normal voltage to frame 1, and also marginal voltage to frames 1 and 2.

If the short is found on the wires going to the laminated bus, the next step is to remove the particular voltage from each gate in the given frame until the short disappears. Find the short on the last gate disconnected.

Measure voltages in the following order:

1. Measure −6v, +6v, and −12v at the gate location 01B3. Adjust to the proper levels. See the 1401 wiring diagram for location of supplies.
2. Measure −6v, +6v, −12v, +30v, and −36v at gate location 02B1 on the machines with tapes. If this feature is not present, measure at 02A7 or 02A8, depending on which is present. Adjust the correct supply according to wiring diagrams. If there are no tape adapter gates, −36 is not present and −30 must be set up on 01B3.
3. Measure −60v at 01B8 on the −60v bus bar, and adjust the supply in the 1402. In Model D, the supply is found on 01B4.
4. Measure −20v at 01B2 position A240, and adjust the supply in the 1402. In Model D, supply is found on gate 02AB.
5. Measure +30v on 01A1 (and the 1406 core-array gates) at F26N.
6. Measure +12v fixed on 01A1 (and the 1406 core-array gates) at F26Q.
7. Measure +12 variable (18v differential) on 01A1 (and the 1406 core-array gates) at F16Q. Optimum voltage for the +12 is noted on decals for each core array.

Note: Always adjust −12v after −6v. Always adjust +12v after +30v. The marginal voltages are not measured. They should be within tolerance if these steps are followed.

Grounding Ferroresonant Capacitors

A safety hazard on 1401 SMS power supplies can expose servicing personnel to electrical shock. To eliminate this condition, remove power from the system and ground capacitors in gate 02A3 as follows:

1. Remove the dummy heat sink, standoff studs, and capacitor cover.
   Remove the paint from the top rim of all capacitors.
2. Replace removed parts and add grounding wire, 598363 or equivalent, between the standoff studs and the slide-rail screw.
3. On a Model D, the 1250 watt capacitors are located in gate 02A7. The same procedure as noted in items *1* and *2* must also apply.
4. After installation, there should be less than one ohm resistance from each capacitor case to the frame ground.

Excessive SMS Power-Supply Voltage

1. If the voltage is too high and cannot be varied by the adjusting control, check for shorted series power-supply transistors (located on the large power-supply heat sink).
2. If the output voltage is high and CB1 did not trip, replace the overvoltage protective device, 208960 (if machine is so equipped).

If TAU-2, measure −36 at 02B2.
−60v located in 1402. Model D location 01B4. Measure at 01B8 on −60v bus bar.
−20v located in 1402. Model D location 02A8. Measure at 01A2 A24Q.

Portable Marginal-Check Power Supply

A portable marginal-checking power supply is furnished with 1401 systems with serial number 25588 or later. The gate selection switches for marginal voltages have been eliminated. The portable marginal-check power supply will be stored in the lower left of the 1402 in the area left vacant by the elimination of fixed marginal-check supply.

OPERATING INSTRUCTIONS

1. Plug N/C supply into 1401 convenience outlet.
2. Insert output cable into the voltage jack for the marginal voltage to be varied (02A4).
3. Using meter to check for voltage variation, adjust potentiometer for desired variations. Machine should operate with ±1.2 volt variation on all marginal voltages.

CAUTIONS

1. Voltage-control potentiometer must be fully counterclockwise when you insert or remove output jack.
2. Voltage-control knob must be fully counterclockwise when switching from buck to boost.
3. Do not jumper marginal voltages to gate 01B5. Marginal voltages are present on this gate to protect hammer-driver fuses.

Three-Volt Marginal Power Supply

When the voltage-selection jack plug is in the rest or remote position, varying of the adjusting potentiometer will trip the circuit breaker in the ±3 volt marginal supply. This is a safety feature to prevent jack plugging a voltage with the 3-volt supply adjusted away from zero volts. Immediately before marginal testing, be sure the potentiometer is set at zero volts; then check this circuit breaker to be sure that it is in the ON position.

Storage Gate Voltages (1401 and 1406)

Use the following procedure to set 1401 and 1406 Storage Gate voltages properly and to perform voltage variations.

SYSTEMS BELOW SERIAL 20000

1. Measure the +30v at 01A1 F26N and the +12v at 01A1 F26Q.
2. Adjust the +30v supply to +30v and the +12v supply to +12v.
3. Vary the +12v, plus and minus one volt, while running the core-storage worst pattern deck 9100. Run the test for one minute at both the +11v and +13v setting. If the test runs without errors, proceed to Step 5.
4. If there is difficulty in meeting the limits just mentioned, the +12v supply can be adjusted up to a maximum of one volt in either direction to a point where the plus and minus one-volt variation do not produce any errors. Do not exceed the limits of +10 and +14 for the +42v.
5. Record the final setting for the +12v on the tag near the pot. Periodic voltage variations during PM can be accomplished by varying the +12v plus and minus one volt around this setting.

SYSTEMS ABOVE SERIAL 20000

1. Measure the +30v at 01A1 F26N, the +12v fixed at 01A1 F26Q and the 18v differential (also known as the +12v variable) at 01A1 F13Q.
2. Adjust the +30 supply to +30, the +12v fixed to +12v, and the 18v differential supply to +12v, with respect to ground.
3. Set up the marginal-check voltage supply to vary the +30M and vary the +30M plus and minus one volt while running core-storage worst pattern test 9100. Test should run for one minute without error at the +29v and +31v settings.
4. If there is difficulty in meeting the limits, the 18v differential output can be adjusted up to a maximum of ½ volt in either direction from +12v to the point where the +30M can be varied plus and minus one volt without errors. Record the final setting in the installation manual. (San Jose systems do not have a tag on the power supply.)
5. If the system has a 1406, follow the same procedure. In the 1406, there is one +30v supply, one +12v supply, and two 18v differential supplies. In the case of a 16k system, there is one 18v differential supply for each storage gate.
6. Measure the +30v at 06B1 F26N, the +12v at 06B1 F26Q; and the 18v differential for 06B1 at 06B1 F13Q, and for 06B5 at 06B5 F13Q. Always adjust the +30v before the 18v differential.
7. To vary the +30M in the 1406, the remote marginal cable or the portable marginal-check power supply must be used. Remember, the +30M will be varied for the entire 1406. If you want to run marginals on only one 1406 storage gate at a time, the 18v differential supply for that gate can be varied plus and minus one volt instead of the +30M.

Note: On systems below 20000, there is one +12v supply. When the +30v supply is varied, the +12v supply remains very close to +12v. On systems above serial 20000, there is an additional +12v supply called the 18v differential. Under normal operation, the 18v differential output varies with the +30v supply and maintains an 18v differential between the two supplies. When the +30M is varied, the output of the 18v differential remains at 12v.

CAUTION: When varying the +30M, do not attempt to get the full swing on the potentiometer. Nothing is gained, and there is the possibility of decreasing the life of the driver cards. Plus and minus 1.5 should be the maximum allowable variation on the +30M.

Noise

The scope must be plugged into the machine unit in which the check is made.

The probe must be grounded to circuit ground, not machine ground, as close as possible to the circuit being observed. When proper grounding is not observed, noise is exaggerated.

POWER-SUPPLY NOISE

The most common example of this is the noise on the power supplies from the clock distribution gates. It should be suitably filtered. Additional filtering can be obtained on any gate by plugging in a GJ— general-purpose filter card, 371501. Noise should not exceed 2% peak to peak at the power supply, 4% peak to peak at the gate.

SWITCHING SPIKES

These are caused by logic switching. *Example:* In a two way —AND circuit, one leg goes plus as the other leg goes minus. The plus-going leg can switch slow, or the minus-going leg can switch fast. Either can cause a very short pulse or spike. This type of noise is fixed in time to the machine clock.

A switching spike may not have been removed, because it has been switched out of succeeding logic, so it cannot cause trouble. It probably cannot be removed without a circuit change. Mark the size and shape of the spike in the logic so that it won't bother you again. *Example:* X-gate, on systems above 20000, 36.17.11 4C pin H has a switching spike that does not cause trouble. The switching spike occurs on —T hundreds 0 line — pin L and is a result of the main star set-and-reset circuits. This line is not a good sync point, however, because the spike would trigger the scope every clock cycle. The units at 4B and 5B provide X-gate sync.

A switching spike can cause machine trouble. This is a result of a circuit operating improperly (usually too slow, but can be too fast). The scope must be calibrated to the machine time base, and careful analysis made of circuit delays to determine the component that must be replaced. Replacing any component in the immediate circuit may make the machine work *for a while.*

True Noise

This noise is not related to the machine clock. It comes from clutches, switches, or relays.

Try to determine the general time of the noise within the general program loop. Because of the nature of mechanical operations and differences in time base of mechanical operations, compared to 1401 cycles, there can be quite a variation of time and still fall within the same general area of the program loop. It can also be quite intermittent. Try to relate it to a specific input or output unit.

If it cannot be related at all to the program in time, it may be some component in a mechanism that is not necessarily in synchronism with the program. *Example:* 1403 ribbon-reversing switch, 729 head-up switch.

Relating Noise to Machine Index

This is usually too short to fire the dynamic timer.

1. Sync the external position on a known circuit-breaker time.
2. Calibrate the time base to the machine-cycle time.
3. Observe the suspected line, and determine cycle time from graticule divisions.
4. After you get a rough location, you may choose a better sync, and reduce the time base for a better picture.

If a 535/545 scope is available, and the line does not have normal signals on it, this method can be used:

1. Sync internal use 1 ms cm sweep speed.
2. Connect +gate main sweep scope hub to dynamic timer contact hub.
3. Connect the dynamic timer common to ground.
4. Probe the suspected line, and watch the timer dial. The light comes on where noise occurs, and remains on for the sweep of the scope.

Relay lines do not make good sync points, because of the inductive spike when the coil is de-energized. It causes an additional sweep. If a relay line must be used and does not have spike suppression, the spike can be eliminated at the scope-sync hub (spike will not be eliminated in machine) as shown in Figure 103.

Ripple

Acceptable ripple is 2% peak to peak at supply or 4% peak to peak at gate.

If ripple is present:
Replace the SMS amplifier card.
Check the filter capacitors.
Check the rectifiers.

Bad Power Supply

If unable to turn power on, a power-supply circuit breaker is probably tripped, and must be reset.

If no CB's are tripped, the thermal switch over core storage may be open. Check it with a meter.

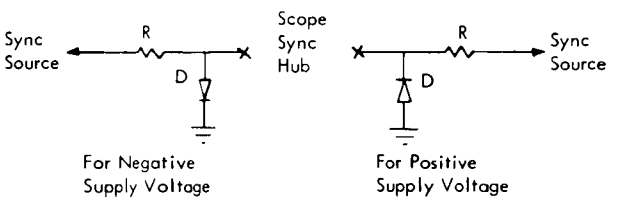


Figure 103. Relay Sync Circuit

If unable to sequence on, refer to *Power-Supply Troubleshooting Procedure.*

If the output voltage of a supply is high and cannot be varied, check for shorted series-power-supply transistors on the heat sink.

If the output voltage is high and circuit breaker 1 did not trip, replace the overvoltage assembly.

If trouble is in the individual power supply, some of the following points can be useful:

1. There is a ninety percent chance the trouble is the SMS card (low or no voltage with no adjustment of output voltage).
2. If the voltage is high with no adjustment, one of the series regulator transistors is shorted (or the SMS card is bad).
3. With the power supply removed, you can wire 110 Vac into TB1 pins 1 and 2. Output may not reach full value, but should be close and adjustable (remove overvoltage device).
4. Visually inspect the unit for crimped wires or cable chafing on the screw ends. (The unit may work in the opened position, but not in closed.)
5. An open diode in the rectifier circuit shows up as low voltage under load. Also, this can be detected by feeling the diodes; they are quite warm when operating normally. If one is colder, it is open. *(Output ripple should not exceed 20 mv).*
6. A shorted diode in the rectifier circuit will probably pop the circuit breaker in the primary of the input transformer, but not necessarily. It may pop the over-current CB because of overvoltage spikes on the output. With the overvoltage devise removed, the spikes are visible.
7. A shorted or open series regulator transistor can be detected by scoping or feeling the resistors in their emitter circuit.
8. Check voltages after the machine has been on for 15 minutes. Voltage drifts slightly between cold and warm states.
9. Do not ground the heat sink. (Instead, ground to the holding screws at the corners of the unit.)

Current Problems

Caution: A safety hazard exists at the top cable group that feeds the indicator lamps on the operator's panel. These are the optional-feature lamp wires which are taped-off at the ends with Scotch Electrical Tape*. The tape sometimes falls off, exposing the bare ends of the wires which have −12v on them. They can then ground out against the frame as the op panel door is opened, and blow out a paddle-plug connection, located at 01A1 A24A. Because this is the main source of −12v for the panel switches and other voltages are still on, the storage-address decode switches overload and burn up until several are lost. This makes troubleshooting difficult. The time spent taping these wires a little better can save you much trouble later on.

* Minnesota Mining and Manufacturing Co.

Scoping the terminal board at the bottom of 01A1 is dangerous. Row-bit cores can be lost easily.

The power-off switch on the 1403 drops one leg of the three-phase power. It is designed to prevent 1403 power on for safety. If it is operated with 1401 power ON, the 1403 phase fuses usually blow. CAUTION: 230 Vac is still available on the 1403 with this switch off.

The vibration of heavy duty 1402 relays can cause spikes on voltages. Shock-mount them or decrease the armature-spring tension to correct this.

The inter-frame connectors at 02A0 can ground on the vertical support bar. Insulate with electrical tape (Figure 104.)

Intermittent Trouble Sources

1. A missing tie-down can cause intermittent failure or failure with slight voltage variation.
2. A loose terminal severs connections on the power-supply terminal board.
3. Poor cable grounds.

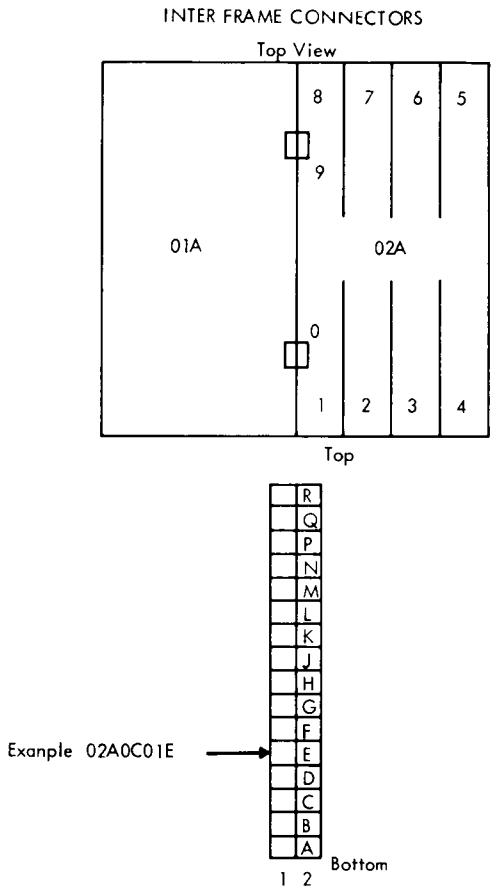


Figure 104. Interframe Connections

Tape-System Service Aids

Error Record Display

It is frequently necessary to display a tape record on which an error occurred. This can be accomplished as follows:

1. Backspace one record.
2. Assign tape drive 1.
3. Press the tape-load key.
4. Print out (location 001).

AC Erasing of Tape

The degausser can be used to erase a complete reel of tape. Energize the degausser, while at least 12 inches from the tape, and move in slowly. Move the degausser with a circular motion on a plane with the reel for about ten seconds. Retrieve the degausser slowly to prevent introduction of hum.

Dynamically Checking Tape for Defects

A machine may be experiencing write checks in a particular channel because of a bad spot on tape. A quick check of tape condition can be performed as follows:

1. Write continuously (all bits).
2. Scope suspected channel (sync internal).
3. A defect then appears as a *glitch* on the pattern (Figure 105).

The defect can be caused by an oxide particle, defective spot, tape crease, or tape flutter. (Tape flutter can be caused by improper head-wrap angle.)

False Neon Indication

The solid wire attached to the tape-selecting connector on gate 02A01, row A (tape-test panel), can be broken easily. This gives wrong indications on the tape-test panel neons. On later machines, this wire has been changed to a stranded wire that is not vulnerable to breakage.

U Op Code with A-Modifier

On 1401 systems with E. C. 109504, an op code of U with an A-modifier can be used to read tape, for example, U% U1A. This op code turns on manual read call and reads the tape but it does not place any information into storage. The instruction causes one record to be read. The TAU error trigger is turned on for an error, and a branch-on tape error (L-modifier) can be used.

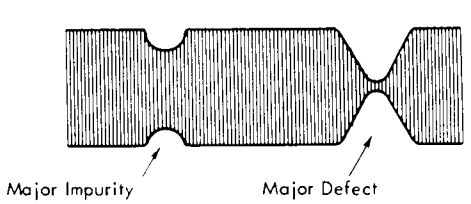


Figure 105. Tape Output Pattern

Using this instruction, verify tapes with regard to parity. The machine can be checked for this feature on systems logic 71.11.21.1. The units concerned are 5G, 5H, 5J, and 6G.

The results of this test must be tempered with the knowledge that some temporary (correctable) read errors should be expected. These errors usually do not stop the machines because they are read correctly on subsequent programmed re-read instructions.

Indicator-Lamp Check

All indicating lamps in TAU-2 (alloy TAU) can be checked at one time by removing the lead from 02A1 D01K and touching it to pin J.

Skew Checks

Skew checks can be caused by extreme differences in preamp settings within a given drive. This is generally noticed when one track is set very high (such as 10v peak-to-peak).

Start/Stop Timing

A fast method of putting a drive into the necessary start/stop mode of operation for checking start/stop time is to write tape in high density and read back in low density. This produces the desired tape motion without removing any cards or making any wiring changes.

Read and Write Errors

Intermittent read and write errors can be caused by broken or bent bond pins in the tape-unit power-cable heads or cable-connectors. Pin 3, which is about ⅛ to ¼ inches longer than the other pins, bends or breaks off in changing cables. This pin forms the bond between tape units. When the bond is missing, noise is often introduced on lines to and from the tape units, causing errors.

Erase Head

Problems can be experienced on erase-head installation on IBM 729's (B/M 585447 EC 248974) in that the AA2W card in D14 may not conduct properly when write status comes up. The instructions state to "Ground pin E to J" of D14. To reduce this card to a less critical circuit, tie pin E to F which will make a single input AND arrangement.

Failure to Go into a High-Speed Rewind

Failure of the IBM 729 to go into a high-speed rewind can sometimes be due to light passing through the black finger guard over the photo-sensing block. Because the new-type photocell has a clear glass side, this light can desensitize the circuit. Place some black friction tape on the inside of the cover over the photocell area.

Intermittent Read and Write Checks

Intermittent read and write checks can be caused by bent I/O shoe pins or pins that have been pushed out and fallen in back of the I/O shoe panel. The correction for bent or missing I/O shoe pins is obvious but bent or missing pins in one tape unit can cause failures in another tape unit on a 4- or 6-tape system and can be easily overlooked. When I/O shoe-connector troubles are suspected, check all connectors on all the tape units.

Use of Error-Stop Switch When Running Program

This is an example of using error-stop (on tape CE panel) while running programs.

1. Run the card-to-tape test with the mode switch on the D-position.
2. Turn the error-stop switch (CE tape panel) on.
3. Force a read-check-of-write error by turning down a preamp output. An error at this point freezes the read registers. Using the D-mode position with error-stop on the TAU panel only causes a freeze up as described on a write operation. To cause a freeze up on a read only, the circuit developing condition stop on error switch can be altered.

Mode Switch D Procedure

The mode switch D position blocks the C-bit generator. For example, when running a tape-to-printer operation, any out-of-parity character entering the 1401 from tape causes an inhibit error. Storage can now be scanned to analyze the bit configuration of the out-of-parity characters.

A procedure to display the tape record on which an error occurred is:

1. Backspace the tape one record.
2. Set the tape-unit address drum to 1.
3. Set the mode switch to N.
4. Press start-reset; then tape-load.
5. Print out starting in 001.

On binary tapes written for 704, 709, or 7090, the check character is always in even redundancy. This causes an A-skew register error so the B-skew register is used. Because the diagnostics do not write check characters, they cannot detect errors that occur on check characters.

Tape Skew

A quick way to check tape skew is to sync on first bit and look at the output of the A-register error-check circuits. All bits should be written and the error-circuit output should be 2 microseconds or less.

The following is a procedure for checking TAU-2 clipping:

1. Set up a continuous write operation; then reset at the tape drive.
2. With a dc meter referenced to −12v, measure pin A of the first final-amplifier card (AFC).
3. Now measure pin D. This should read between +1.20 and +1.31v. This completes the write-clipping check.
4. Now go to read continuous and reset at the tape drive.
5. Again with the dc meter referenced to −12v, measure pin A of the first final-amplifier card. This should read between −0.53 and −0.71v.
6. Now with the meter still referenced to −12v, measure the output pin D. This should read between +2.20 and +2.30v. This completes the usual dc clipping-level check.

The ceramic split guides can be the cause for skew errors and any other problems appearing to be tape alignment trouble. Oxide working its way up behind the spring-loaded rear guide can result in the guide becoming almost totally ineffective. All oxide buildup on the surface and between the guides should be removed periodically with a typewriter brush.

False Tape-Indicator Errors

Tape-indicate, when it appears to be false, can be caused in the following ways (see IBM 729 *Service Aid* CEM 12):

1. Variation in response of TI photocell. Select photocells for the shortest duration.
2. Backspace or rewind received just before the end-of-file reflective spot. Write forward before the back-spacing motion can cause the TI to come on. This is legitimate.
3. Noise, ground loops, and open grounds. Bent power or signal connector pins, in some cases not on the drive that is failing, can cause this.

Process Errors During Tape Operation

Tape drive problems, especially on sorts, can result in process errors. This is due to program utilization of the tape go-down time. These can be difficult to pin down. It is often best to tackle the problem in the following manner:

1. Thoroughly clean the tape drives.

2. Check and adjust all preamps to 8v peak-to-peak on high density.
3. Run the IRG diagnostic on all tape drives.
4. Analyze the results from each tape unit and correct any below-standard indications.
5. Should the problem still exist, check for noise or hash riding on the data lines from tape. This is often caused by bent or pushed-out shield pins in the tape-unit signal connectors. (For additional information on noise, refer to *IBM 729 Service Aids CEM's*, particularly CEM 61.)
6. Check TAU clipping levels.

Checking Base-Line Shift

While writing all bits in low density, connect the scope to the read lines and look for a shift of the base line not to exceed the specifications outline in the IBM *729 Reference Manual* (223-6868). A varying base line indicates a bad write-current driver card.

TAU levels swing from ground to either —6v or —12v. An acceptable level should be considered as follows:

ground	down to —0.65v
—6v	up to 5.8v
—12v	up to —8.8v (unless clamped to —6v)

In NAND TAU the rise time of the ac set must be approximately 70 nanoseconds. Usually a 0.1 microsecond rise causes no problems.

Delay-Counter Check

To check the delay counter in TAU-2 for free running, write with gaps with the slip-on connector at A26 of 02A1 grounded on a J-pin in 02A1.

Intermittent Tape Failure

A good test for intermittent tape failures is to erase an entire tape. Rewind and start from load point with a manual read. The first bit comes only from the A-register (high clip) so any noise or oscillating cards read into the B-register and are retained, because no clock cycles occur. If the B-register fills up with bits or picks up any bits, press reset and the manual read restarts to ascertain whether this noise leading into the B-register is a one-shot affair or is being picked up often. If one or more bits are picking up repeatedly, the read lines can now be scoped for this noise. When noise high enough to read into the A-register occurs, the tape clock starts, because of the first bit, and the tape stops. This condition can be ANDed to freeze up the error.

Checking L.R.C.R. Trigger

The setting of each L.R.C.R. Trigger is automatically checked on 1401's above serial 21196. At the start of every tape R/W operation, the TAU error latch and each L.R.C.R. trigger is turned on. These outputs are ANDed to gate on the final amplifiers. Failure of any trigger to turn on results in tape runaway on 7330 R/W operation and 729 read operations. A TAU hang-up condition occurs if an L.R.C.R. trigger fails to turn on at the start of a 729 tape write operation.

The L.R.C.R. Triggers may be checked as follows in systems prior to serial 21195.

1. Write a one-character record (all bits) from the CE panel in low density.
2. Backspace one record-change to high density and read the record.
3. All the L.R.C.R. triggers should be on at the end of the operation. This is due to the incompatibility of character density between the read and write operation performed which results in failure to read the check character.

Tape Adapter Unit (TAU-9)

Read

In this operation (Figure 106) TAU receives a read call and develops a tape-unit go signal that starts tape motion. A read delay, also initiated by read call, causes the tape unit to reach normal operating speed before reading data. After read delay, the TAU final amplifiers are conditioned to accept information.

Each character read from tape is level-sensed and sent to read registers A and B. The first character to enter the read registers turns the read clock on for a complete cycle. This clock furnishes timing and gating signals to control data flow through TAU during a read operation.

Data input to the read and write register is usually taken from read register A. If an error is detected in this register, the read clock conditions the read and write register to stop accepting information from read register A and to read register B (Figure 107).

After each character is read, the read clock (unless it is turned on by the next character) starts the end-of-operation action. This action includes processing the check character, resetting the read circuits, and stopping tape motion (Figure 108a, b, and c).

Read While Writing

In this action, the write-control circuits initiate a read operation while writing to check for writing errors. Reading while writing enables the operator to detect write-operation malfunctions, tape imperfections, and excessive noise immediately. This operation is essentially the same as a normal read operation except that data is not set into the read and write register, and all information checking is done at the read register.

Write

TAU receives a write call and develops a signal that starts tape motion (Figure 109). A write delay causes the tape unit to reach normal operating speed before writing data. The write clock is started by write call and conditions the read and write register to be on after write delay.

Write input-data lines set the read and write register and information becomes available to the tape unit. The write clock also generates a write pulse that is sent to the tape unit; this pulse is necessary to initiate writing.

TAU continues writing until interrupted by a disconnect call that completes the write operation.

Disconnect

Disconnect call is a signal generated by the system to end the write operation (Figure 109). This signal turns on the TAU disconnect trigger which, with the write clock (WC) 14, turns the write disconnect delay (WDD) trigger on and starts the delay counter stepping at the microsecond rate.

When the delay counter counts to WDD 60, the write-trigger release and the tape-unit write triggers are reset. All write triggers on at this time write a bit as they are reset, thus writing a check character.

Reset of the write trigger release when the WDD trigger is on causes the delay counter to step at the millisecond rate. When the delay counter has counted to WDD 20, both the go and WDD triggers are reset and the tape unit coasts to a stop. The write trigger remains ON until the read-check operation is completed to keep TAU in the busy status.

Backspace

The backspace operation is similar to a read operation, except that no data is transferred from tape to the system (Figure 110). A backspace call is initiated and the tape unit is in read status. TAU conditions the tape unit to move backward for one record and return to forward status. If the tape unit is in write status, TAU causes the tape to move forward and erase noise created by changing from read to write status.

Characters set into the read register during backspace start the read clock, which resets at the end of each character. When the end of record is reached, the read clock initiates action to stop backspacing and to set the tape unit in forward status.

The read and write register and TAU error-checking circuits are not conditioned on during this operation, because no data is made available to the system.

Rewind

Two rewind operations are possible in TAU: normal rewind and rewind unload. In the normal-rewind operation, a rewind call signal conditions the TAU rewind trigger. This trigger output is sent to the tape unit and initiates a rewind operation. When the tape unit goes into rewind status, the TAU rewind trigger is reset completing the operation.

For the rewind-unload operation, TAU initiates the tape-unload function by setting tape-unit control circuits to unload tape from the vacuum columns after the rewind operation is completed.

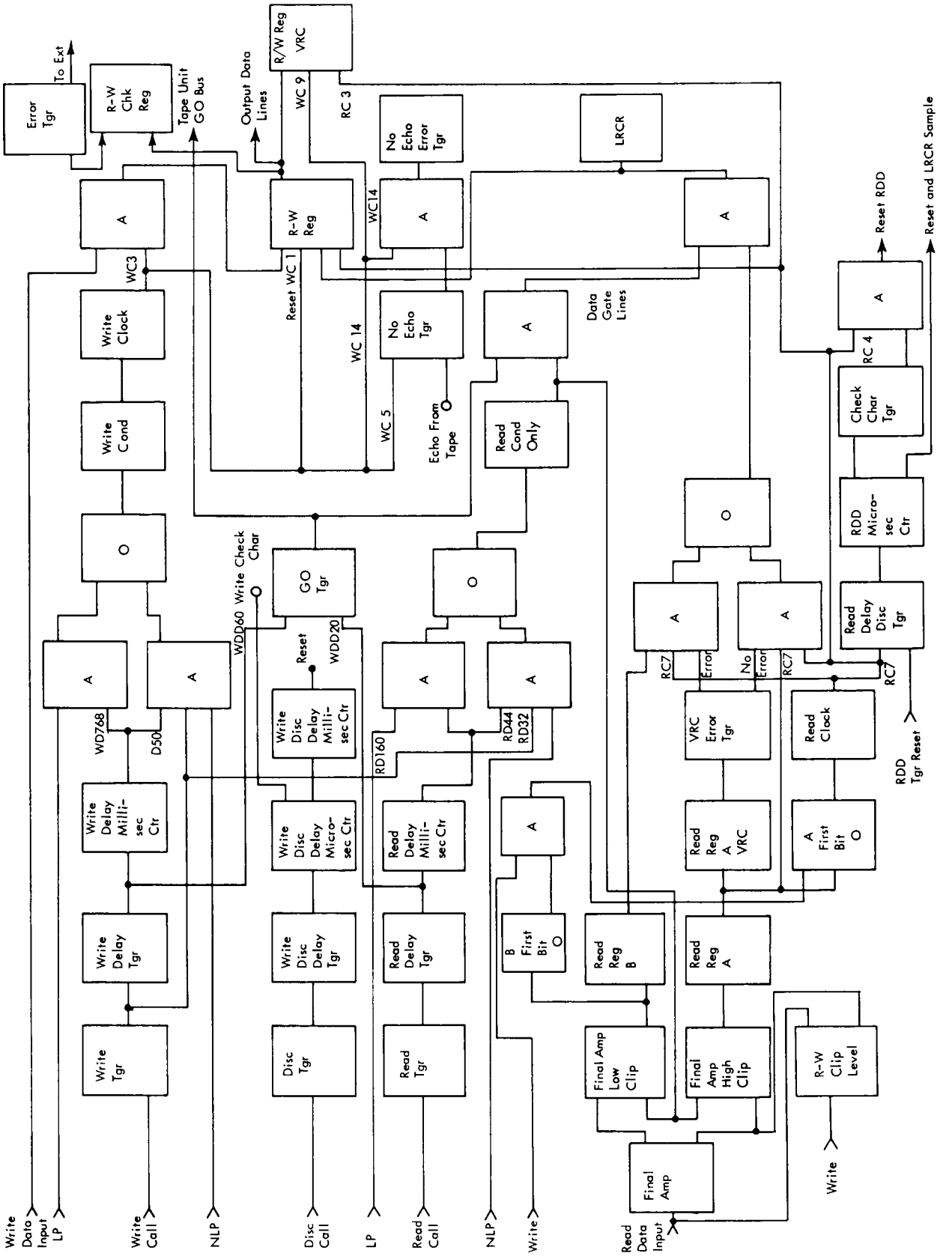


Figure 106. TAU Logic Flow

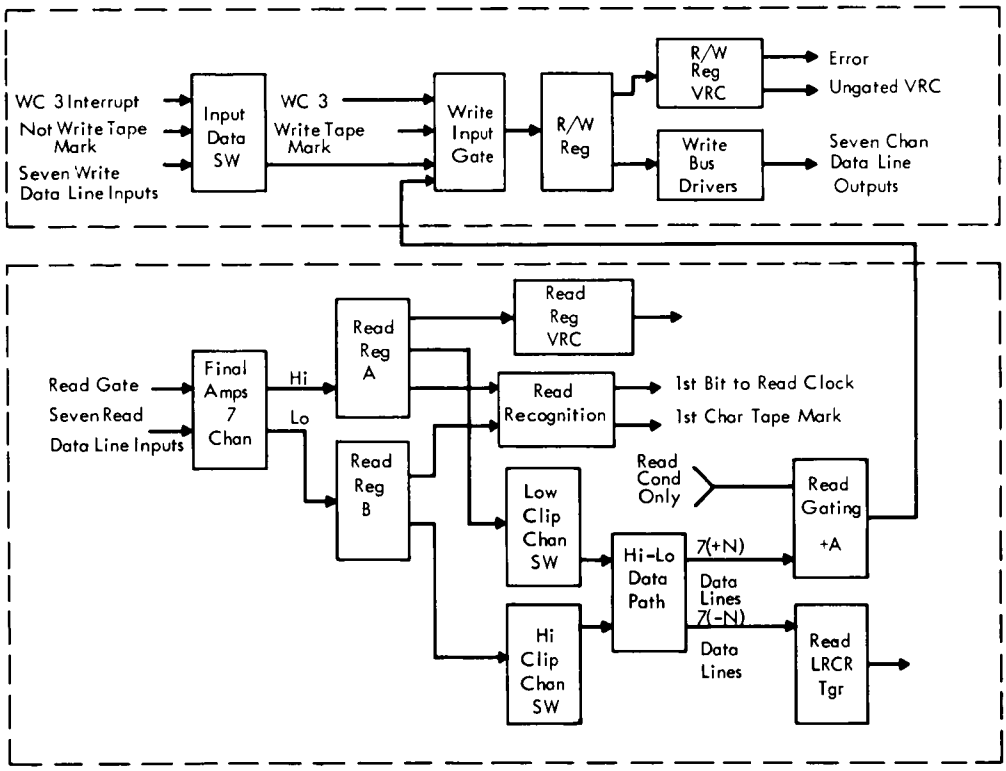


Figure 107. Read and Write Data Flow

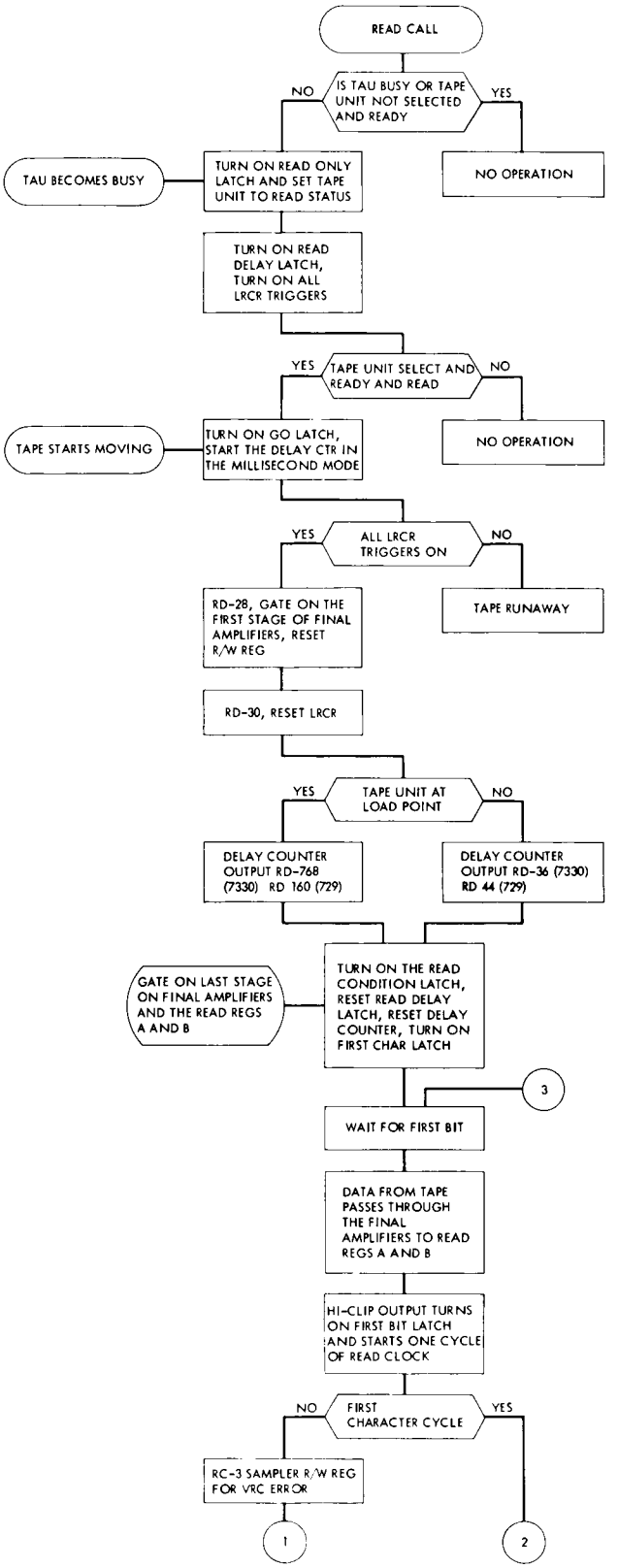


Figure 108. Read Data Flow (Part 1 of 3)

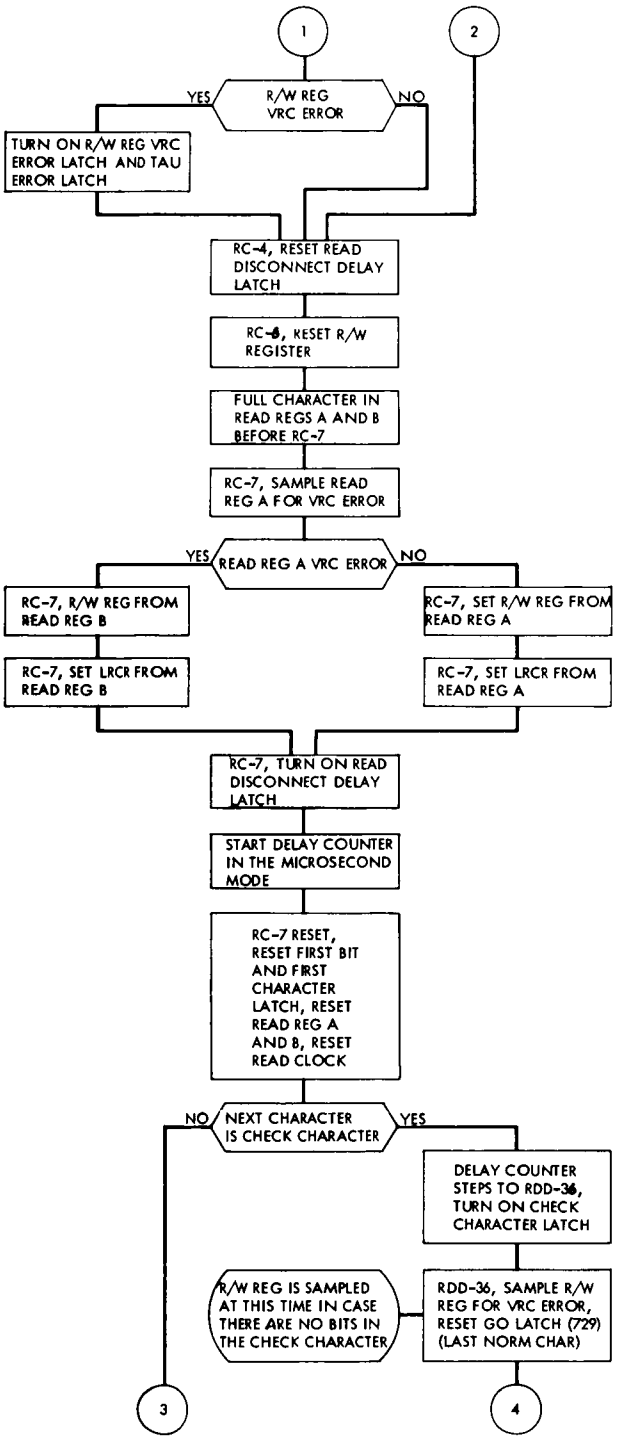


Figure 108. Read Data Flow (Part 2 of 3)

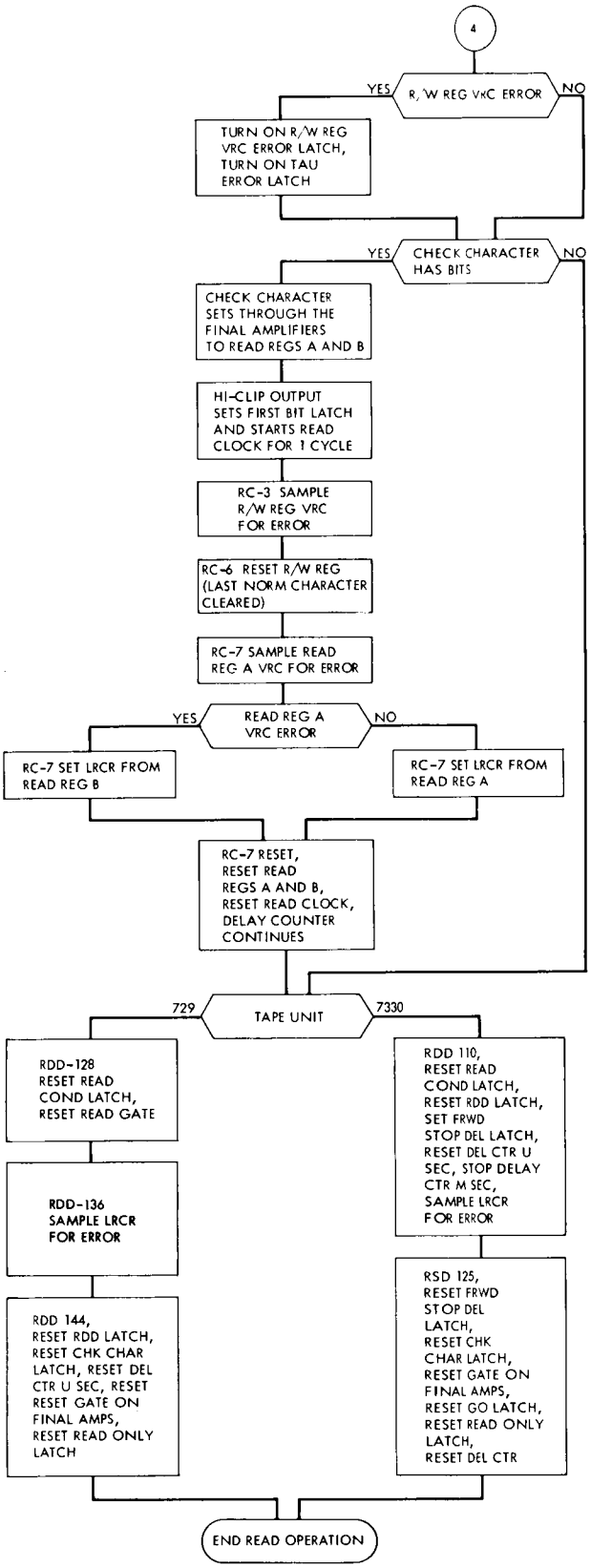


Figure 108. Read Data Flow (Part 3 of 3)

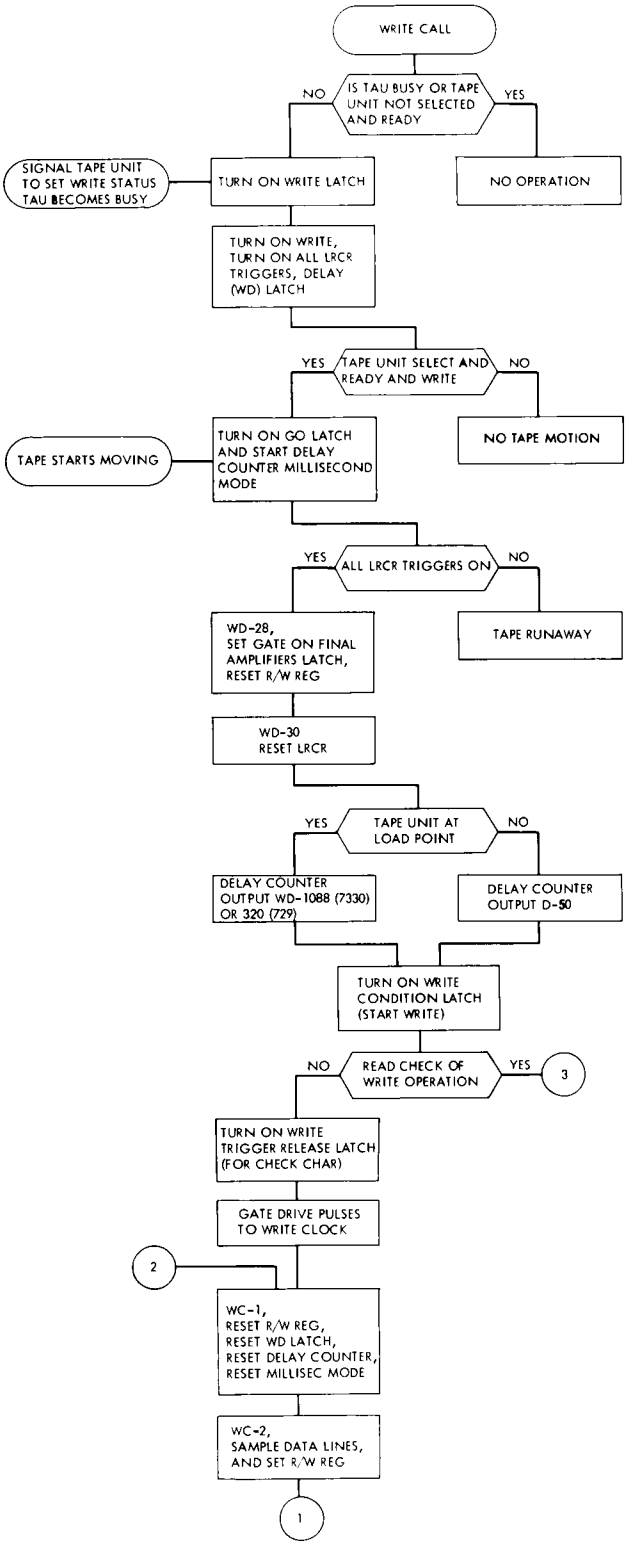


Figure 109. Write Data Flow (Part 1 of 4)

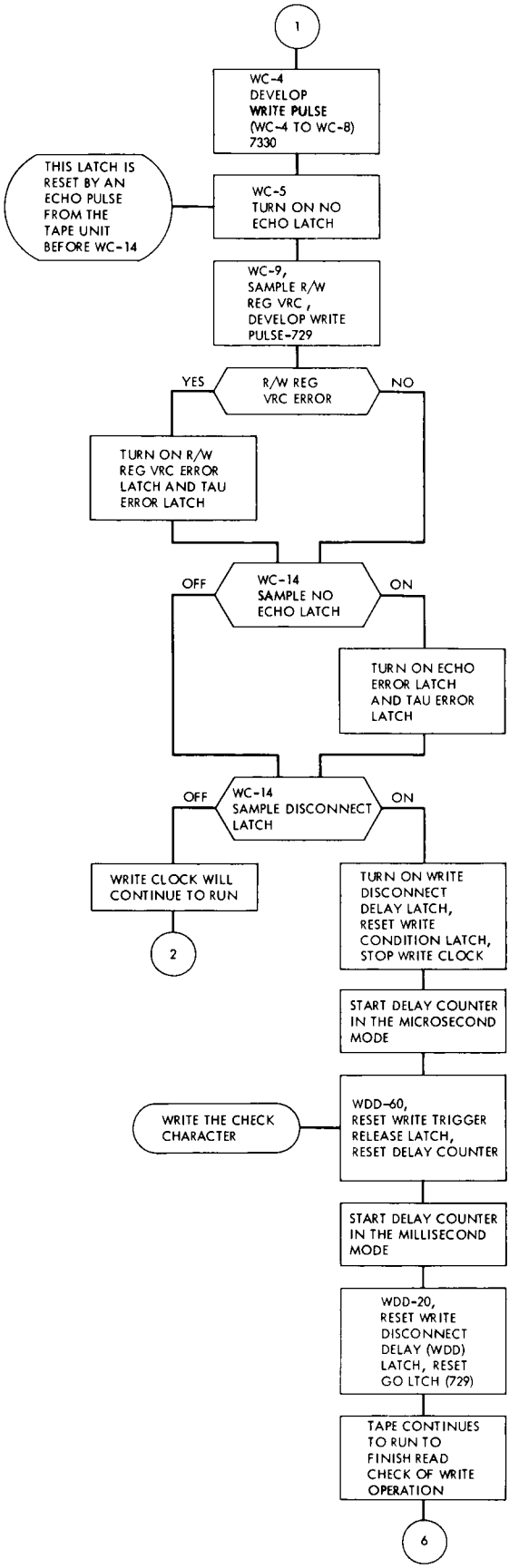


Figure 109. Write Data Flow (Part 2 of 4)

Timing

All the necessary timings and delays required by TAU, are generated by oscillator driven binary counters. The timing circuits in TAU consist of a read clock, a write clock and a delay counter. Because TAU can operate with the 7330, 729 II, IV, V and VI tape drives at different densities, the timings of the various control circuits must vary. By selecting different oscillators the output of the timing circuit can be varied. Figures 111, 112, and 113 list the timing and clock pulses for the various tape drives and their densities.

Read Clock

The read clock (Figure 111) consists of four binary triggers logically gated on and off. These triggers are driven in parallel by the selected clamped oscillator. The trigger outputs are used as read-timing control.

Write Clock

The write clock (Figure 112) consists of four binary triggers logically gated on and off. These triggers are driven in parallel by the selected crystal oscillator. The trigger outputs are used as write timing control.

Delay Counter

The delay counter consists of twelve binary triggers. The first five triggers are driven in parallel by the selected oscillator and logically gated on and off. The remaining seven are driven in series by the output of each preceding trigger. This circuit controls tape motion and data-flow timings. Delay-counter timings are named according to the gate lines and the count that the circuit totals.

The delay counter timings are shown on Figure 113.

Power Supply

The power requirements are:

$-6 \pm 4\%$	0.84 amp
$-12 \pm 4\%$	4.80 amp
$+12 \pm 4\%$	0.82 amp
$+12 \pm 4\%$	0.77 amp

Tape Input/Output Signals

All input signals from the IBM 729 tape units are —N or +P current switching levels terminated with a diffused base to Saturated Drift Transistor Diode Logic (SDTDL) transmission-line terminator except the read bus. All inputs from the IBM 7330 tape units are —N levels terminated with standard SDTRL distributed

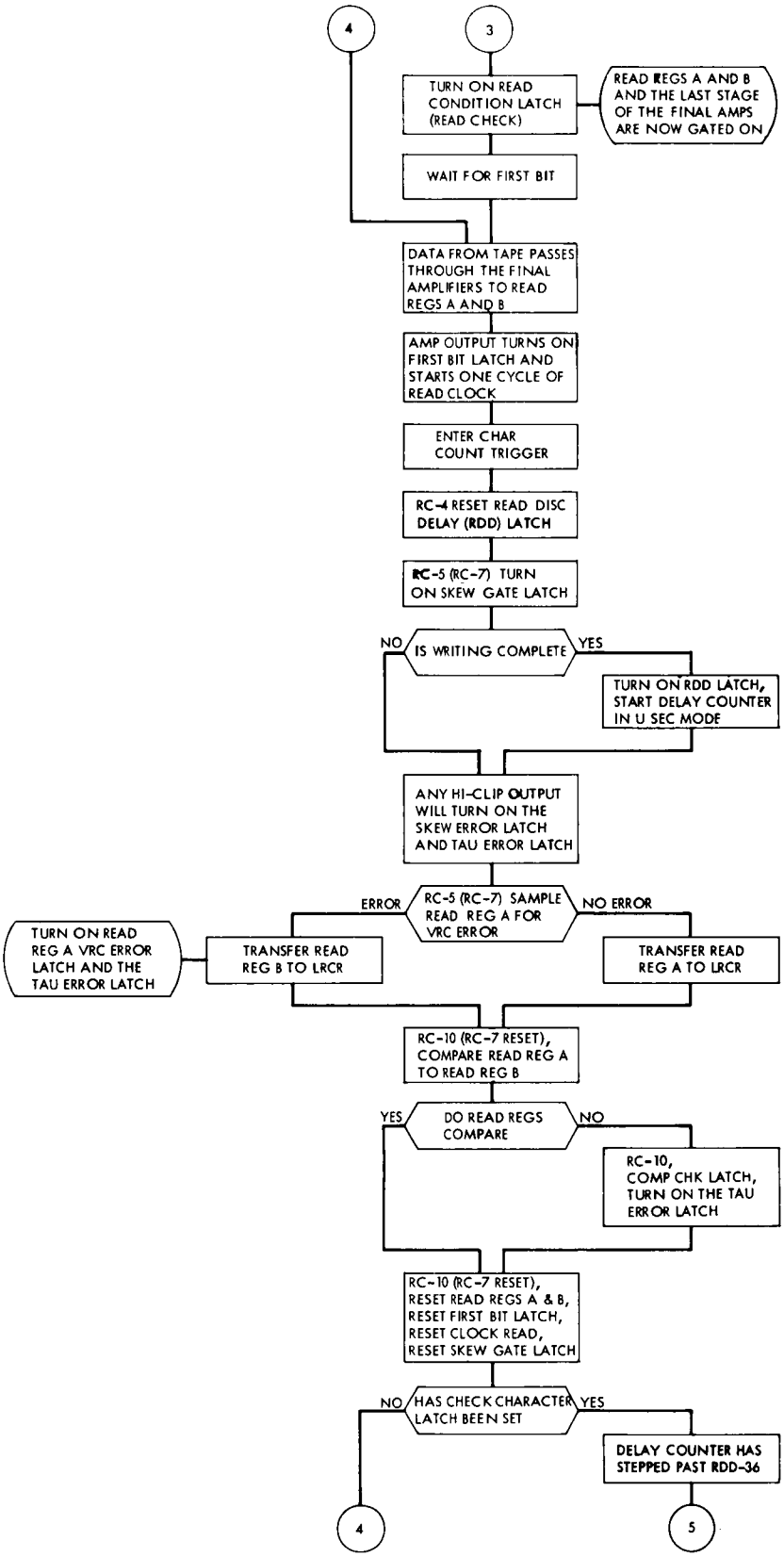


Figure 109. Write Data Flow (Part 3 of 4)

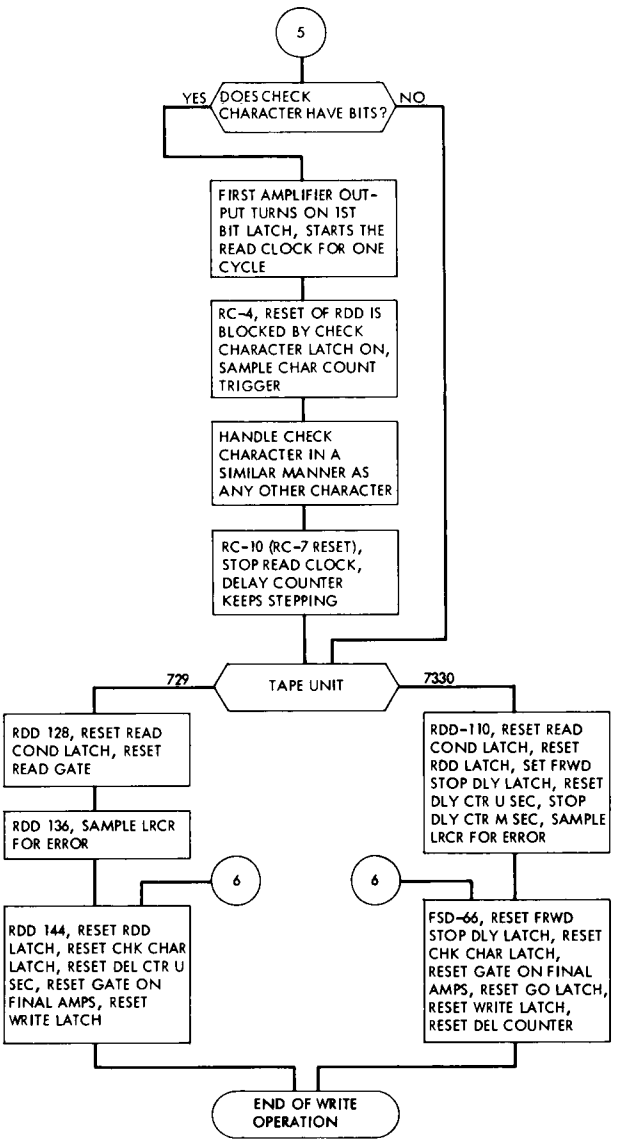


Figure 109. Write Data Flow (Part 4 of 4)

line terminators except the read bus. Each terminator is driven from one of ten tape-unit line drivers spaced along a maximum of 100 feet of external cable.

All output signals to the tape units are —N or +P current switching levels. The N lines are driven by a SDTRL 93 ohm coax-line driver. P-lines are driven by SDTDL power inverters through a 200 ohm series resistance. The circuits have a pyramiding capacity of one to ten tape units with 100 feet of external cable. The TAU contains all output lines except the select lines.

The read busses are voltage levels with a nominal read signal of 8v peak-to-peak. The termination in TAU allows for a maximum capacity of one to ten tape units with 100 feet of external cable.

TAU-9 Final Amplifier

The TAU-9 final amplifier consists of five SMS cards. Each card serves specific functions in a chain of events between the read bus signal and the signal used to set the read register. Refer to Figure 114.

The sense-amplifier circuits are used to sense the NRZI tape signal after it has been amplified by the tape preamplifier located in the tape drive. This circuit operates either the IBM 729 II, 729 IV, or 7330 tape drive. (The IBM 7330 is a low-speed synchronous tape drive.) If the IBM 729 Tape Drive is used, the output signal from the tape drive is applied to the high-frequency input of the sense-amplifier filter and gate card. If the IBM 7330 tape unit is used, its output is applied to the low-frequency input. Two channel outputs per track are provided for the two distinct clipping levels. Status lines are provided to gate the tape signals when the input lines are switched between several preamps. Read/write control lines change the clipping levels on both channels.

A read-control line gates the signal when switching between read and read-while-write conditions. Another control line changes the noise rejection of the circuit depending upon the type of tape drive used.

The over-all circuit for one track is indicated by the block diagram shown in Figure 106. The following is a listing of the various cards used in the final amplifier:

1. Sense Amplifier Filter-and-Gate Card
2. Sense Amplifier Rectifier and Clipper
3. Sense Amplifier Peak Detector, Integrator, and VM Driver
4. Sense Amplifier Select Gate, Read Gate, and Band Pass Control
5. Sense Amplifier Clipping-Level Control

FILTER AND GATE STAGE (FIGURE 115)

The input to the filter-and-gate card accepts high- or low-frequency inputs from either the IBM 729 or 7330 tape unit. The low-frequency input from the IBM 7330 passes through a low-pass filter network whose cutoff frequency is about 30 kc. This filter network reduces the amplitude of any high-frequency noise. The dividers R5 and R7 bias the base of the input transistor (T3) to +6v when the high-frequency input is being used. Likewise R27 and R28 bias T2 at +6v when the low-frequency input is used. Because the reference voltage of the input signal is at ground, the transistor to which an input has not been connected is cut off. The outputs of T2 and T3 pass through another filter network (L33, C10). The cutoff frequency of this filter is 64kc, which is twice the maximum operating frequency of 32 kc. With this type of filter arrangement the high-frequency input passes through the second

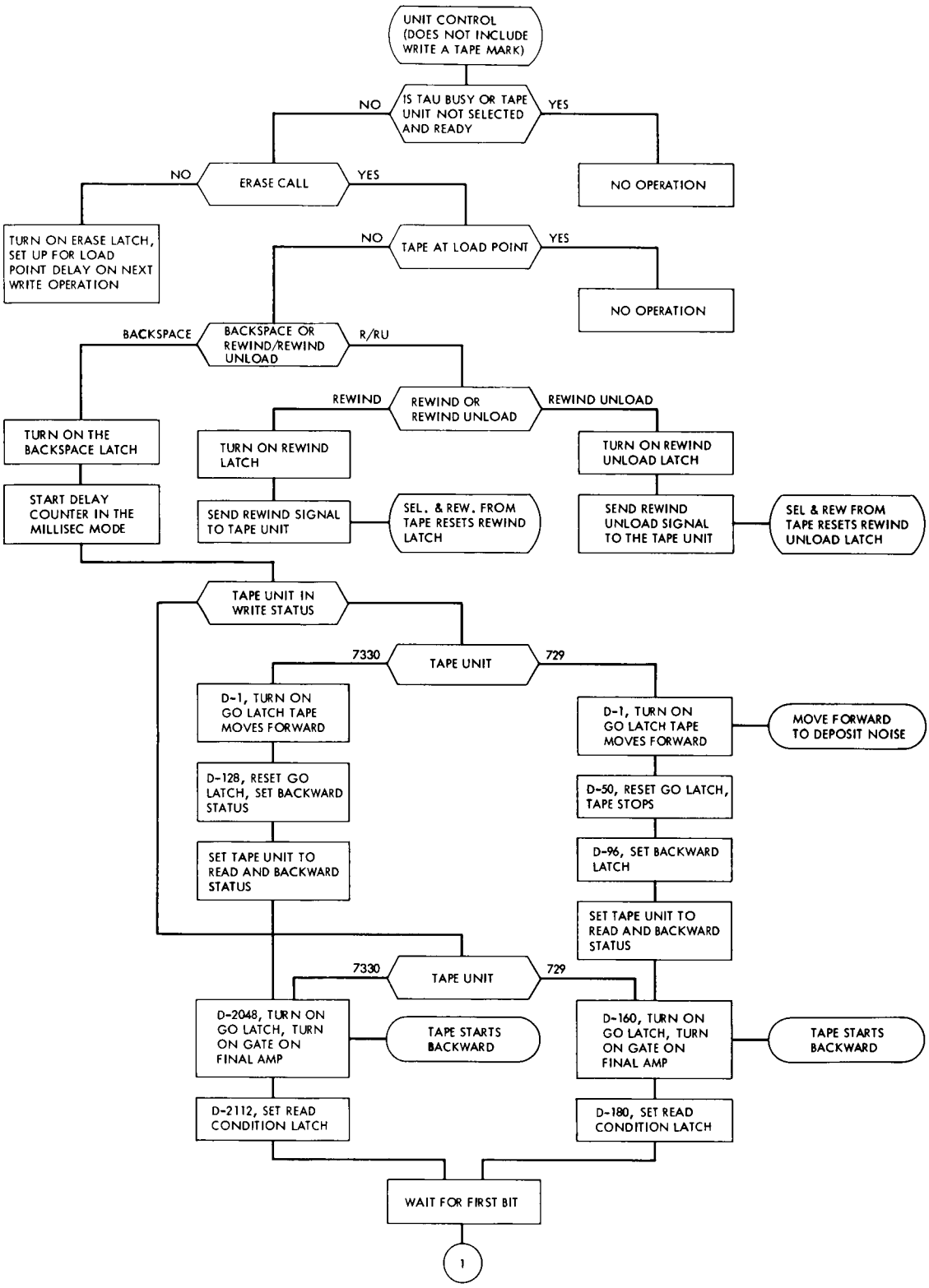


Figure 110. Unit Control Data Flow (Part 1 of 2)

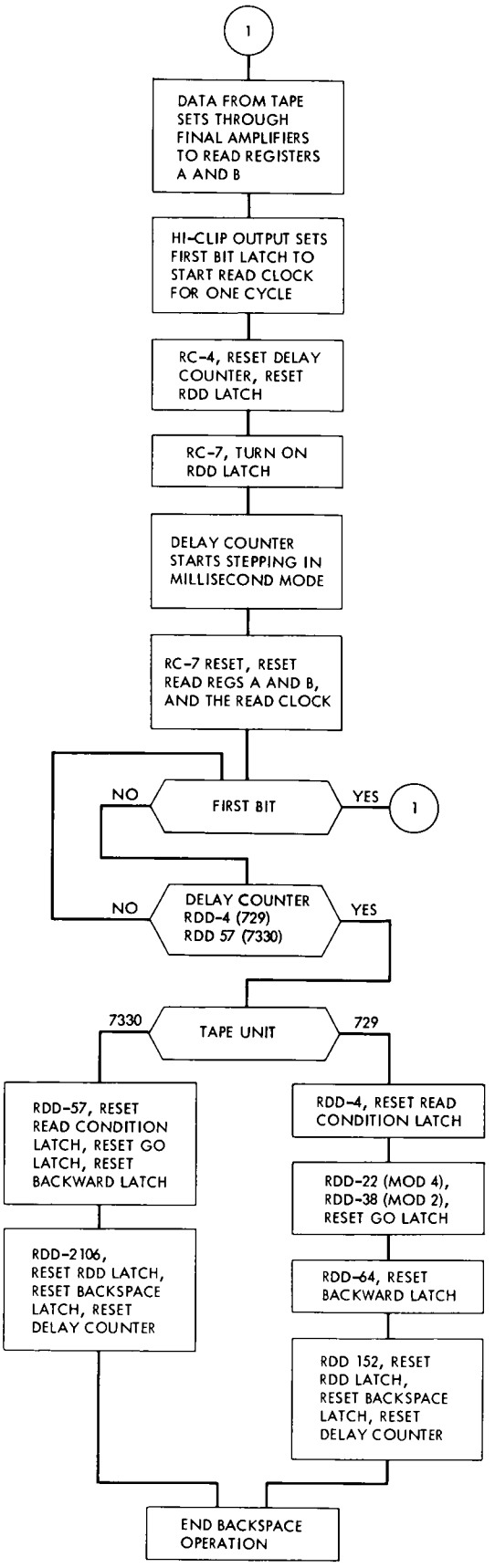


Figure 110. Unit Control Data Flow (Part 2 of 2)

filter, but the low-frequency input passes through both filters.

The transistors T5 and T6 form a gating circuit. When the input at pin F is +6v and the input at pin G is −6v both T5 and T6 are cut off. The signal is then coupled to T7. When the signals are reversed on pins F and G, both T6 and T7 go into saturation and the signal is then shorted to ground so that no output is available. The divider network on the base of T7 is used to bias the signal slightly below ground. This furnishes the reference level for the next stage of the final amplifier (the rectifier and clipper stage). The output-signal amplitude to the next stage is between 7.2v peak-to-peak to 8.0 peak-to-peak depending upon a high- or low-frequency input.

RECTIFIER AND CLIPPER STAGE

The input from the filter-and-gate card is coupled to the rectifier and clipper card through a stepup transformer. This increases the voltage of the input signal so that more accurate clipping and peak sensing can be accomplished. Resistor R6 holds the direct current through the transformer primary at a low value. The secondary of the transformer steps up the signal amplitude to 20v peak-to-peak (out of phase). Transistors T4 and T5 form a rectifier stage so that all signals (ones), whether positive or negative, become positive. Diodes D37 and D40 prevent transistors T4 and T5 from breaking down at the peak of the pulse when the emitter-base junction would be back biased by 20v. R16 is the emitter resistor for T4 and T5.

The emitter followers T6 and T7 are back biased by the resistor drivers so that the signal is clipped. Depending upon whether the circuit is in read or read-while-write mode, different amounts of the signal are clipped. The high and low channels correspond to two different clipping levels or two different thresholds.

This signal is then coupled to the peak detector, pulse shaper, and voltage-driver card. The output-signal amplitude from the rectifier-and-clipper card for a low-acceptance channel varies from 0v to 9v peak-to-peak for read and 0v to 7.5v peak-to-peak for a read-while-write condition. For the high-acceptance channel the output varies 0v to 6.85v peak-to-peak for read condition and 0v to 6.16v peak-to-peak for the read-while-write condition. These positive pulses are approximately the same shape as the input pulse with the bottom of the pulses clipped off.

PEAK DETECTOR AND INTEGRATOR

The rectified and clipped signal from each channel of the rectifier-and-clipper card is coupled to the peak detector, pulse shaper, and voltage-mode driver card. In this circuit the input signal to the bases of T1 and T9 rises but is delayed so that T9 turns on. The diode

Tape Unit	7330	7330	729 II and V	729 II and V	729 V	729 IV and VI	729 IV and VI
Density	200	556	200	556	800	200	556
Drive Osc	115 kc	320 kc	240 kc	667 kc	960 kc	360 kc	1 mc
RC3	26.4 u sec	9.8 u sec	12.8 u sec	4.8 u sec	3.4 u sec	8.6 u sec	3.4 u sec
RC4	35.1 u sec	12.8 u sec	16.9 u sec	6.3 u sec	4.6 u sec	11.4 u sec	4.6 u sec
RC7 (Write)	43.8 u sec	15.9 u sec	21.1 u sec	7.8 u sec	5.6 u sec	14.1 u sec	5.6 u sec
RC6	48.2 u sec	17.5 u sec	23.2 u sec	8.6 u sec	6.0 u sec	15.6 u sec	5.8 u sec
RC7 (Read)	61.2 u sec	22.2 u sec	29.5 u sec	10.8 u sec	7.6 u sec	19.7 u sec	7.6 u sec
RC7 Reset (Read)	66.0 u sec	24.0 u sec	32.0 u sec	11.9 u sec	8.4 u sec	21.5 u sec	8.4 u sec
RC7 Reset (Write)	91.7 u sec	33.1 u sec	44.1 u sec	16.1 u sec	11.0 u sec	29.5 u sec	11.0 u sec

ALL READ CLOCK TIMINGS ±5% WITH RESPECT TO THE FALL OF THE FIRST BIT

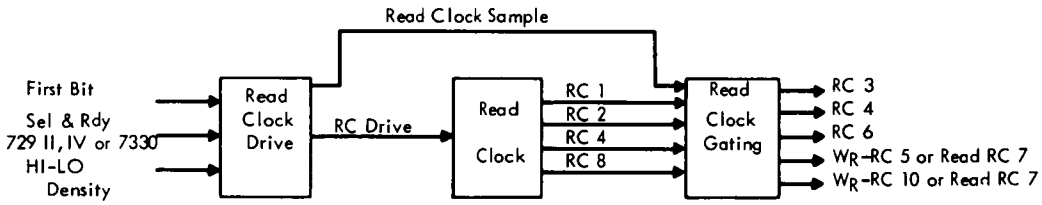


Figure 111. Read Clock Timings

Tape Unit	7330	7330	729 II and V	729 II and V	729 V	729 IV and VI	729 IV and VI
Density	200	556	200	556	800	200	556
Drive Osc	115 kc	320 kc	240 kc	667 kc	960 kc	360 kc	1 mc
WC1	Ref	Ref	Ref	Ref	Ref	Ref	Ref
WC2	8.7 u sec	3.12 u sec	4.16 u sec	1.5 u sec	1.1 u sec	2.78 u sec	1.0 u sec
WC4	26.1 u sec	9.4 u sec	12.5 u sec	4.5 u sec	3.1 u sec	8.34 u sec	3.0 u sec
WC9	65.2 u sec	23.4 u sec	31.5 u sec	11.5 u sec	8.3 u sec	21.1 u sec	7.75 u sec
WC14	113.2 u sec	40.7 u sec	54.1 u sec	19.5 u sec	13.5 u sec	36.1 u sec	13.0 u sec
WC1	139.2 u sec	50.0 u sec	66.6 u sec	24.0 u sec	16.7 u sec	44.5 u sec	16.0 u sec
WC4 to WC8	22.7 u sec	7.8 u sec	—	—	—	—	—

ALL WRITE CLOCK TIMINGS ±1% WITH RESPECT TO THE TURN ON OF WC-1

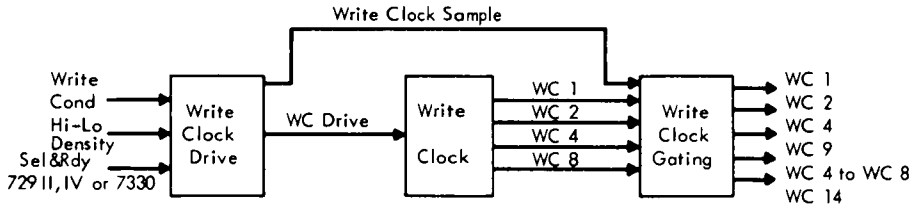


Figure 112. Write Clock Timings

Tape Unit	729 II and V	729 II and V	729 V	729 IV and VI	729 IV and VI	7330	7330
Density	200	556	800	200	556	200	556
Osc	240 kc	667 kc	960 kc	360 kc	1 mc	115 kc	320 kc
RDD 36	150 u sec	54 u sec	37 u sec	100 u sec	36 u sec	313 u sec	112 u sec
RDD 110	—	—	—	—	—	957 u sec	344 u sec
RDD 128	532 u sec	192 u sec	133 u sec	355 u sec	128 u sec	—	—
RDD 136	566 u sec	204 u sec	139 u sec	377 u sec	136 u sec	—	—
RDD 144	600 u sec	216 u sec	150 u sec	400 u sec	144 u sec	—	—
WDD 60	250 u sec	90 u sec	62 u sec	166 u sec	60 u sec	522 u sec	188 u sec

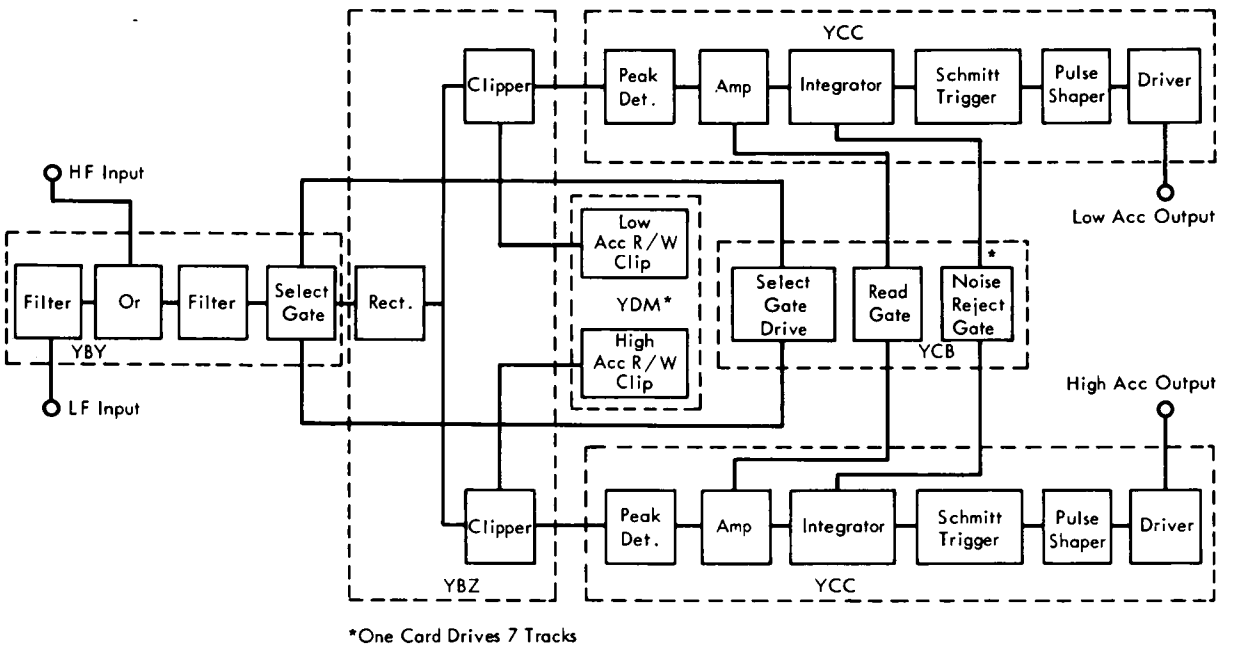
DELAY COUNTER OUTPUTS—MICROSECOND MODE

Tape Unit	729 II and V	729 IV and VI	7330
Osc	6.67 kc	10 kc	10 kc
RDD4	0.6 m sec	0.4 m sec	—
RDD22	—	2.2 m sec	—
RDD38	5.7 m sec	—	—
RDD57	—	—	5.7 m sec
RDD64	9.6 m sec	6.4 m sec	—
RDD152	22.5 m sec	15.2 m sec	—
RDD2106	—	—	210.6 m sec
WDD20	3.0 m sec	2.0 m sec	2.0 m sec
RD28	4.1 m sec	2.8 m sec	2.8 m sec
RD30	4.5 m sec	3.0 m sec	3.0 m sec
RD36	—	—	3.6 m sec
RD44	6.6 m sec	4.4 m sec	—
RD160	24.0 m sec	16.0 m sec	—
RD768	—	—	76.8 m sec
WD28	4.1 m sec	2.8 m sec	2.8 m sec
WD30	4.5 m sec	3.0 m sec	3.0 m sec

Tape Unit	729 II and V	729 IV and VI	7330
Osc	6.67 kc	10 kc	10 kc
WD32	4.8 m sec	3.2 m sec	—
WD49	7.3 m sec	4.9 m sec	4.9 m sec
WD52	7.8 m sec	5.2 m sec	5.2 m sec
WD80	11.9 m sec	8.0 m sec	8.0 m sec
WD320	48.0 m sec	32.0 m sec	—
WD1088	—	—	108.8 m sec
FSD-1	—	—	0.1 m sec
D50	7.5 m sec	5.0 m sec	5.0 m sec
D64	—	—	6.4 m sec
FSD-66	—	—	6.6 m sec
D96	14.4 m sec	9.6 m sec	—
FSD-125	—	—	12.5 m sec
D128	—	—	12.8 m sec
D160	24.0 m sec	16.0 m sec	—
D180	27.0 m sec	18.0 m sec	—
D2048	—	—	204.0 m sec

DELAY COUNTER OUTPUTS—MILLISECOND MODE

Figure 113. Microseconds and Milliseconds Control



*One Card Drives 7 Tracks

Figure 114. TAU Final and Block Diagram

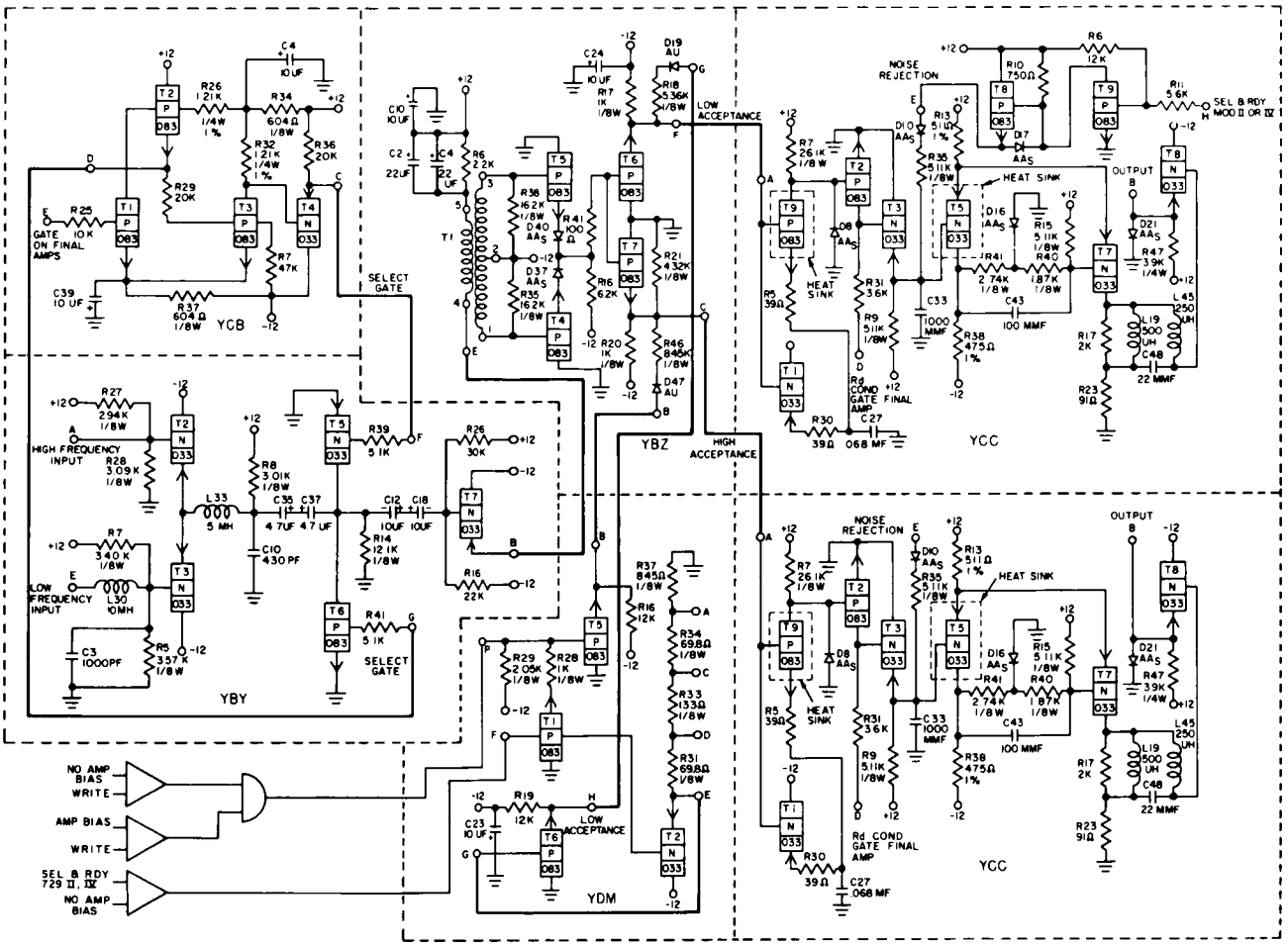


Figure 115. TAU Final Amplifier

at location D8 prevents T9 from saturating. At the peak of the input signal, the emitter voltage is still rising. The input then decreases so that T9 is cut off; thus the rise transition at the collector of T9 corresponds to the peak of the pulse. The transistor at location T1 and the resistor at R30 discharge C27 during the second half of each pulse.

The output of the transistor at T9 is fed to T2 where the signal is amplified to produce faster transition times. When a read-condition gate (+12v) is applied to the collector of T2, the transistor goes into conduction. With the collector at 0 volts, T2 is cut off. The integrator stage (T3) in turn drives the first stage of the trigger located at T5. When a high-frequency input is used, a +12v input is applied to forward bias D10. The combination of D10, R35, and R9 makes up a low-resistance network so C33 charges rapidly to +12v. When the low-frequency input is used, the noise rejection input at D10 is at ground, which reverse-biases the diode. This slows the charge time of C33 to +12v. Thus the frequency response of this circuit is changed by the noise-rejection input voltage.

As the output of T3 swings positive, the transistor at T5 turns off. The diode at location D16 and the resistor at R40 bias the base of T7 to trigger about +3v. A positive swing from T3 causes T5 to turn off. T5 going off causes T7 to turn on. The collector current of T7 flows through L19, which establishes a field. During the fall transition of the input signal to the trigger, T5 turns on and T7 goes off. When T7 turns off, the field around L19, L45, and C48 starts to oscillate. One pulse is produced and the oscillation is damped by R17. In order that no ringing appears on the output the diode at D21 is used to damp the output. The output from T8 is a −S line occurring at the peak of the input pulse ± 3μs.

CLIPPING-LEVEL CONTROL

Because different acceptance levels are required for read and write conditions, it is necessary to have some means of changing the clipping levels upon the appli-

cation of a +S or a −S input. Two separate circuits are used: one for the high-acceptance channel, and one for the low-acceptance channel. These circuits provide clipping levels to all circuits in the seven tracks. The low-acceptance channel has several acceptance levels. These acceptance levels can be changed by jumpers on the back panel.

The high-acceptance channel circuit consists of two NPN emitter followers. With a +S input of 0v on T1 (pin F) and the input to T5 (pin P) open, the output from T5 is around −4v. This corresponds to the read-while-write conditions using a low-speed tape drive. With a +S input of 0v and an input to T5 furnishing enough current to cause the output of T5 to reach ground, this corresponds to the read-while-write condition using the IBM 729 Tape Drive.

With a −S input of −12v, the output is also −12v, which corresponds to the read condition of both low- and high-speed tape drives.

The low-acceptance channel circuit consists of a PNP emitter follower (T2) and an NPN emitter follower (T6). When the input is −S or −12v, the output varies between −8.03v and −12.48v depending upon which jumper is used. When the input is +S or 0v, the input is also 0v.

GATE CONTROL CARD (YCB)

The gate-control card consists of three separate circuits: a select gate driver, a noise-rejection gate, and a read gate. These circuits provide the various gating signals for all seven tracks.

Select Gate Driver. When a +S input is applied to the status gate, T1 goes into saturation and T3 cuts off. Because of the values of the resistors R37, R26, and R34, the output voltage at pin D is about −6v, and the output at pin C is about +6v.

When a −S input is applied to the select gate, T1 is cut off, and T3 goes into saturation. Because of the values of the resistors R37, R32, and R34, the output voltage at pin D is about +6v and the voltage at pin C is −6v. With these voltages, no output is developed to gate the filter-and-gate card.

Noise Rejection and Read Gate. For the noise rejection and read gate, a −S input cuts off T9 so that the output is at +12v. A +S input causes T9 to go into saturation and the output swings to 0v. The diode located at D17 ensures that the output does not go more positive than 0v.

The read gate operates the same as the noise-rejection gate. A −S input produces a +12v output, and a +S input produces a 0v output.

Manual Tape Controls

Operator's Console

One indicator lamp and three switches are added to the operator's console for tape control. These allow the necessary controls for tape loading and for checking out error conditions. The tape-unit-select control activates the CE manual controls. An explanation follows for the indicators and switches.

TAPE INDICATOR

The lamp is lighted when the TAU error trigger is set. It is turned out automatically when the next tape instruction is sent to the TAU.

TAPE-UNIT SELECT SWITCH

This is a rotary switch that is used for the manual selection of tape units. A normal (N), a diagnostic (D), and six select positions are provided. In the normal position, the control is effectively out of the circuit. With the switch set to the D position, the operation is similar to the N position with the following exceptions:

1. A tape-read error is placed in storage exactly as it is read from the tape. No correction is made for validity.
2. In writing, with the error-stop switch on, the write error freezes in the skew A- and skew B-registers.

In any select position, the unit-select and tape-branch circuits cannot be set by program instructions. The manual-control switches on the CE panel are activated in any select position. The program can proceed on nontape operations while CE operations are being performed on tape.

LOAD TAPE

This key is used to read in one record from tape unit 1 without a programmed instruction. The system must be stopped before the key is used. The load instruction is initiated and the system is started in an execute cycle (B-cycle). The record is stored, starting with address 001, and continued until an inter-record gap is sensed on the tape. At the end of the record, the 001 address again is forced at the start of the next instruction.

BACK SPACE

This key is used to back space the selected tape unit by one record. The tape-unit select switch must be set to select a tape unit. This switch serves in the manual evaluation or correction of tape records.

CE Panel

A CE test panel for the tape area is located in 02A1 of the 1401. Lamp indicators and control switches allow forced operation and evaluation of the tape adapter unit (TAU). Either of two CE test panels can be used, depending on the TAU model installed. TAU-2 is used in earlier systems having only the IBM 729 Magnetic Tape Units. TAU-9 that is used in later systems has additional facilities for the IBM 7330 Magnetic Tape Units. The basic concept of the two units is the same. Their operation is detailed in *TAU Instruction Manual,* 223-6847. The two panels and their differences are shown in Figures 116 and 117.

INDICATOR LAMPS

The upper portion of the CE panel indicates the status of the various TAU triggers. A lighted lamp indicates that the associated trigger is in the ON status. The lamps function during normal operation, but many do not light because of very short pulsing. Their major service value comes from being left on when the system stops under error conditions. The lamps are divided into related groups as follows:

Read-Write Control Indicators. Eight lamps show the status of the read and write clock-control triggers.

1. READ indicates the basic read-operation trigger.
2. WRITE indicates the basic write-operation trigger.
3. READ DELAY indicates the starting delays for a read operation.
4. WRITE DELAY indicates the starting delays for a write operation.
5. READ CONDITION indicates the actual read operation.
6. WRITE CONDITION indicates the actual write operation.
7. READ DELAY DISCONNECT indicates the stopping delay for a read operation.
8. WRITE DELAY DISCONNECT indicates the stopping delay for a write operation.

These indicators, plus the clock- or delay-counter indication, give the point in the cycle at which the hang-up occurred.

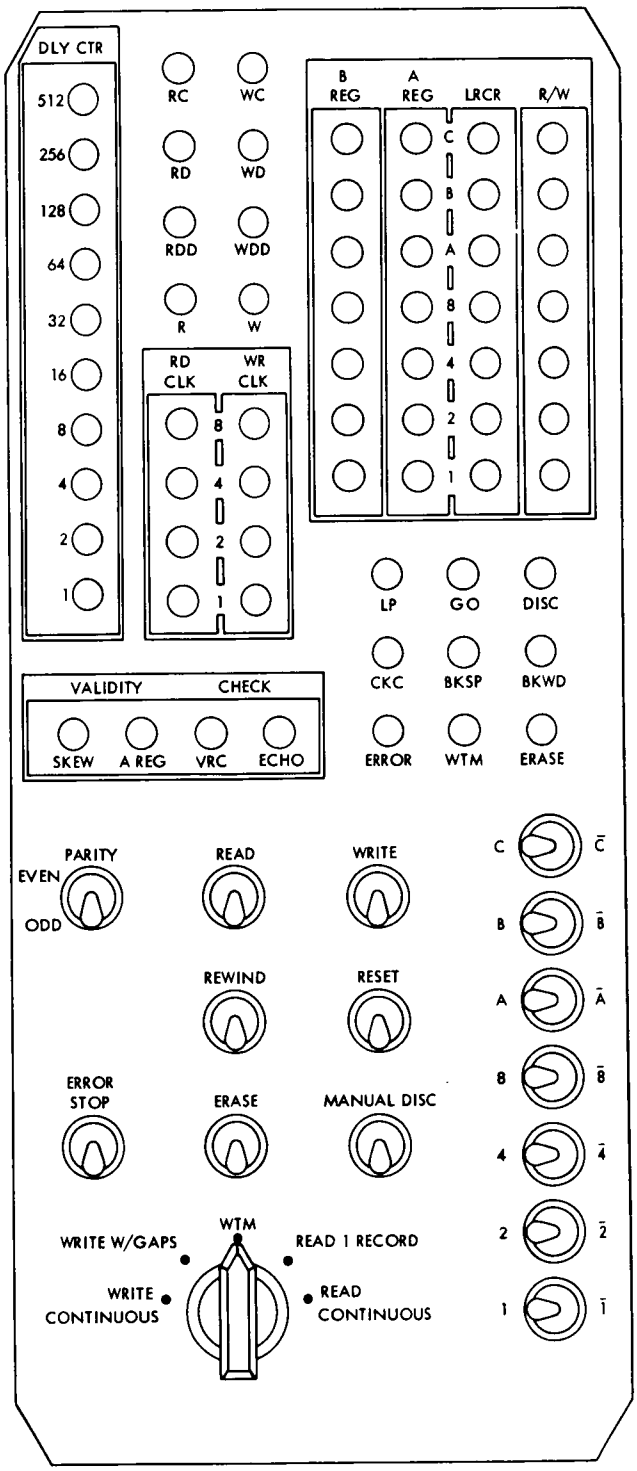


Figure 116. TAU 2 Tape CE Panel

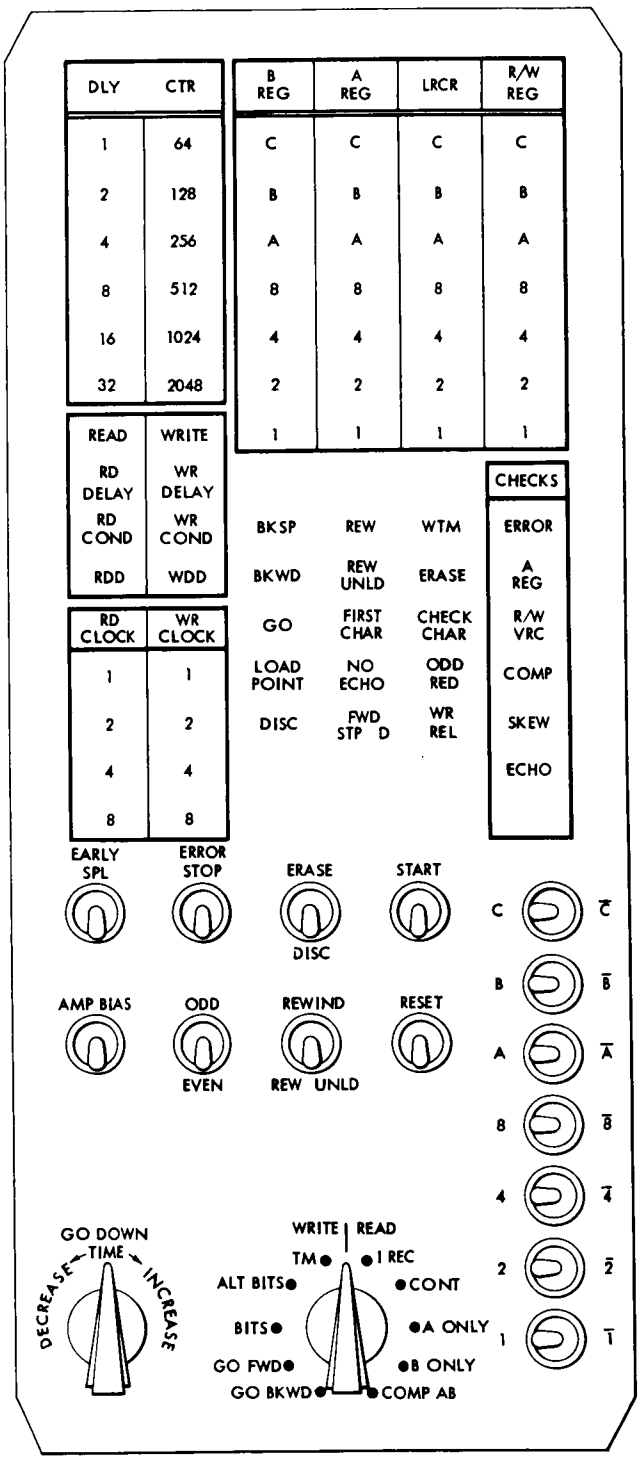


Figure 117. TAU 9 Tape CE Panel

Read-Write Clocking. Four lamps on each clock show the status of the clock in binary notation.

1. READ CLOCK indicates the position of the clock that is used for read operations (also used for READ AFTER WRITE).
2. WRITE CLOCK indicates the position of the clock that is used for write operations.

Delay Counter Indicators. Lamps show each trigger in the counter ring, that progresses in binary notation. TAU-2 panel has ten lamps (1 to 512), and TAU-9 panel has twelve lamps (1 to 2048).

Register Bit Indicators. Seven lamps show the bit status in BCD code for each register.

1. B-REGISTER (SKEW) indicates the bits in the register during the operation. Normally it is blank, while stopped. With the error-stop switch on, the bits freeze at the error condition on STOP.
2. A-REGISTER (SKEW) indicates the bits in the register are the same as B-REGISTER SKEW.
3. LONGITUDINAL REDUNDANCY CHECK REGISTER indicates the bits left in the check register at the end of the operation. The check character normally returns all triggers to the OFF status.
4. READ/WRITE REGISTER indicates the bits in the register. The register normally retains the bit combination of the check character when stopped. With a CE error-stop condition, the register freezes with the bit combination at the time of error.

Function and Status Indicators. In general, this group of lamps reflects operations other than read or write. It also includes several status gates to show the progression of the cycle.

1. BACKSPACE indicates that the backspace trigger-operation trigger is set to back the tape over a record.
2. BACKWARD indicates that the backward-motion trigger is set to reverse the operation of the tape drive.
3. GO indicates that the tape movement trigger is set for either forward or backward motion.
4. LOAD POINT indicates that the selected tape drive has not advanced since it was placed in load status. To insure clean tape, the tape starts to move a short distance before starting the read or write operation.
5. DISCONNECT indicates that the basic operation is completed and that the controls are cycling for a stop.
6. REWIND (TAU-9 only) indicates that the tape is in a rewind operation. The drive is left in load-point status on completion. With the IBM 7330, this is a slow-speed or a backspace rewind.
7. REWIND AND UNLOAD (TAU-9 only) indicates that the tape is in a rewind operation. The drive is left in the unloaded status on completion. For the IBM 7330 this is a high-speed rewind.
8. FIRST CHARACTER (TAU-9 only) indicates that the first read character of either a read or read-after-write operation.
9. NO ECHO (TAU-9 only) indicates that the trigger was reset as the result of the write echo from the tape drive.
10. FORWARD STOP DELAY (TAU-9 only) indicates that the trigger is set for the IBM 7330 stop delay controls that differ from those for the IBM 729.
11. WRITE TAPE MARK indicates that a write-tape-mark operation is in progress.
12. ERASE indicates that an erase call was made. The lamp stays lit until the end of the following write operation.
13. CHECK CHARACTER indicates the check-character read time on a disconnect cycle.
14. ODD REDUNDANCY (TAU-9 only) indicates that the trigger is set for an odd-redundancy call as the result of either the operation control or the CE panel parity switch.
15. WRITE RELEASE (TAU-9 only) indicates that the write trigger-release latch is set ON to allow functioning of the write triggers in the tape drive.
16. ERROR (TAU-2 only) indicates that one of the check circuits detected an error and set the TAU error latch. This lamp is located in the check area of TAU-9.

Check Indicators. These lamps indicate errors that are detected by the validity check circuits in TAU.

1. ERROR (TAU-9 only) indicates that one or more errors were detected to set the TAU error. The lamp is included as a status indicator in TAU-2.
2. A-REGISTER (SKEW) indicates a vertical redundancy check of the register bits.
3. READ/WRITE VERTICAL REDUNDANCY CHECK indicates a redundancy check of the register bits.
4. COMPARE (TAU-9 only) indicates a difference in the bits that are read into the A- and B-registers.
5. SKEW indicates a bit or bits that is, or are, sensed after the read sample gate. Either the bits are angled or skewed on the tape at an angle that is greater than permissible, or the characters are written too closely together (packed).

CONTROL SWITCHES

The lower portion of the CE panel provides switches to force various operation-calls to TAU. These switches are not effective unless the console tape-drive select switch is set to a drive.

Early Sample – TAU-9 only. This is a toggle-action switch that causes the read-sample pulse to occur one clock pulse early. This shortens the time allowed to read before the skew gate is set. It serves to detect feeding problems in the tape drive.

Amplifier Bias – TAU-9 only. This is a toggle-action switch that reverses READ ONLY and READ-AFTER-WRITE clipping levels. The clipping levels for READ-AFTER-WRITE are tighter than for READ ONLY to insure good records. Use of these levels for READ ONLY aids in detecting reading problems.

*Error Stop.*This is a toggle-action switch that causes the A-register, B-register, and read/write register to free with the bit condition at the time of the error. Restart operations stop at the end of the exising call.

Parity Odd-Even. This is a toggle-action switch that sets the redundancy call to the TAU for manual operations.

Erase. This is a momentary-type switch that causes an erase call to the TAU. The erase trigger is set in the usual manner, but no operation is performed until the write call that follows is initiated. This switch on the TAU-9 panel shares a center-off type switch.

Manual Disconnect. This is a momentary-type switch that causes a TAU disconnect or a write operation, and blocks the continuous restart controls for other operations. This switch on the TAU-9 panel shares a center-off type switch.

Rewind. This switch is of the momentary-action type. When operated, it causes the selected tape drive to start a rewind operation. The operation ends with the tape in load point status. With the IBM 7330, it causes a slow-speed rewind. This switch on the TAU-9 panel shares a center-off type switch.

Rewind and Unload – TAU-9 only. This operation shares a center-off, momentary-type switch. When operated, it causes the selected tape drive to start a rewind operation. The operation ends with the tape in the unloaded status. With the IBM 7330, it causes a high-speed rewind.

Read – TAU-2 only. This is a momentary-type switch that is used to start a read only operation. The function control switch must be set to a read operation.

Write – TAU-2 only. This is a momentary-type switch that is used to start a write operation. The function control switch must be set to a write operation.

Start – TAU-9 only. This is a momentary-type switch that is used to start various tape operations. Selection of the operation is determined by the setting of the function switch.

Reset. This is a momentary-type switch that is used to force a TAU reset. The error-check latches, the function latches, the register latches, and the clocking triggers are reset. Its use during an operation causes the immediate stop of the operation.

Bit Switches. Seven toggle-action switches provide selection of the bits to be written during a write operation. The selection and the parity setting must produce a valid combination. The same character is written in every position. TAU-9 has an alternate character control described under *Function Switch.*

Function Switch. A dial switch provides various read and write operating conditions. The switch layout and features differ between TAU-2 and TAU-9. They are described separately to prevent confusion.

1. TAU-2 Function Switch
   a. WRITE CONTINUOUS causes the tape unit to write a continuous record of the preset character until manually stopped, or until the tape reflective strip is sensed.
   b. WRITE WITH GAPS causes the tape unit to write multiple records of the preset character. The length of the individual record is controlled by pulses from the WRITE DELAY CONTROL. MANUAL DISCONNECT or the tape reflective strip can stop the operation only at the end of a record.
   c. WRITE TAPE MARK causes the tape unit to write a tape-mark character and stop when the write switch is operated.
   d. READ 1 RECORD causes the tape unit to read one tape record and stop at the inter-record gap. MANUAL DISCONNECT has no effect if operated.
   e. READ CONTINUOUS causes the tape unit to read record by record with automatic restart between records. The operation stops at the end of a record with MANUAL DISCONNECT or at a tape indicator.

2. TAU-9 Function Switch
   a. WRITE TAPE MARK causes the tape unit to write a tape mark character and stop when the start switch is operated.
   b. WRITE ALTERNATE BITS causes the tape unit to write a record that alternates between the preset character and one with all bits. Because ALL BITS is an obb-bit count, the parity and preset character must be set ODD. This operation can write a continuous record or multiple records with gaps.
   c. WRITE BITS causes the same type of operation as write ALTERNATE BITS. The record is composed en-

tirely of the reset character and can be of either odd or even parity.

d. GO FORWARD causes forward tape movement without either read or write controls. The 1401 controls cause intermittent movement to check the clutch operation. This operation causes tape erasure, when it follows a write operation.
e. GO BACKWARD causes backward tape movement without other tape controls. The 1401 controls cause intermittent movement to check the clutch operation.
f. READ 1 RECORD causes the selected tape drive to read a single record. The stop is automatic at the inter-record gap. The MANUAL DISCONNECT has no effect on the operation.
g. READ CONTINUOUS causes the selected tape drive to read consecutive records until stopped. The TAU controls cause a stop at each inter-record gap, but the 1401 controls initiate another start. The operation terminates at an inter-record gap with either a MANUAL DISCONNECT or a tape indicator.
h. READ A ONLY causes a read continuous operation. The A-register is always transferred to the read/write register and the B-register is not used. This allows observation of the A-register value on invalid characters.
i. READ B ONLY causes a read continuous operation as above. The B-register is always transferred to the read/write register and the A-register is not used. This allows checking the B-register for invalid characters, when the A-register is correct.
j. READ COMPARE AB causes a read continuous operation. The A- and B-registers are compared in the same manner as for read after write. This allows effective checking of the validity of both registers.

Go-Down Time Control — TAU-9 only. This is a variable resistor control that is part of the timing control for the interoperation-delay single-shot. Its normal use is with the go forward and go backward operations.

CE Panel Operation — TAU-2

The tape CE console that is located on gate 02A1 controls all basic tape operations that are off specifications (off spec.). This allows a basic check of TAU and of the tape dirves to be made while the 1401 is running nontape programs.

The controls on the CE console are deactivated when the tape-select switch on the main console is in the N (normal) position.

The following functions can be performed from the CE console.

Write Operations

WRITE CONTINUOUS

This mode provides for the writing of a continuous record. To WRITE CONTINUOUS:

1. Select the desired drive by using the tape select switch on the main console.
2. Set the tape mode switch for WRITE CONTINUOUS.
3. Set the bit switches for the character to be written.
4. Press the write toggle switch.
5. The operation can be stopped by pressing the disconnect switch or the EOF reflective strip.

WRITE WITH GAPS

This mode allows writing one of three lengths of records with a normal inter-record gap.

The number of characters that are written is determined by the location of the slip-on connector at 02A1 A26A, B, or C. The following is a table of the approximate number of characters written for each setting:

		Approximate Number of Characters (IBM 729 II and IV)	
Edge Connectors	*Write Delay*	*High Density*	*Low Density*
A26A	52	13	5
A26B	80	188	68
A26C	768	4,488	1,618

To write with gaps:

1. Select the drive.
2. Set the mode switch for WRITE WITH GAPS.
3. Set the bit switches for character.
4. Press the write toggle switch.
5. This operation is stopped in the same manner as WRITE CONTINUOUS.
6. When the selected drive is at load point and when using WD 52 or WD 80, it is necessary to press WRITE, then RESET, then WRITE to obtain the proper operation. This is necessary because of the long delay before writing from load point.

WRITE TAPE MARK

One tape mark at a time can be written from the CE console. For a write tape mark (WTM) operation:

1. Select the drive.
2. Set the mode switch for WTM.
3. Press the write toggle switch.

ERASE

Pressing the erase toggle switch sets the erase trigger. This causes an erase operation to occur before a write-continuous or write-with-gaps operation.

Read Operations

READ CONTINUOUS

In this mode, a continuous-read operation occurs. To READ CONTINUOUS:

1. Select the drive by using the tape select switch.
2. Set the mode switch for READ CONTINUOUS.
3. Press the read toggle switch.
4. This operation can be terminated by reading a tape mark or pressing the disconnect switch.

READ 1 RECORD

With the setup as in READ CONTINUOUS, only the mode switch is set for READ 1 RECORD. Pressing the read toggle switch causes one record to be read from the tape.

Miscellaneous Functions

REWIND

Pressing the rewind toggle switch causes the drive selected to rewind if that drive is in ready status. After the rewind is complete, the drive returns to a ready status.

DISCONNECT

This switch gives a disk call to the selected tape drive. It is used to stop read and write operations.

REDUNDANCY SWITCH

Use this switch to determine whether even- or odd-redundancy checking is to be used during a read or write operation.

RESET

This switch provides the same function for CE operation as start reset does for normal operation.

STOP ON ERRROR SWITCH

The use of this switch is covered under *Diagnostic Procedures.* This switch must be returned to the OFF position when not in use.

Diagnostic Procedures

STOP ON ERROR

With this switch on during a write operation, the skew register freezes up under an A-register or compare error condition. This allows a visual inspection of the error in the A- and B-skew registers.

DIAGNOSTIC (D) POSITIONS ON THE TAPE SELECT SWITCH

The diagnostic position allows a record that is written on tape to enter storage exactly as it is read with no correction by the C-bit generator. Therefore, with the switch in this position, an error can be analyzed for a possible reconstruction of the record. To operate in this mode:

1. Set the tape select switch on the D position.
2. Run the program in the normal manner. The 1401 stops with an inhibit check when the invalid character is read.
3. An entire record can be read in by turning off the check stop, and the read-in area can be scanned to locate the error.
4. The stop-on-error switch is activated when in the D-mode. Therefore, the skew register freeze-up occurs on a write operation if the switch is on.

Adjusting Start-Stop Times of the IBM 729, by Using the CE Panel Only

To check start-stop times, a continuous record of a given bit is written on tape. The tape is rewound and the write-head driver card for this bit removed. The tape is then written in the WRITE WITH GAPS mode. This prevents erasing the one track and allows scoping it to see the start-stop envelope. The same procedure is used to set backward start-stop times. However, BACKWARD is jumpered ON in the tape drive to allow the tape to be written while running backward.

CAUTION: If the erase head is installed, which was provided by E.C. 248974, the head must be disconnected by pulling edge connector 37G if the start-stop time is to be checked, when using a 1401 system equipped with TAU-2. It is not necessary to disconnect the erase head when checking start-stop times on systems equipped with TAU-9 or when the tape drive tester is used.

TO CHECK FORWARD START-STOP TIMES

1. Write all bits continuously for approximately the full reel of tape.
2. Write a tape mark.
3. Rewind the tape and remove the 8-bit write-head driver in the tape drive (LZ — in D27).
4. Using the WD 52 position, write with gaps using any valid character that excludes the 8-bit.
5. Scope the 8-bit preamplifier output using the go-trigger indicator as a sync point.
6. Adjust start-stop times as stated in the IBM 729 *Reference Manual,* 223-6868.

COUNT FIVE, FORWARD

1. With the 8-bit track written, set for WRITE CONTINUOUS.
2. Use the same scope setup as in *To Check Forward Start-Stop Times.*
3. Pressing the write toggle switch gives one sweep on the scope.
4. To run the test, press reset, count five, press write.
5. Adjust the drive as stated in IBM 729 *Reference Manual.*

BACKWARD START-STOP TIMES

1. Read the tape (that is written for the previous steps) out to the tape marks.
2. Remove the card in location F10 of the tape drive.
3. Reload the drive but in order not to allow the tape to rewind, press LOAD-REWIND and immediately reset. The unit will load and start into a low-speed rewind. Press reset again.
4. Repeat 4, 5, and 6 of *Count Five, Forward.*

CE Panel Operation — TAU-9

The 1401 Tape CE console that is located on gate 02A1 controls all basic tape operations off line.

The controls on the CE console are inoperative when the tape select switch on the main console is in the N (normal) position.

Write Operations

WRITE TAPE MARK

This mode provides for the writing of a tape-mark character, and then stops.

1. Select the desired drive by using the tape-select switch on the main console.
2. Set the function switch to the write tape-mark position.
3. Activate the momentary-start switch.

WRITE ALTERNATE BITS

This mode causes the tape unit to write a record that alternates between the preset character and one with all-bits. Since all-bits is an odd-bit count, the preset character must be set ODD. This operation can write a continuous record or multiple records with gaps.

1. Select the desired tape drive by using the tape-select switch on the main console.
2. Set the function switch to the alternate-bit position.
3. Set the bit switches for the character to be written.
4. Set the redundancy switch to ODD.
5. Select the write-disconnect control. The write operations can be continuous restarts of indefinite-length records. Selection is made by a jumper on terminal block A26, where variable timings control the length of the record. The write-delay timings from TAU terminate at 02A1-A26 as shown.

A26A	Voltage level for the continuous operation.
A26B	Provides WD52 timing.
A26C	Provides WD80 timing.
A26D	Provides WD768 timing.
A26J	Used for an immediate disconnect.

   A disconnect can also be effected by a tape indicator or a manual disconnect.
6. Activate the momentary-start switch.

WRITE BITS

This operation causes the same type of operation as described in the section, *Write Alternate Bits.* The record to be written is composed entirely of the preset characters selected by the bit-selection switches. This operation can write a continuous record or multiple records with gaps.

1. Select the desired drive by using the tape-select switch on the main console.
2. Set the bit-selection switches.
3. Position the function switch to bit position.
4. Set the redundancy switch.
5. Determine the disconnect control. This is explained in *Write Alternate Bits.*
6. Activate the momentary-start switch.

GO FORWARD

The go-forward operation causes a forward tape operation without read or write controls. The first operation is initiated by the start switch to produce a manual go signal to the TAU. With the function switch set for forward operation, this is the only signal required to start movement in the selected tape drive. If the tape drive is in write status, the tape is erased during the forward operation.

The initial operation length is determined by the time the start switch is held. When the switch is released, the fall of the manual GO starts a 10-millisecond single shot. Below this timing, the exact timing of the single shot is variable with the go-down-time-control. The go-down-time-control switch varies the start and stop delays to evaluate the mechanical start-and-stop delays of the tape drive.

1. Select the desired drive by using the tape-select switch on the main console.
2. Make sure that the tape drive is in READ status. Place the tape function switch in the read 1 record position and activate the start switch. This causes the 1 record to be read from tape, and leaves the drive in READ status.
3. Position the function switch to the go-forward position.
4. Set the go-down-time switch to the desired position.
5. Activate the momentary-start switch. The initial operation length is determined by the time the start switch is held. When the switch is released, the fall of the manual GO line starts a ten-ms single shot. The exact timing of the single shot is variable below this timing with the go-down-time control. The use of the single shot output forces a TAU reset that stops the tape movement.

The fall of the ten-ms single shot starts the 6-millisecond single shot for the next tape movement. For the

GO operations the 6-millisecond timing is changed to 60-millisecond, by switching in a ten-microfarad capacitor, (logic 71.71.61). The operation continues until a tape indicator or a manual disconnect is sensed.

GO BACKWARD

The go-backward operation causes a backward tape movement without other tape controls. This operation causes intermittent tape movements to check the clutch operations. The go-time control is a variable resistor control that varies a timing control for the interoperational-delay single-shot as explained under the go-forward operation. During the go-backward operations, the function switch furnishes a backward signal to the TAU to shift the tape-drive clutch. The backspace operation places the tape drive in read status.

1. Select the desired drive by using the tape-select switch on the main console.
2. Position the function switch to the go-backward position.
3. Set the go-down-time switch to the desired position.
4. Activate the momentary-start switch. The initial operation length is determined by the time the start switch is held, as explained in the *Go Forward* section. This operation continues until a tape indicator or manual disconnect is sensed.

Read Operations

READ 1 RECORD

The read 1 record operation causes the selected tape drive to read a single record, and to stop when the inter-record gap is sensed.

1. Select the desired tape drive by using the select switch on the main console.
2. Set the function switch to the read 1 record position.
3. Activate the momentary-start switch.

READ CONTINUOUS

The read continuous operation causes the selected tape drive to read consecutive records until a tape mark or end-of-file is reached. When an inter-record gap is sensed, the TAU controls cause a stop but the 1401 controls initiate another start.

1. Select the desired tape drive by using the select switch on the main console.
2. Set the function switch to continuous position.
3. Activate the momentary-start switch.

READ A-ONLY

The read A-only position causes a continuous read operation. The A-register is always transferred to the read/write register and the contents of the B-register are not used. This allows observation of the A-register contents while troubleshooting.

1. Select the desired tape drive by using the select switch on the main console.
2. Set the function switch to A only.
3. Activate the momentary-start switch.

READ B-ONLY

The read B-position also causes a continuous read operation. The B-register is always transferred to the read/write register and the A-register is not used.

1. Select the tape drive.
2. Set the function switch to the B-only position.
3. Activate the momentary-start switch.

READ-COMPARE AB

This operation causes a continuous read operation. The A- and B-registers are compared in the same manner as for a READ-AFTER-WRITE. This allows checking the validity of both registers.

1. Select the tape drive.
2. Set the function switch to read compare position.
3. Activate the momentary-start switch.

Miscellaneous Functions

REWIND

Activating the rewind toggle switch causes the selected tape drive to rewind, when that drive is in READY status. The operation ends with the tape in load-point status. With the IBM 7330 operation, it causes a slow-speed rewind.

REWIND UNLOAD

This switch shares a center-off, momentary toggle switch with the rewind position. When operated, it causes the selected tape drive to start a rewind operation. The operation ends with the tape in the unloaded status. With the IBM 7330, it causes a high-speed rewind.

RESET

This momentary switch is used to force a TAU reset. The error-check latches, function latches, register latches, and clocking triggers are reset. If used during an operation, an immediate stop is encountered.

ODD-EVEN

This switch sets the redundancy call to the TAU for manual operation.

AMP BIAS

This switch reverses the read only and read-after-write clipping levels. The clipping levels for read-after-write are tighter than for read only to insure good records.

Use of these levels for read only aids in detecting reading problems.

ERROR STOP

With the switch in the error-stop position, the A-register, B-register and R/W register freeze with the bit combinations that are present at the time of the error. This switch is effective on both read and write operations. On a write operation the R/W register freezes on an R/W validity check. The read registers, A and B, freeze with any error condition. An analysis of the register bits determines which type of error was sensed.

On a read operation, the read-register errors do not set the TAU error. An error detected in the R/W register freezes all registers. The character in the read register is the following character from tape.

EARLY SAMPLE

With the switch placed in the EARLY SAMPLE position, the read-sample pulse occurs one clock-pulse earlier. This shortens the time allowed to read before the skew gate is set. This can be used to detect feeding problems in the tape drive.

ERASE

With the switch placed in the ERASE position, an erase-call signal is developed to set the erase trigger. The erase operation is performed on the following write call.

DISCONNECT

This switch causes a TAU disconnect on a write operation, and blocks the continuous-restart controls on other operations.

START

This start switch is a momentary-type switch that develops the various tape calls that are specified by the tape-function switch.

BIT SWITCHES

Seven toggle switches are provided for the selection of bits to be written during a normal write operation or a write alternate-bit operation.

Auxiliary Console

Bit Switches

Eight bit switches are used to alter characters in storage. These switches are used with the alter mode as explained in the mode-switch description. (Figure 118).

The bit switches are located on 37.31.11 and activate the inhibit lines with manual entry.

Enter Key

This switch is used to enter the characters selected by the bit switches into storage, when the mode switch is set to ALTER.

The enter key is located on logic 37.31.11. Refer to *Alter Mode*, Objective 2.

Process Check Stop

This is normally on to cause the machine to stop automatically when a process-check error occurs. If the switch is in the OFF position, the machine does not stop on error conditions, except for input-output checks, and op register and address register checks.

The process-check stop is located on logic 37.31.11 and switches with process check on ILD-16 to activate delta-process reset.

I/O Check Reset Switch

This switch resets error conditions sensed on the I/O units when the I/O check stop switch is off.

The I/O check reset resets the various input/output check latches if the I/O check-stop switch is off. It is located on logic 37.31.11. The transfer point is at —T when the I/O check-stop switch is on, making it ineffective. The bottom section of the switch is for optional features such as print buffer.

Print Select Switch

This three-position rotary switch, when switched to the FULL STORAGE PRINT position, activates storage print out, which controls the print error storage (YU12) and print line complete (YU13) core planes.

The PRINT STORAGE SCAN position of the switch controls the plus 1 modifier and 1400 character control lines. The address register is reset for both of these switch positions.

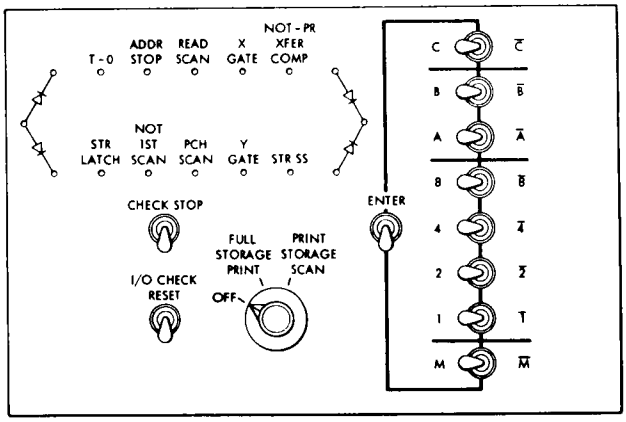


Figure 118. Auxiliary Console

Sync Points (under 26410)

There are ten lines from various triggers, latches, and gates that terminate in jacks at the panel and are used for sync purposes. These are T-0, address stop, read scan, X-gate, not print transfer complete, start latch, not first scan, punch scan, Y-gate, and start and single-shot.

The following sync points are for the 1401 systems with serial numbers *under* 26410.

T-0

Sync point T-0, which is actually clock pulse time 000-030, is at a +U level for the first 30 microseconds of every clock cycle. The leading edge of this pulse is a very useful sync when trouble-shooting other clock pulses, addressing and modifying signals, etc.

Address Stop

This sync point is very useful in producing a sync on any address that is determined by the manual address switch. The leading edge of this sync comes at time 90 of the cycle in which there is a compare between the storage address register and the manual-address switch.

Read Scan

This sync point comes from the output of the read scan trigger. The read-scan trigger is turned on at the beginning of each of the twelve read scans. It is useful in syncing on the leading edge of the first read scan when troubleshooting the reader.

X-Gate, Y-Gate

The X-gate from the OFF side of either the read cycle trigger or the punch clutch trigger. These triggers are binary-coupled, producing an X-gate every other read clutch or punch clutch cycle.

The Y-gate comes from the ON side of these triggers. Thus, by reading or punching continuously, alternate X-gate and Y-gate sync pulses are produced that are important in the read or punch check circuits.

Not Print Transfer Complete (+U)

This is a sync point for use in a print-buffer system to scope the print-transfer controls. This sync goes to a −U level for 132 B-cycles while transferring information from main storage to buffer storage. The line goes to a +U level at the completion of the print transfer.

Start Latch

This sync point is brought directly from the start latch. The leading edge of the pulse goes positive whenever the start key is pressed, sometime during the interval of clock pulse time 030-060.

Not First Scan (+U)

This sync point should be used while scoping the printer control circuits. The line will go to a +U level when printing starts, with the first print scan counter trigger going on. It will stay at +U for the entire 49 print scans until the print scan complete trigger is turned on at the completion of printing.

Punch Scan

The punch-scan sync point is similar to the read-scan sync point because it comes from the punch-scan trigger. It is also used in the same way as the read-scan sync.

Start Single-Shot (+U)

A sync point to use when scoping the carriage control circuits. Start SS is activated by a programmed space or skip, an automatic space after print, or the printer space key.

Diodes

Terminals of four diodes appear on the panel. These are not AND circuits, but can be used to isolate signals to prevent feeding back through the diodes.

Sync Points (above 26410)

The following sync points are for 1401 systems with serial numbers 26410 and above (Figure 119).

+U T-0

Time is 000-030 from clock-pulse generation circuits (logic 31.12.51).

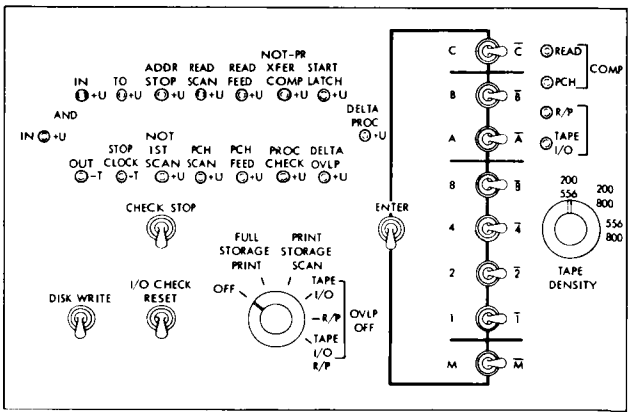


Figure 119. Auxiliary Console above 26410

+U Addr Stop

This signal is comprised of address-stop latch (ON as result of compare between the star and manual address switches) and time 090-105. A third conditioning input is available (logic 32.45.31) for additional control.

+U In, +U In, and −T Out

These 3 hubs comprise the inputs and output of an extendible 2-way AND located on logic 32.41.31.2. The AND inputs are designated as +U so that other signals available at the hubs may either be converted or used to provide conditional sync points. The output of this AND may be used as an input to −T STOP CLOCK.

−T Stop Clock

This hub controls a latch to stop the 1401 clock at the end of a storage cycle (time 000) if the input condition(s) is/are met (logic 31.10.11).

+U Delta Proc

This is the output of cycle-control delta-process latch (logic 31.02.11.2).

+U Proc Check

This is the output of composite condition to light process-check light on console (8 conditions) (logic 31.09.11.2).

+U Start Latch

This is the output of cycle-control start latch (logic 31.01.11.2).

+U Delta Ovlp

This is the output of delta-overlap cycle latch. Functional only with overlap feature (logic 74.31.21).

+U Not-Pr Xfer Comp

This is the output of the OFF side of the print-transfer-complete trigger. Functional only with the print buffer feature (logic 36.31.51).

+U Not 1st Scan

This is the output of print-scan counter activated at all times except during 1st scan (logic 36.35.11.2).

+U Read Scan

This is the output of read-scan trigger gated with B or overlap cycles. Read-scan trigger is turned on for each successive row scan (logic 36.11.11.2).

+U Read Feed

This is the output of read-feed trigger (logic 36.10.-11.2).

+U Pch Scan

This is the output of punch-scan trigger gated with B or overlap cycles. Punch-scan trigger is turned on for each successive row scan (logic 36.22.11.2).

+U Pch Feed

This is the output of punch-feed trigger (logic 36.-24.11.2).

SMS Tool Group

Card Puller

CAUTION: When using this tool, place an IBM card or similar document on both sides of the SMS card to be removed. This prevents damage to components on the SMS card to be removed and on the adjacent SMS cards.

The card puller, 451030, facilitates insertion or removal of SMS cards. It is designed to slide over the card edges. When it is in position, its latch seats in a hole in the card. When it is locked on, it reduces the possibility of dropping the card or of causing other damage while handling. The tool is released by pressing the pivot latch. This tool should be available in all installations containing machines equipped with SMS cards.

Card-Contact Lubricant

When an SMS card is removed from its receptacle, if the card-tab contacts are visibly contaminated with foreign particles (such as dust), or the card tabs have been handled excessively, clean and lubricate the SMS card before reinstalling.

The following procedure insures a low-contact resistance, and reduces wear on the gold-plated contact surfaces. If there is any doubt about the contamination of the contact surfaces, relubricate them. The cleaning and lubricating procedure permits relubrication any number of times without affecting contact reliability:

1. Apply lubricant, 451053, either directly to contacts or indirectly by saturating any clean, lint-free cloth or tissue.
2. Clean and lubricate the contacts by wiping them with a moistened cloth starting from the leading edge and moving toward the component section of the card.
3. Rub the contacts with a clean piece of cloth until there is no visible trace of lubricant. The cloth darkens if the contacts are not properly cleaned.
4. Repeat 1, 2, and 3, if necessary, until the contacts are clean.

The lubricant is supplied in 4-oz. cans, 451053, and should be available in all installations containing machines equipped with SMS cards.

Back-Panel Scope-Probe Tiplet and Ground Wire

The probe tiplet, 451062, and ground wire, 451060, were released for use on machines with SMS cards. They attach to the current-attenuator probe that is supplied with all scopes and they assist in probing SMS back-panel contact pins. The probe has a slotted tip that slides over the contact pins on SMS card back panels. To measure voltage noise or ripple accurately, the attenuator probe must be grounded. To facilitate this on SMS machines, an attenuator ground lead with a slotted tip is available to fit the ground pin on any SMS card socket. One set should be available with each scope that is used in servicing SMS card-equipped machines.

Card-Extender and Cable-Isolation Tool

The card-extender and cable-isolation tool, 451075, makes it possible to check SMS card components, to isolate cable circuits or to switch inputs during machine operation. The socket end of the tool can be rotated on the support to any of six positions. The support can be removed by unscrewing it from the card end of the tool. These features make it possible to check cards in any machine location. The wires from the card end connect to the socket with slip-on connectors which can be removed or interchanged when checking circuitry. Each wire is numbered to coincide with the receptacle pins. This tool should be available to customer engineers who service machines equipped with SMS cards.

Pin-Removal Solder-Iron Tip

The solder-iron tip, 451111, provides a method of replacing damaged pins in all SMS card sockets. The soldering tip fits the soldering-iron element, 454333. WARNING: Damage to the printed-circuit land pattern occurs when it is exposed to excessive heat. Therefore, apply just enough heat to release the pin or to resolder the connection. If damage to the land pattern occurs, repair by using wrapped-wire connections between the pins affected. Instructions:

1. Remove all wrapped-wire connections from the pin to be replaced (soldered or unsoldered).
2. Insert the iron over the pin to its full length.
3. As the solder flows, tap the plunger extension with pliers to release the pin.
4. Remove the pin.
5. Insert a new pin. Pull into place with pliers. Use an iron to resolder the pin to the land pattern.

Replacement portions of this tool can be ordered: plunger, 451113; insulator, 451114; cap (screw) solder tip, 541112.

Hand-Wrapping/Unwrapping Wire-Connector Tools

CAUTION: Using the wrong tool, or the incorrect wire size results in unreliably wrapped-wire connections. The blue-handled tool, 451142, wraps #24 and #26 wire. The amber-handled tool, 451140, wraps #20 and #22 wire. Instructions for using these tools follow.

WRAPPING

1. Strip insulation 1⅜ inch (required to obtain five turns of bare wire plus ¼ to ¾ turn of insulated wire).
2. Fully insert stripped wire into the off-center retaining hole.
3. Bend the wire 90 degrees to the retaining hole. Avoid pulling the insulation out of the tool.
4. Insert the tool over the contact pin until it touches the block or the preceding wrap. The contact pin fits into the center pilot hole of the tool.
5. Hold the loose end of the wire. Turn the tool clockwise or counterclockwise. Apply enough pressure to insure that the turns are against each other. The maximum separation between turns must not exceed .005 inch excluding the first and last turn.

   Note: Factory-wired machines have both left- and right-hand wraps.

UNWRAPPING

CAUTION: Unwrapped wire must not be rewrapped. A new wire must be used as a replacement, or a length of wire spliced to the existing wire. The splice is made by using a butt connector, 216230. Strip the wire ⅛ inch and crimp it with the bare-wire hand-crimping tool, 450898.

Each tool has a right- and left-hand unwrap feature. Apply only enough pressure to loosen the turns. Use the correct tool for unwrapping. The amber handle is for #20 and #22, the blue handle for #24 and #26. These tools should be available to customer engineers who service machines equipped with SMS cards.

Oscilloscope Operating and Servicing Hints

Operating Pointers

The following items are presented to make customer engineers aware of many common pitfalls associated with oscilloscopes. The disconcerting thing about most of these points is that the CE is not likely to know that he has trouble with the scope setup. The end result is that it just takes longer to fix the machine.

The important thing to remember about these points are:

1. They can happen when using either the small or large scopes.

2. They can happen when servicing any machine type.
3. They can happen to all persons using scopes, regardless of the amount of scope experience.

The prime reason seems to be that the CE is concentrating to such an extent on the machine trouble that the necessary consideration is not given to proper scope setup. Because deductions are drawn from the scope, it follows that faulty scope setups lead to faulty, and thus time consuming deductions about the machine problem.

STABILITY SET TOO CLOSE TO FREE RUN

This causes intermittent double traces. The stability control should be rotated counterclockwise noticeably past the point where free-running stops. On scopes that have a preset-stability screwdriver adjustment, check this adjustment to make sure it is not too close to free-run status.

It is not necessary to re-adjust the stability control when changing sync points.

TRIGGER LEVEL

1. The control is set too close to the up level of the sync signal (Figure 120).

   This causes missed sweeps which of course cannot be seen; thus there is no indication they happened. The trouble usually happens when moving from one sync point to a similar pulse that is slightly lower in amplitude and the trigger-level control is not re-adjusted.
2. Control set too close to the down level of the sync signal (Figure 120).

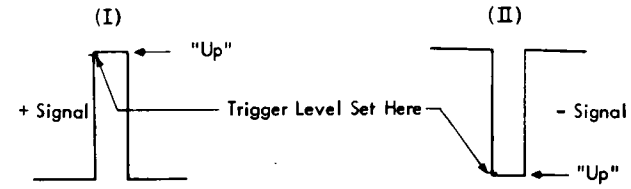
   This causes intermittent double traces because of triggering on small noise spikes or low-level pulses that result from loading changes on the sync-signal line. Again, this is usually caused by changing sync points without re-adjusting the trigger-level control. It is particularly true when moving the sync from a small swing signal to a large swing signal.
3. Control adjusted from the wrong direction on negative sync signals.

   This can cause double traces as shown in the sketch of the negative signal in Figure 122.

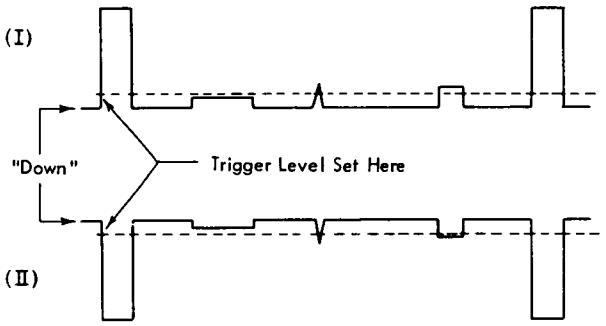
   The proper ways to set the trigger-level control follow:

   Positive Signals (Figure 121). Turn the trigger level fully clockwise. Then turn the trigger level counterclockwise just past the point where stable sweeps are obtained. This causes triggering to occur near the positive end of the signal.

   Negative Signals (Figure 122). Turn the trigger level fully counterclockwise. Then turn the trigger level clockwise just past the point where stable sweeps are obtained. This causes triggering to occur near the negative end of the signal.
4. Always re-adjust the trigger level when changing sync points.



Trigger Level (Too Close to Up Level)



Trigger Level (Too Close to Down Level)

Figure 120. Trigger Level

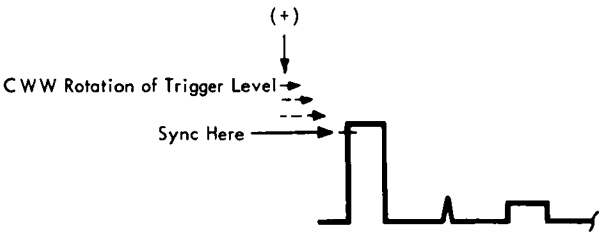


Figure 121. Trigger Level Positive

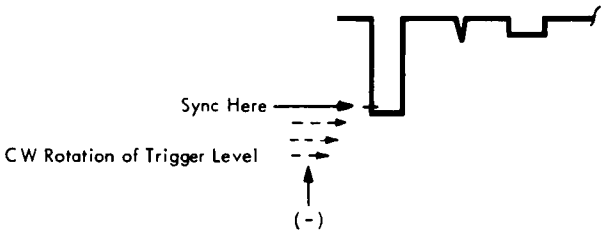


Figure 122. Trigger Level Negative

TRIGGER MODE

1. AUTOMATIC should not be used because triggering can occur on down-level variations as small as 0.05v. Double sweeps can result from noise or low down-level pulses.
2. DC is preferred to AC because the shift of some sync signals changes with varying loads and can cause missed sweeps in the ac mode. Also, in the ac mode, the trigger level does not give any indication of the machine voltage level at which triggering is occurring. Use dc mode when possible.

TRIGGER SLOPE AND SOURCE

1. Set the desired slope.
   a. It is very easy to change syncs from a positive to a negative signal, or vice versa, and neglect to change the trigger slope. Result: the scope triggers at the end of the sync pulse or gate instead of at the beginning.
   b. At times it is desirable to sync when a signal goes OFF but, again, consciously set the desired slope.
2. Use external sync almost exclusively. Internal sync gives no time reference to any other machine pulse. Good troubleshooting procedure demands that the time relationship of the observed pulse to the machine operation be known at all times. This is even more important in solid-state circuits than in tube circuits. Degraded transistors primarily exhibit slow switching times, and tubes exhibit poor output levels.

HORIZONTAL POSITION

Occasionally, after the scope is calibrated to machine time pulses, the horizontal position control is moved slightly for some reason. Scoping then continues without the CE having returned the control to the prior position. This causes erroneous observations because *time* no longer appears where it is expected to be.

X5 MAGNIFIER

Exercise care with the use of the X5 magnifier. It is quite easy to have the portion of the signal that actually contains the error information positioned off the screen. There are two common reasons for using the X5 magnifier:

1. to expand the signal when the available sync is too far from the signal on a X1 sweep for detailed observation.
2. to obtain an extremely fast sweep rate.

SWEEP TIME

The signal being displayed should be expanded as much as is practical in all cases. This aids a good analysis of the signal because it can be observed in detail.

VERTICAL VOLTS

When observing signals having widely different amplitudes, change the vertical gain on the scope. If this is not done, the small signals cannot adequately be observed for correct amplitudes.

Make sure the green-light filter is on the scope. This improves the effective intensity of a weak trace about ten times. The filters can be obtained as follows:

For 535/545 Scopes:	Order 460528, light filter.
For 310/310A Scopes:	Obtain the light filter from the nearest Tektronix* field-service office.

Using the viewing hood, especially on the 310 scope. This hood improves intensity about ten times.

Always check the attenuator probes for proper compensation before using them. An under-compensated probe causes a good-level short-duration pulse to appear weak. More important, an over-compensated probe causes a weak short-duration pulse to appear good.

Servicing Hints

OVER-ALL CHECKING

Indiscriminate probing with a scope while a program is running is very tempting, especially on a solid failure. It is not recommended because many signal lines are fed by more than one logic block and missing pulses cannot be discovered when the machine-time references are not known.

The machine time of pulses must be known at all times before valid deductions can be made.

NOISE CHECKS

1. Proper scope setup.
   a. Plug the scope into the convenience outlet in the machine unit where noise checks are to be made.
   b. The short ground lead must be attached to the scope-probe attenuator and then grounded as close as possible to the line being observed. This must be the circuit ground, not the machine-frame ground. If this setup is not followed, you are liable to be chasing *noise* that really does not exist in the immediate circuit being observed.
2. Types of noise (includes switching spikes). Noise falls into three categories defined by their individual time relationships to the machine clock. Any observed noise *must* be categorized before the proper action can be decided upon.
   a. Noise that is fixed to the machine clock but that appears at a time when it is switched out in succeeding logic so no malfunctions can result.

*Tektronix, Inc.

This noise is actually a logic switching spike that was not removed because it cannot cause trouble due to its time relationship to the clock. Do not try to remove this kind of noise because it probably cannot be accomplished without a circuit change. A good tip that will help if you are ever in the area again is to mark the size, shape, and time of the spike in the logics where it occurs.

b. Noise that is fixed in time to the machine clock and is at a time where it is causing trouble.

This *noise* is actually a logic switching spike that is resulting from a circuit that is operating improperly (usually too slow but occasionally a very fast transistor circuit causes trouble).

This problem has the pitfall that replacing any one of several pluggable components in the immediate circuit may make the machine work, *for a while*. Calibrate the scope to the machine-time base and closely analyze the delays through the circuits causing the spike so that the *correct component* is replaced.

c. Noise that is not fixed in time to the machine clock.

This is true noise. It comes from areas such as switches, clutches, and relays. The best way to locate its source is to determine the general time of the noise within the program loop. If possible, relate this to some mechanical operation within the system.

Do not be mislead by the fact that the noise can be quite intermittent. Because it is usually associated with a mechanical operation its time can vary widely when compared to the clock and still occur within the same general area of the entire program loop. This can be traced to switches, clutches, and relays, related in time to a specific input/output machine cycle associated with the program loop.

If the noise is not consistently within the same general area of the program loop, it can be caused by components in circuits such as ribbon-reversing or tape-drive take-up mechanisms (operations that do not take in synchronism with the program loop).

3. Relating *noise* time to dynamic-timer time. Noise is usually of such a short duration that it does not fire the neon on a dynamic timer. After a 310 or 535/545 scope has been used to determine that noise exists on a line, its relationship to a dynamic timer can be determined as follows:

a. Sync EXT on a known circuit-breaker time.
b. Calibrate the time base to machine-cycle time.
c. Observe the suspected line for noise and determine its cycle time from the graticule divisions.
d. If necessary, a more appropriate sync point can be chosen after the noise is roughly located. The sweep speed can then be increased to observe the noise in more detail.

For use with a 535/545 scope*

a. Sync INT and use a sweep speed of 1 ms/cm.
b. Connect the + GATE MAIN SWEEP scope hub to the CONTACT hub on the dynamic timer.
c. Connect the dynamic timer COMMON hub to GROUND if it is not already connected internally.
d. Probe the suspected line and observe the timer dial. The noise occurs at the point where the timer light comes on. The light remains on for the duration of the sweep on the scope.

**Note:* This is applicable only to voltage lines because normal pulses on signal lines also trigger the scope sweep. The 310 method must be used on signal lines.

THE SCOPE AS AN INDICATOR

When checking for a signal that occurs infrequently, it is sometimes advantageous just to know what has happened. This can be done by using a very slow sweep speed and using INT sync. CAUTION: If the intensity is too high, the scope screen may be damaged. The signal initiates the sweep but because the sweep is very slow, it holds the evidence for several seconds.

An additional feature on the 535/545 scopes is *single sweep*. This permits retention, for any period of time, of the fact that the signal occurred. It is particularly effective in checking for noise on a voltage line. Set up the scope as described to determine if the line had noise spikes of sufficient level to trigger the scope.

There are two methods for obtaining a SINGLE-SWEEP; one for 535/545 scopes, the other for 535A/545A scopes.

1. 535/545 scopes (no SINGLE-SWEEP position on the display switch).

a. Start the scope in a completely normal setup main-sweep NORMAL and main-sweep SYNC controls set for proper triggering on the external signal).
b. Turn DELAYING SWEEP STABILITY fully counterclockwise.
c. Set the display switch to MAIN SWEEP DELAYED.
d. Press MAIN SWEEP RESET. (Note that the main sweep ready light is on.)
e. Only the first sync pulse received at the main sweep TRIGGER INPUT hub initiates a sweep and turns the ready light off.
f. Repeat *step d* to check for a signal on the line again.

2. 535A/545A scopes (SINGLE-SWEEP position on the display switch).
   a. Start with the scope in a completely normal setup (display switch at A and TIME BASE A sync controls set for proper triggering on the external signal).
   b. Set the display switch to A SINGLE SWEEP.
   c. Follow steps *1 d* through *1 f* the same as with a 535 or 545 scope.

SWEEP-DELAY OPERATION (ALL 535/545 MODELS)

The sweep-delay feature of the 535/545 scopes is an extremely valuable service aid that is not fully utilized by many CE's who have these scopes available. The usual procedure for the set up is confusing, thus time consuming, and it does not give any indication of where to start with the delay controls.

The sweep-delay feature should be used on most service calls that require a scope because it practically eliminates the time-consuming problem of obtaining a good sync close to the signal being observed. It is only necessary to sync on the op code and initiate the appropriate amount of delay. 100 ms is the maximum delay on the no-suffix scopes.

The procedure outlined here is much quicker to use and easier to remember because it eliminates several unnecessary intermediate steps. At the same time, it gives built-in assurance that it is set up properly.

1. Setup for delayed sweep:
   a. Assume the scope is set up normally and the desired signal cannot be observed in detail.
   b. Set the main-sweep stability clockwise until free run occurs.
   c. Move the sync lead to the DELAY SWEEP TRIGGER hub.
   d. Set the delay trigger SLOPE toggle switch to the proper polarity.
   e. Set the delay sweep TIME/CM switch at a time equal to the main sweep TIME/CM including the main-sweep multiplier if the scope has one. (It may be necessary to go one position slower than the main sweep if the variable main-sweep control is being used and the signal to be expanded is near the right end of the trace.)
   f. Set the delay-sweep multiplier at about 0-05 (the horizontal sweep may not function at exactly 0-00).
   g. Set the display switch to MAIN SWEEP DELAYED (A delayed by B on some scopes).
   h. Adjust the delay sweep stability-and-triggering-level controls in the usual manner to obtain a stable sweep. This results in the same display as that being observed before changing to delayed sweep because the delay multiplier is causing very little delay. (The desired signal may have moved to the left somewhat if the delay TIME/CM was set slower than the main sweep TIME/CM in *step e.*)
   i. Turn the delay-time multiplier until the desired signal approaches the left side of the screen. The main sweep can then be changed to expand it. This step can be repeated to expand the signal further.
2. Triggered delayed sweep. The preceding procedure works well when the total delay is less than about 10 milliseconds. The expanded signal may jitter and make diagnosis uncertain. (If much jitter is present for delays less than 10 milliseconds, the scope delay circuits or the machine oscillator can be suspected of malfunctioning.)

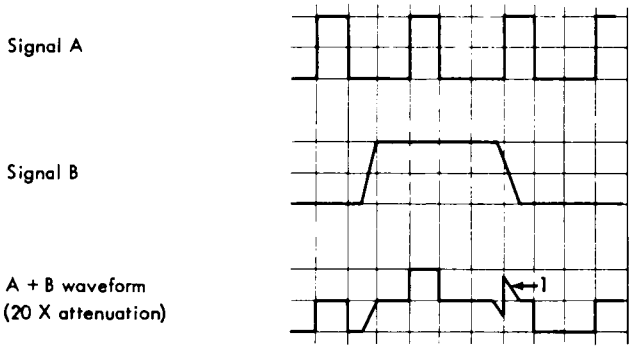
   Signal jitter can be removed by causing the main sweep to start on a machine-time pulse or gate after the delay-sweep generator has timed out. This is accomplished as follows:
   a. Turn the main-sweep stability counterclockwise until no more traces appear.
   b. Attach the desired clock pulse or gate to the main sweep TRIGGER hub.
   c. Adjust the main-sweep trigger-level-and-slope controls properly. The sweep now starts with the first machine pulse received after the sweep delay has occurred.

      Note: Because the sweep can only start with a machine clock pulse, the signals jump as the delay multiplier is rotated. This must be considered when expanding the signal as described in *Step 1-i.*

The delayed-sweep feature can be used to its greatest advantage by having the scope set up on delayed sweep at all times that EXT sync is being used. Whenever delay is required, it is only necessary to advance the DELAY TIME/CM and MULTIPLIER controls to obtain the desired delay. One point should be kept in mind if this method is used: when *no delay* is desired, keep the DELAY TIME/CM set at two μs and the DELAY MULTIPLIER set close to 0-00 so that the minimum inserted delay is less than 0.5 μs. This minimum delay will be several microseconds with the DELAY TIME/CM set to the slower ranges even though the MULTIPLIER is very close to 0-00.

Duo-Input Switch

The duo-input switch (451129) allows viewing the timing relationship of two signals at one time on the Tektronix Oscilloscope Type 310. Any two 10 × attenuator probes that are approximately the same length can be used. The switch has three positions, the functions of which allow:



NOTE: Switching spike at (1)

Figure 123. Duo-Input Switch

1. Viewing only signal A with 10 × attenuation.
2. Viewing only signal B with 10× attenuation.
3. Viewing both signals at the same time with 20 × attenuation. The signals are algebraically added so that precise timing relationships can be observed (Figure 123).

There are two adjustment procedures for the scope probes and the switch box. *Adjustment 1* should be used at all times other than the specific case given for *Adjustment 2*. Use the scope calibrator output as the adjustment signal source.

ADJUSTMENT 1

This procedure, for normal troubleshooting, provides true waveforms in either the A or B position, and a slightly distorted waveform in the A + B position. However, this distortion is quite small, and it does not affect the comparison of the two signals for their timing relationship.

1. Adjust probe A (switch in position A) for the best waveform.
2. Adjust probe B (switch in position B) for the best waveform.
3. Set the switch to A + B. Place both probes on the calibrator output. Adjust the switch trimmer (in small hole near the switch knob) for the best waveform.

ADJUSTMENT 2

This procedure is to be used only when the exact sums of two waveforms are in the A + B position, but both the A and the B positions are likely to be distorted (one overcompensated and one undercompensated).

1. Perform 1, 2, and 3 in *Adjustment 1.*
2. With the switch at A + B position:
   a. Observe the calibrated signal with probe A, and re-adjust probe A for the best waveform.
   b. Observe the calibrated signal with probe B, and re-adjust probe B for the best waveform.

   Note: These probes will require re-adjustment when they are again used without the duo-input switch.

   CAUTION: The switch cannot be used with two × 1 probes because the signals would be sorted together. It can be used to advantage with one × 1 and one × 10 probe where convenience is desired.

DUAL-TRACE ADAPTER — TEKTRONIX OSCILLOSCOPE TYPE 310

Figure 124 shows another version of a dual-trace adapter for a Tektronix Oscilloscope Type 310. This model uses a chopper that has good switching characteristics for this application.

Inputs are direct and when used in tape-skew adjustment, provide a good display on the scope. In most applications of this kind, the loading effect of the 1 megacycle scope input, as against the 10 megacycle input using the probe, can be tolerated. Amplitude adjustments are made by using the probe.

To distinguish the reference bit from the other bits, it is possible to increase or decrease the reference bit amplitude temporarily from the nominal 8v. If both are the same amplitude, the traces will superimpose when in exact phase.

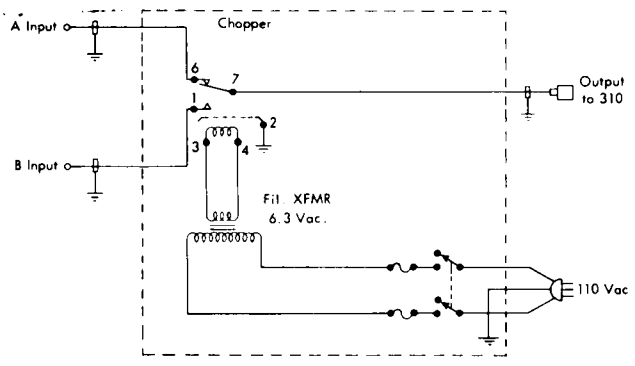


Figure 124. Duo-Trace Adapter

The following photographs are of unusual waveforms that are encountered when scoping 1401 circuits.

The purpose of these photographs is to make the customer engineer aware of these waveforms to minimize service time and to determine whether an unusual waveform is acceptable. Many of the photographs were taken of incorrect waveforms or waveforms that were seen when a trouble is present for a particular circuit.

All scope settings and triggering points are listed where it was deemed helpful. Tolerances for waveforms are listed.

1401 Central Process Unit

The scope pictures are of the star-reset pulse. This pulse is used to reset the instruction address register, A-address register, and the B-address register.

Figure 125 part A shows the waveform at the input pin of the delay card (01B3 A21 A), on 31.10.11.2, while Figure 125 part B shows the output waveform at (01 B3 A21 F).

Scope Setup

Triggering: Ext. plus, on-time 000-030 pulse available at console hub.

1 μs/div.

5 volts/div.

Note: Waveform is same on both Stage II and I.F.C. machines.

Figure 125 part C shows a typical +MAD card output. This card has slow turn-on time indicated by the slow slope on the negative going portion of the wave.

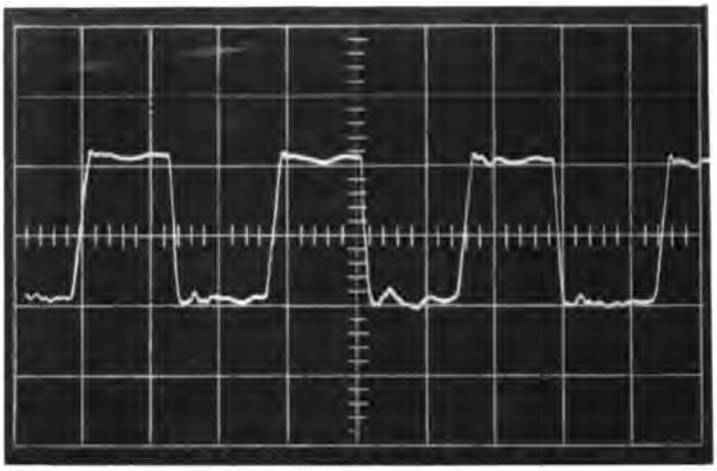
This waveform was scoped at 01B3 B21H on 31.12.21.2. It is the signal labeled — *T Time 090-000.*

Scope Setup

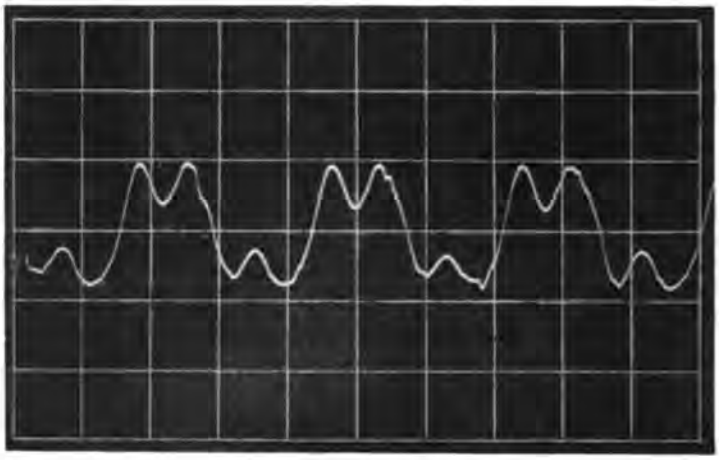
Triggering: Ext. 060-090 time pulse.

1 μs/div.

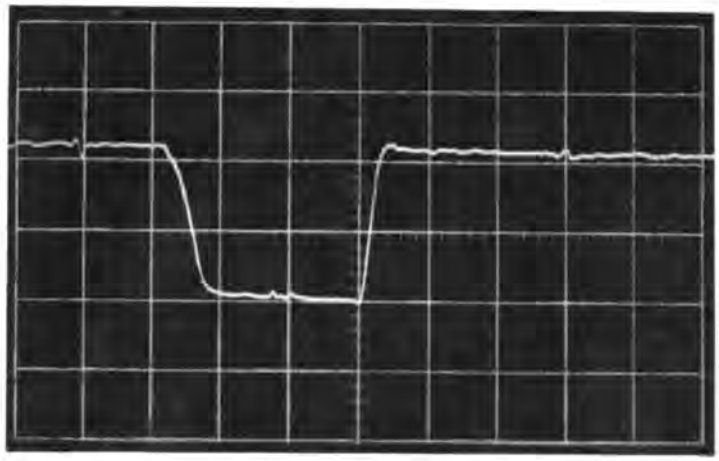
5 volts/div.



A



B



C

Figure 125. Central Processing Unit

Core Storage Waveforms

Thousands Decode Switches

Figures 126A, B, and C are *voltage* waveforms on core. They were scoped at 01A1 F04C on 42.57.11.2 under various conditions. 01A1 F04C is the scope test point for the THOUSANDS decodes switches in the 8 × 10 matrix.

Scope Setup

Triggering: Ext. plus, time 000-030 pulse at console.

10 volts/div.

Time: Exactly 1 complete clock cycle displayed (000-000).

Machine Operation

Manually enter a 1 bit from the console in the Alter mode while holding. Enter key is pressed.

Figure 126A shows the *correct* waveform seen when 1 THOUSANDS decode switch is conducting.

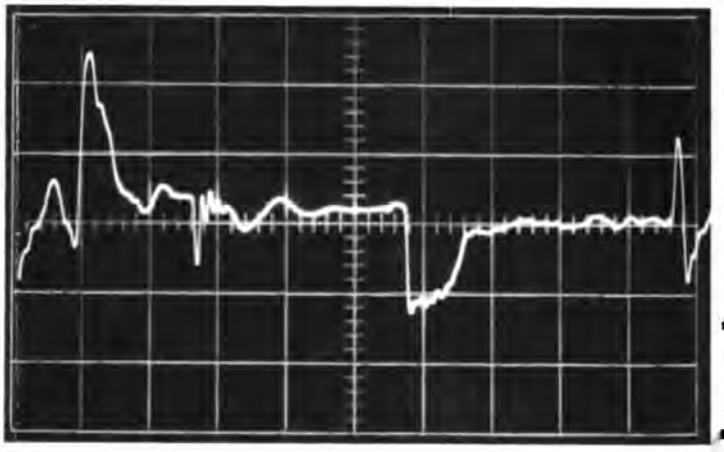
Figure 126B is the *incorrect* waveform seen when none of the THOUSANDS decode switches are conducting.

Figure 126C shows the *incorrect* waveform when more than 1 THOUSANDS decode switches are conducting.

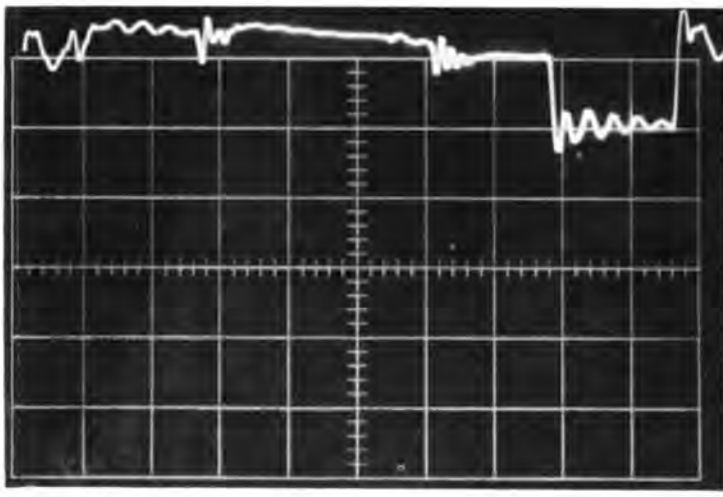
The significant thing to notice between Figures 126A and C is the width of the negative pulse at approximately time 070.

Note: In Figure 126B, as well as 127B, 128B, and 129B, it is not the time function of the trace but the fact that it is at a *high plus potential* for the greater part of the cycle that is important.

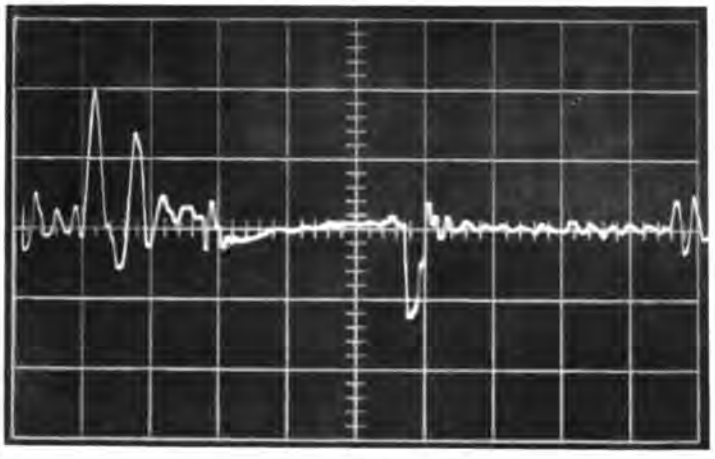
These waveforms will differ slightly from machine to machine.



A



B



C

Figure 126. Core-Storage Voltage Waveforms

Tens Decode Switches

Figures 127A, B, and C show voltage waveforms seen at the test point on the TENS decode switches (01A1 F05C) on 42.57.11.2 under the same conditions as those of the THOUSANDS shown on the preceding pages.

The scope setup is the same.

Triggering: Ext. plus, Time 000-030 pulse.

10 volts/div.

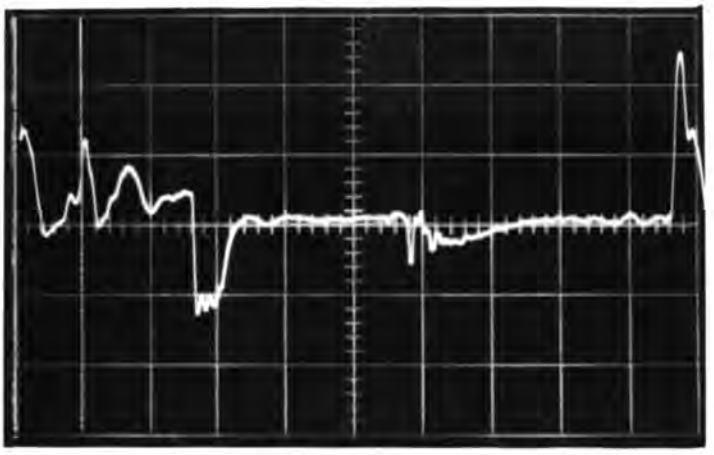
Time: 1 complete clock cycle displayed.

Enter a 1-bit manually from the console holding the enter key pressed.

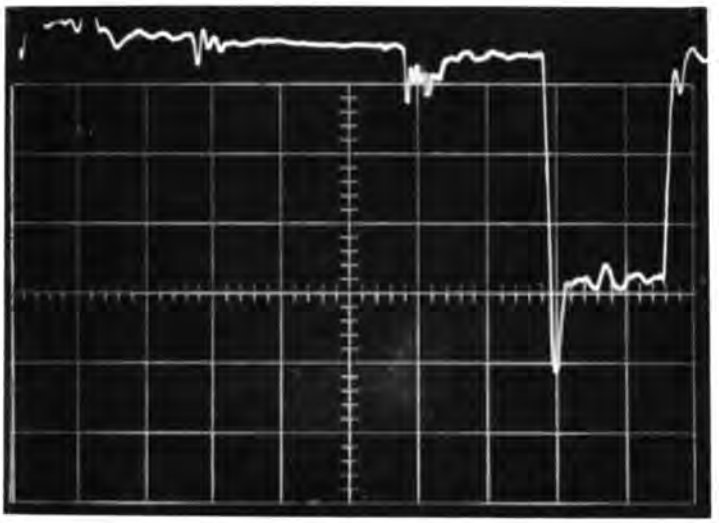
Figure 127A shows the *correct* waveform seen when 1 TENS decode switch is conducting.

Figure 127B shows the *incorrect* waveform when no TENS decode switches are conducting.

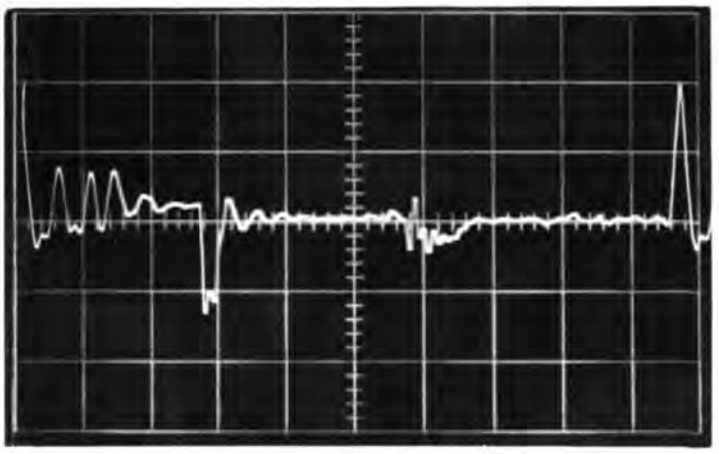
Figure 127C is the *incorrect* waveform when more than 1 TENS switches are conducting. Again, the significant thing to notice between Figures 127A and C is the width of the negative pulse at approximately time 035.



A



B



C

Figure 127. Tens Decode Voltage Waveforms

Hundreds Decode Switches

Figures 128A, B, and C show the voltage waveforms at the test point (01A1 F07C) on 42.57.11.2 for the HUNDREDS decode switches under the same conditions preceding.

Scope Setup

Triggering: Ext. plus, time 000-030 pulse.

10 volts/div.

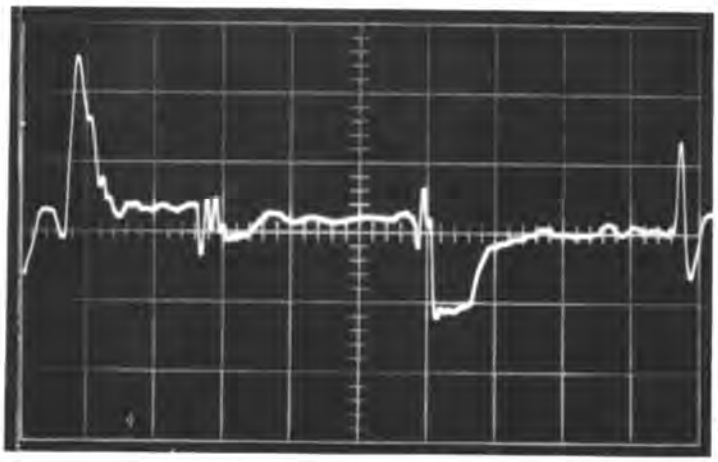
Time: 1 complete clock cycle displayed.

Enter a 1-bit manually from the console, holding the enter key pressed.

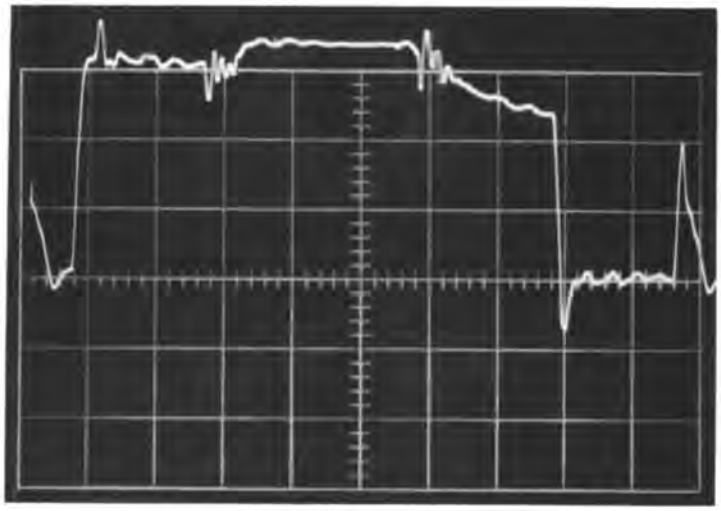
Figure 128A is the *correct* waveform when 1 HUNDREDS decode switch is conducting.

Figure 128B is the *incorrect* waveform when no HUNDREDS decode switches are conducting.

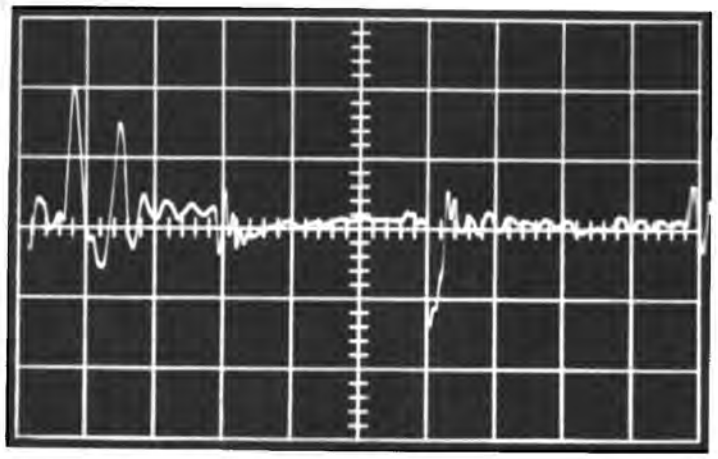
Figure 128C is the *incorrect* waveform when more than 1 HUNDREDS decode switches are conducting. Again, note the width of the negative pulses at time 070 in Figures 128A and C.



A



B



C

Figure 128. Hundreds Decode Voltage Waveforms

Units Decode Switches

Figures 129A, B, and C show the voltage waveforms at the test point (01A1 F08C) on 42.57.11.2 for the UNITS decode switches under the preceding conditions.

Scope Setup

Triggering: Ext. plus, time 000-030 pulse.

10 volts/div.

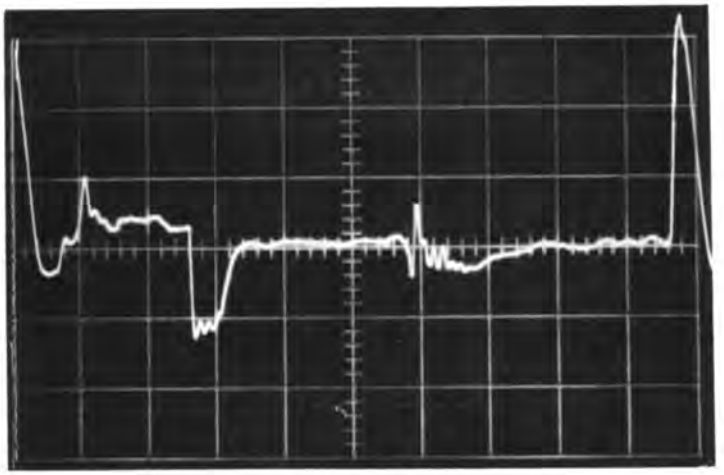
Time: 1 complete clock cycle displayed.

Enter a 1-bit manually from the console holding the enter key pressed.

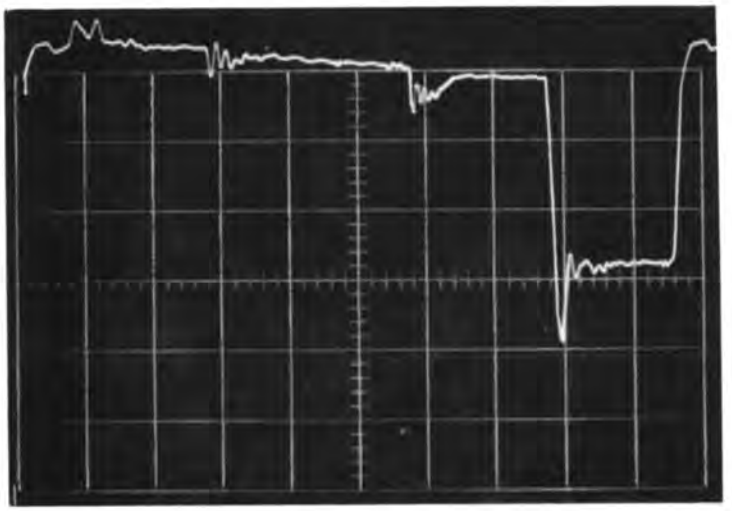
Figure 129A is the *correct* waveform when 1 UNITS decode switch is conducting.

Figure 129B is the *incorrect* waveform when no UNITS decode switches are conducting.

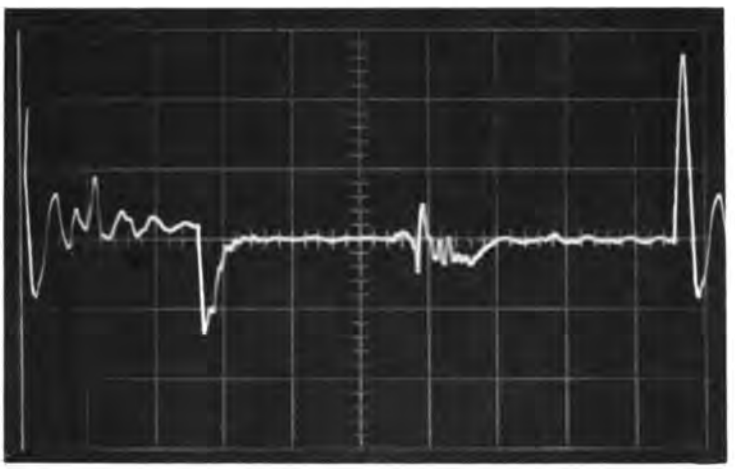
Figure 129C is the *incorrect* waveform when more than 1 UNITS decode switches are conducting. Again, note the width of the negative pulses on Figures 129A and C at approximately time 035.



A



B



C

Figure 129. Units Decode Voltage Waveforms

Current Waveforms on X-Drive Lines

Figures 130A and B show waveforms obtained by using a current probe. The *current* probe was on an X-drive wire where it terminated at the terminator-resistor panel shown on logic 42.40.41 (I.F.C.).

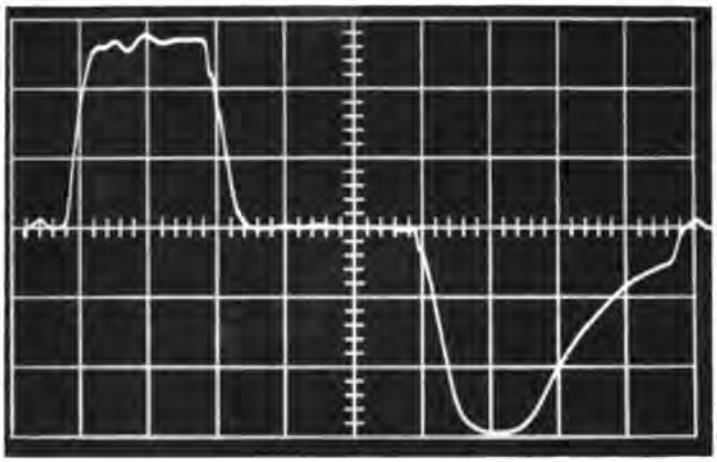
Scope Setup

Triggering: Ext. plus, time 000-030 pulse 100 ma/div.
Time: 1 complete clock cycle displayed (000-000).
Enter a bit from the console.

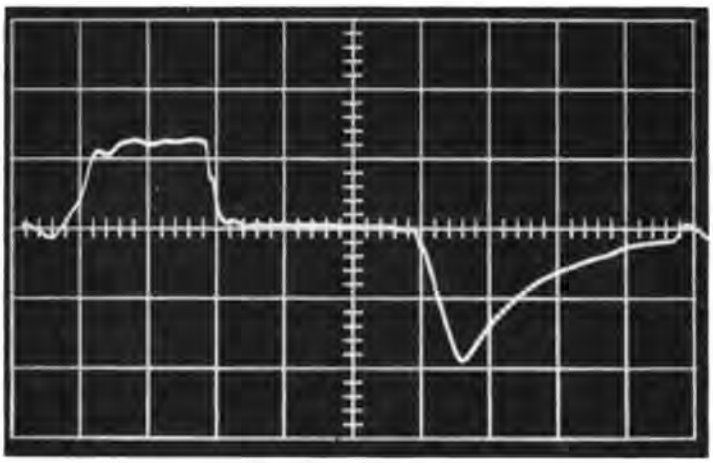
Figure 130A shows approximately 275 milliamperes of current flowing through the X-wire.

The correct current on an X- or Y-drive line should be approximately 270 milliamperes (Stage II, I.F.C.). It will vary somewhat with different temperatures and other conditions.

Figure 130B shows an incorrect amount of current flowing on the same X-wire. The amount is approximately 130 milliamperes or roughing one-half the amount in Figure 129C. Two X-wires were carrying current in Figure 130B because of a machine failure (2 HUNDREDS decode switches were conducting); therefore the current is halved.



A



B

Figure 130. X-Drive Current Waveforms

Current Waveforms on Y-Drive Lines

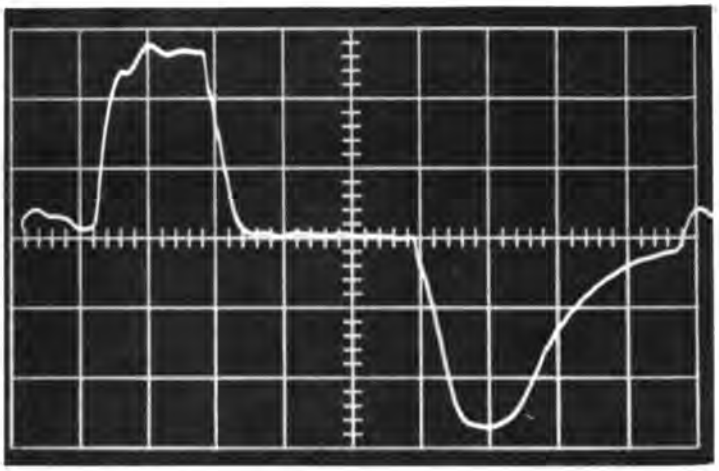
Figures 131A and B show current on Y-drive lines. The current probe was on a Y-drive line at the terminator resistor panel shown on logic 42.40.41 (I.F.C.).

Scope Setup

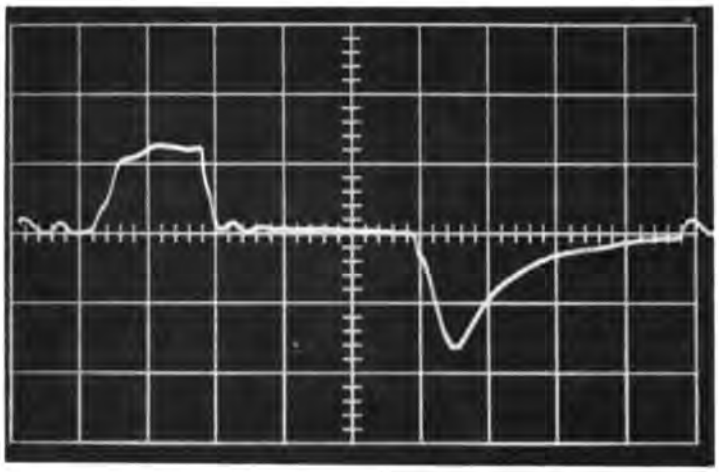
Triggering: Ext. plus, time 000-030 pulse 100 ma/div. 1 complete clock cycle displayed (000-000) entering a bit from the console.

Figure 131A shows 270 milliamperes of current flowing. Because the current should be approximately 270 milliamperes, Figure 131A is *correct*.

In Figure 131B too little current is flowing. This is because 2 TENS decode switches were conducting; therefore the current is halved.



A



B

Figure 131. Y-Drive Current Waveforms

Current on Outputs of Units and Tens Decode Switches

Figures 132A and B show *current* waveforms to be seen on the outputs of units and tens decode switches.

For Figure 132A the current probe was connected on the output pin of the TENS 9 decode switch (01A1 E08P) on 42.54.11 (I.F.C.).

The correct amount of current on the output of a decode switch should be approximately 340 milliamperes (Stage II, I.F.C.); therefore the waveform in Figure 132A (approximately 350 ma) is correct.

With 2 TENS decode switches conducting because of a circuit failure, the current is halved as shown in Figure 132B (approximately 170 ma).

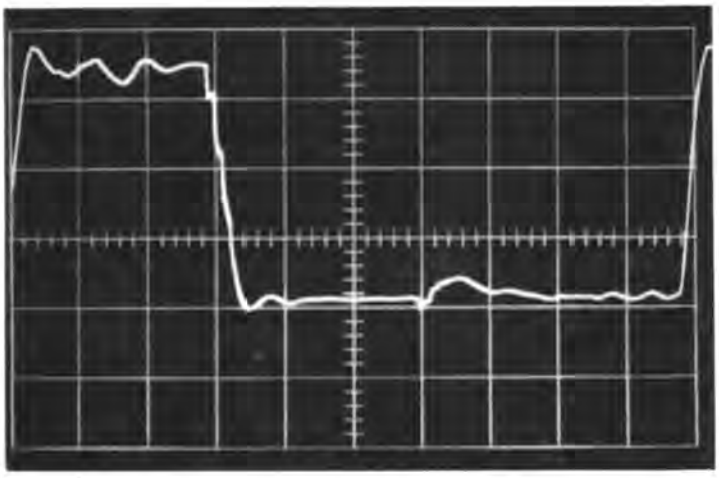
Note: These same waveforms will apply to the UNITS decode switches also.

Scope Setup

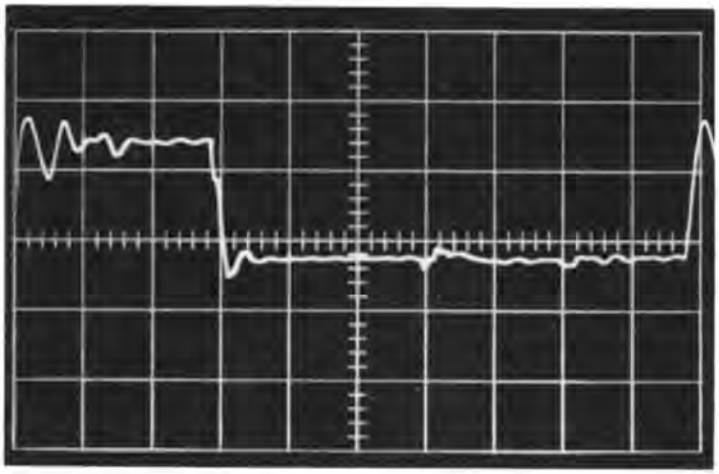
Triggering: Ext. plus, time 000-030 pulse.

100 ma/div.

1 complete clock cycle displayed (000-000). Entering a bit from the console.



A



B

Figure 132. Units and Ten Current Output

Current on Outputs of Hundreds and Thousands Decode Switches

Figures 133A and B show *current* wave forms to be seen on the outputs of hundreds and thousands decode switches.

For Figure 133A the current probe was connected on the output pin of the HUNDREDS 2-3 decode switch (01A1 E19E) on 42.53.11 (Stage II, I.F.C.).

The *correct* current is approximately 340 milliamperes making the waveform in Figure 133A correct (approximately 350 ma).

With 2 HUNDREDS decode switches conducting, the current is halved as seen in Figure 133B (approximately 175 ma).

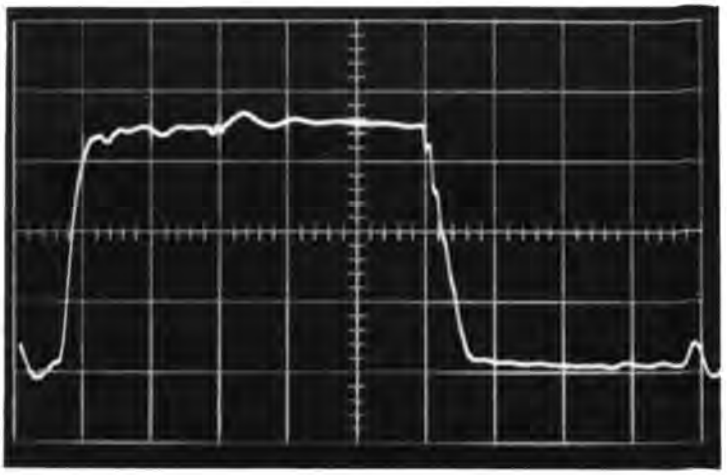
Note: These same wave forms will also apply to the THOUSANDS decode switches.

Scope Setup

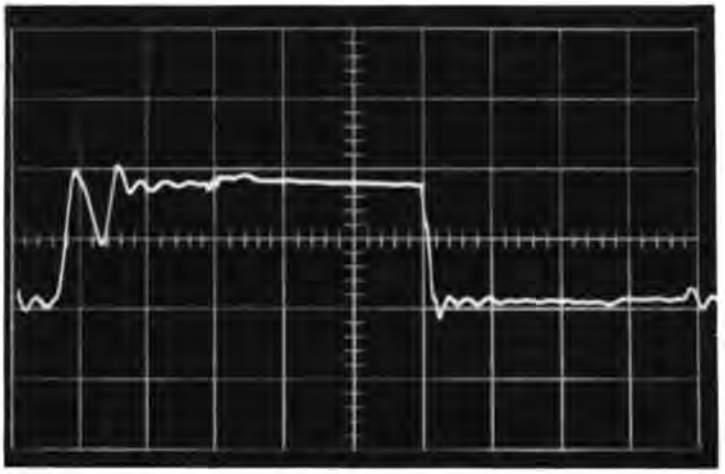
Triggering: Ext. plus, time 000-030 pulse.

100 ma/div.

1 complete clock cycle displayed (000-000). Entering a bit from the console.



A



B

Figure 133. Hundreds and Thousands Current Output

Sense Line Outputs

Figures 134A and B are sense-line outputs. They were scoped at the sense wire output of core storage. Both read and write pulses are apparent.

A 561A scope was used and the setup was as follows:

Channel 1 Input: Connected to 01A1 D15A on 42.59.11.2 (I.F.C.).

Channel 2 Input: Connected to 01A1 D15C (same logic page).

Triggering: Ext. plus, time 000-300 pulse.

.1 volt/div.

1 complete clock cycle displayed (000-000).

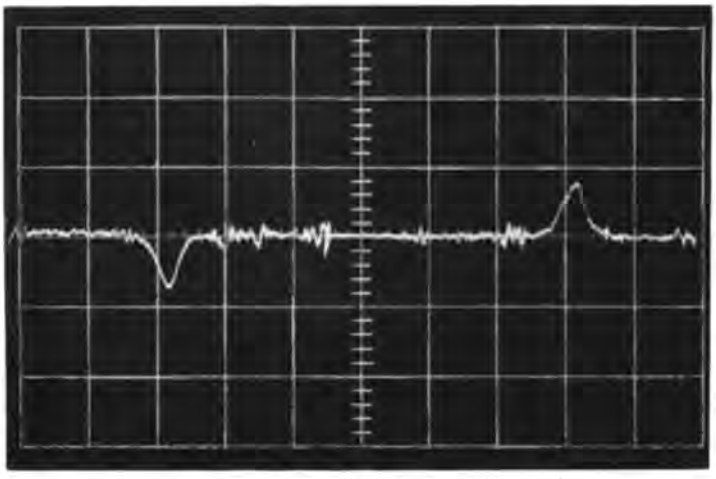
Mode Switch: Added setting.

Note: Turn the red button on the mode switch to INVERT CHANNEL 1.

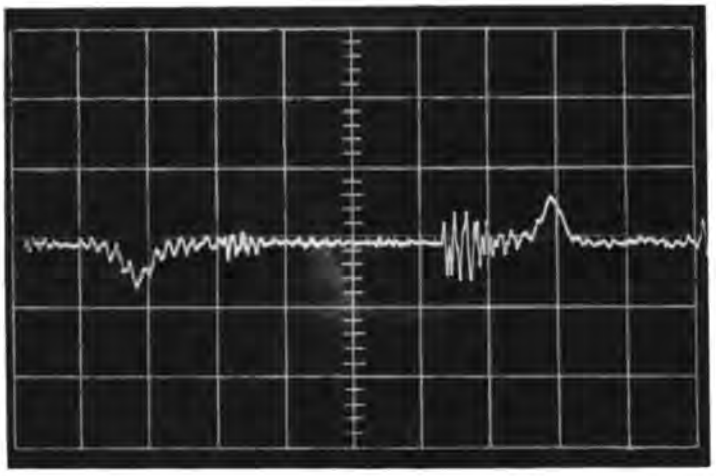
Machine Operation

Entering a word mark from the console by holding the enter key pressed.

Figure 134A was taken on a 4k machine while Figure 134B was taken on an 8k machine which may be the reason for the noise spikes just before write time.



A



B

Figure 134. Sense Line Output

Open Current Source Cards

Figure 135A is the wave form seen with a voltage probe on the test point for the UNITS decode switches (01A1 F08C) on 42.57.11.2 (Stage II, I.F.C.).

The photograph was taken with an open current source card (01A1 F16 pin G open) on 42.57.11.2.

Scope Setup

Triggering: Ext. plus, time 000-030 pulse.

10 volts/div.

1 complete clock cycle displayed.

Machine Operation

Entering a bit from console.

Figure 135B is the output of the UNITS 9 decode switch (01A1E17) on 42.53.11.2 (Stage II, I.F.C.). The *current* probe was connected to pin P of that card. The simulated trouble on the machine was the same as above (open current source).

Scope Setup

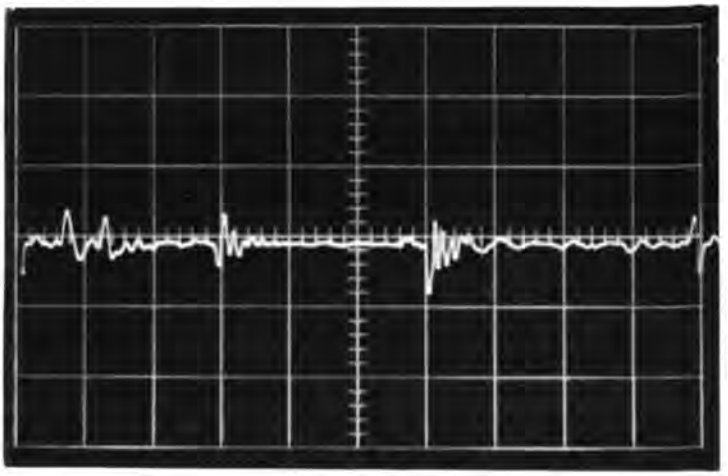
Triggering: Ext. plus, time 000-030 pulse.

100 ma/div.

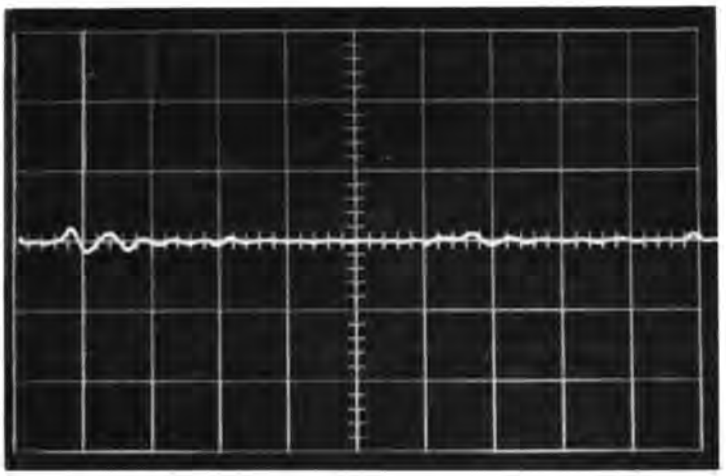
1 complete cycle displayed.

Machine Operation

Entering a bit from console.



A



B

Figure 135. Open Decode Switch Output

I/O Unit Waveforms

1402 Read Brushes and Impulse CB's

Figures 136A, B, and C, are a series of photographs illustrating 1402 read brush and CB relationships. To get these three photographs the following steps were performed.

Scope Setup

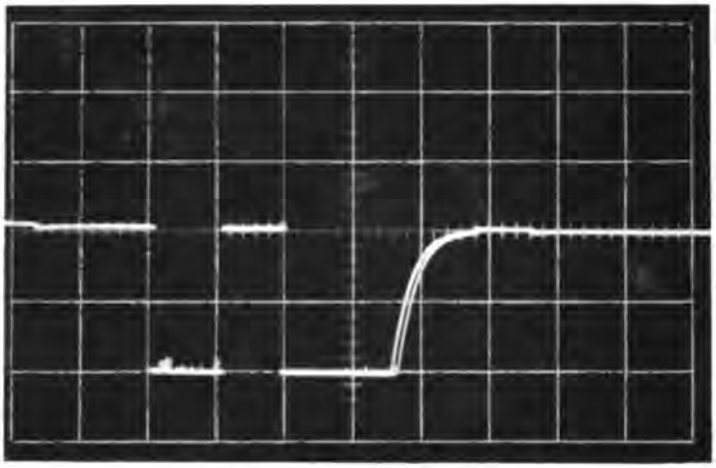
1. Cards were punched with the same digit in any 2 columns and put in the read hopper.
2. A read and branch routine was performed 1 400 –.
3. The read brush wire was pulled from one of the punched columns and the scope probe connected to the brush.
4. The scope was triggered internally with the X5 control operated.
   a. 10 volts/div.
   b. 5 ms/div.

In Figure 136A the scope trace is at –20 volts when the brush is made through the hole in the card. During the time that the brush is made, the CB makes putting 0 volts on the contact roll (short 0 volt trace within time that trace is at –20 volts). Then CB breaks but brush is still made. Note the slight bounce when the brush first makes.

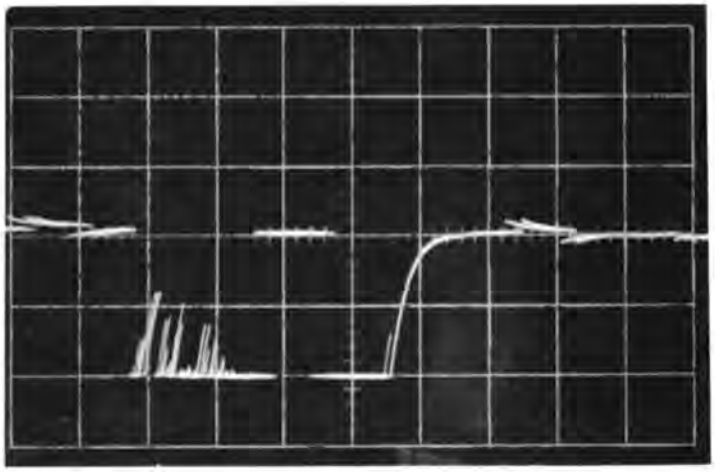
In Figure 136B, the brush is bouncing more now, but not enough to keep the CB impulse from getting through.

In Figure 136C, the brush is bouncing severely enough that the CB impulse is not getting through.

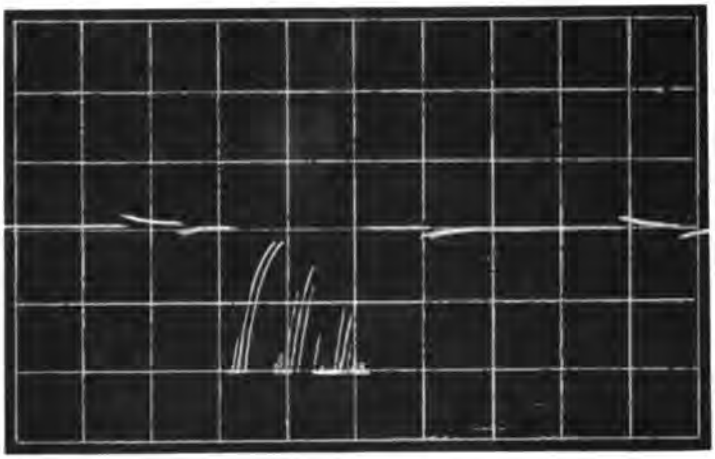
Note: Because two card columns were punched with the same digit, either brush bouncing is seen on the scope.



A



B



C

Figure 136. Read Brush and Impulse CB Waveforms

1402 Scan CB's

Figures 137A and B are pictures of RL-4 bouncing. RL-4 is a scan CB for even digits. When this CB breaks, it is a signal for the 1401 to take read scans for that particular digit.

To get the photographs the following was done.

Scope Setup

RL-4 was isolated (load was removed).

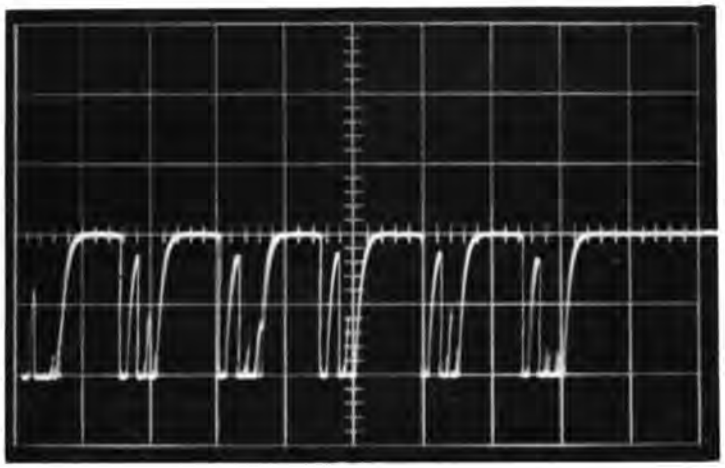
Triggering: Triggered internal minus on RL-4.

5 ms/div.

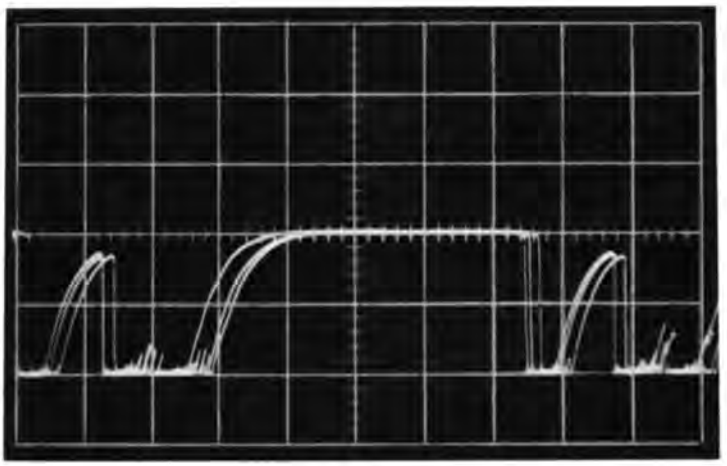
10 volts/div.

The trace is deflected to −20 volts whenever the CB is made. As can be seen in Figure 31, the CB is bouncing.

Figure 137B is the same trace as in Figure 137A but with the ×5 control in effect.



A



B

Figure 137. Scan CB Waveforms

1403 Hammer Response Lines

Figures 138A and B are waveforms seen on the hammer-response lines.

The following setup was used.

Scope Setup

A 1 was entered into core position 201, a 3 in 204, and a 5 in 207.

A print and branch routine was performed (2 400–).

The scope was triggered on Ext. plus on the hammer-fire line of hammer driver 1 (01B5 B05D) on 36.38.61.2 (I.F.C.).

5 μs/div.

20 volts/div.

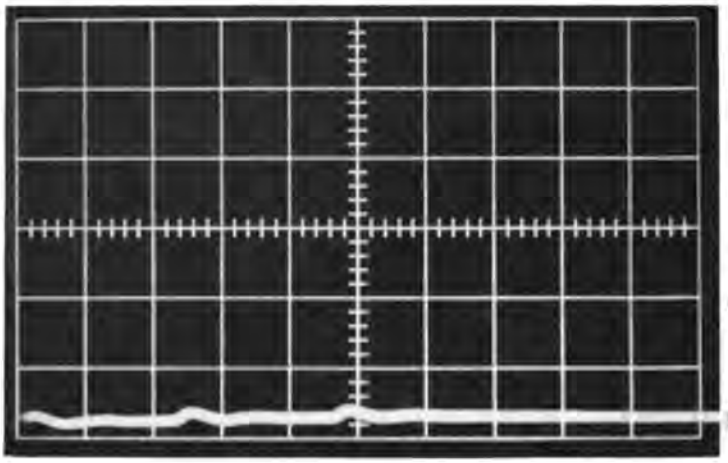
The scope probe was connected on the hammer response output pin of hammer driver 4 (01B5 B05H) on 36.38.61.2 (I.F.C.).

The most negative portion of the trace in Figure 138A represents —60 volts. (The reference line was moved slightly upward to enable easier viewing of the slight shift in the hammer response line.)

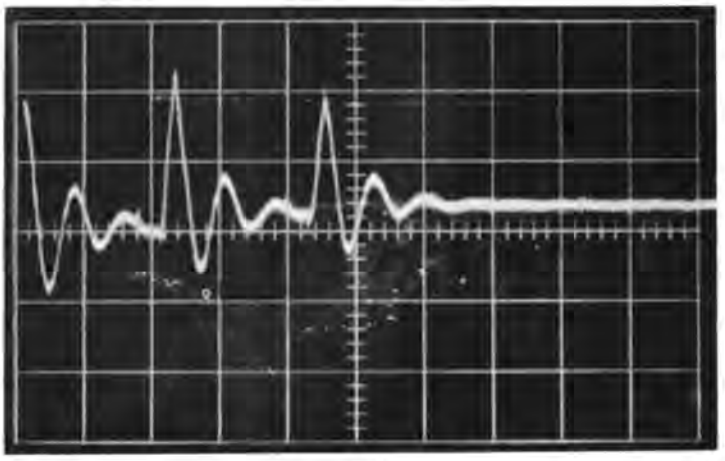
The first bump on the trace is hammer driver 1's response line (indicating hammer driver 1 firing). One cycle later hammer driver 4 is fired indicated by second bump on the line. Then hammer driver 7 fires 1 cycle later.

By changing the input switch control to the ac setting, and going to 1 volt/div., Figure 138B was obtained. The positive shift on the line which indicates hammer firing is quite apparent with this setting.

Note: These hammer-response lines can be viewed in this manner on both buffer and non-buffer machines.



A



B

Figure 138. Hammer Response Waveforms

1403 Drum Pulse

Figure 139 is a photograph of the output of the 1403 drum-read head scoped at the input to the first sense amplifier (SA-1, pin B on 01.08.1).

The scope probe was grounded to pin J on the same card to eliminate noise.

Scope Setup

Triggering: Ext. minus on the output of the home trigger (01A6 A10N) on 36.31.11.2 (I.F.C.).

200 μs/div.

.1 volts/div. (100 mv/div.).

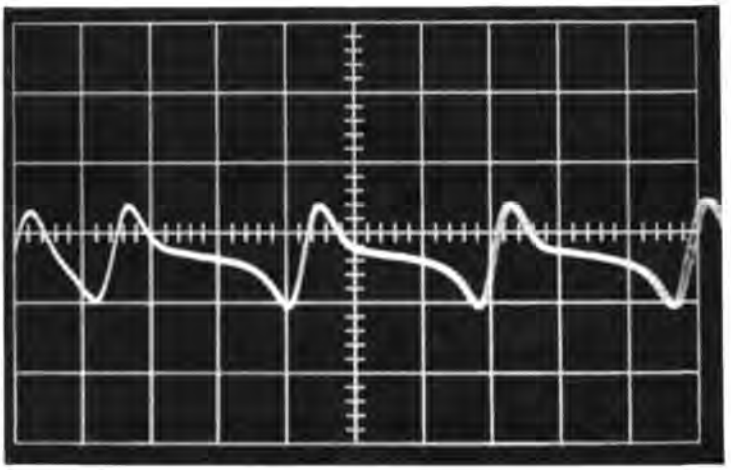


Figure 139. Drum Pulse

Unusual 1403 Circuit Waveform

Figure 140 is an example of the unusual type of waveform that can be seen when scoping transistor *base* pins in 1403 control circuitry. This waveform was scoped at 01A6 B17P on 36.34.21.2 (I.F.C.-N.P.F.).

Scope Setup

Triggering: Internal plus.

2 volts/div.

1 ms/div.

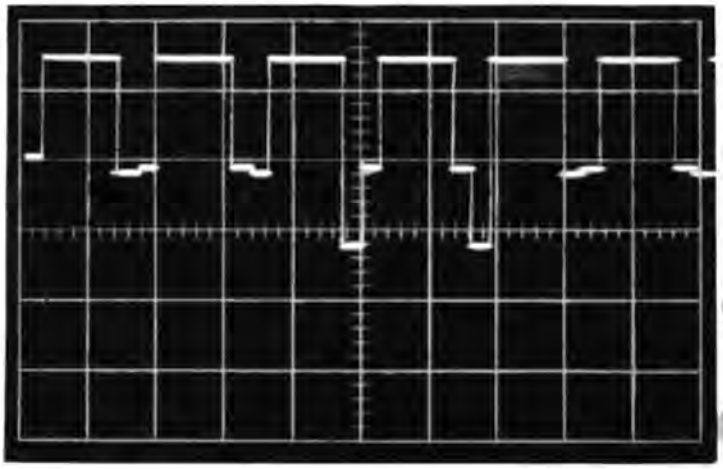


Figure 140. Unusual 1403 Transistor Base Waveforms

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