IBM Customer Engineering

Manual of Instruction

Tape Adapter Unit

IBM®

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MAJOR REVISION (December 1960)

This edition, Form 223-6847-2 is a major revision but does not obsolete Form 223-6847-1. Significant changes in timings have been made in this manual.

CONTENTS

FOREWORD

This manual discusses the basic functions of the IBM Tape Adapter Unit (TAU). Because TAU can be used by several systems, no attempt is made to tie TAU to any particular system. Instead, "external system" or "external system control unit" are used to refer to an outside control.

This manual has been prepared for teaching and as an aid for learning. Engineering changes may alter timings, logic, and other information presented here; therefore, the reader should not use this information alone as a reference manual or servicing aid.

Section 1.0.00 of the manual covers general information and logic of TAU. Included in the general information section is an introduction to TAU and brief explanations of TAU operation.

Section 2.0.00 explains in general terms the basic timing and controls used in TAU.

Section 3.0.00 is a more detailed description of the functional units used in TAU. Included in the functional units are the final amplifier, error checking circuits and timing circuits.

Section 4.0.00 explains, in detail, TAU operations. Logic flow diagrams, block diagrams and sequence charts are included to aid the reader.

Section 5.0.00 describes diagnostic controls included in TAU circuits.

IBM TAPE ADAPTER UNIT

1.1.00 GENERAL INFORMATION

1.1.00 INTRODUCTION

The IBM Tape Adapter Unit (TAU) is a standard assembly used to control the operation of 729 II and IV tape units. TAU by itself is not a complete tape control unit, but contains all the common features found in all previous tape control units. To make TAU compatible with any particular system, the user must supply the additional control circuits specific to the operation of his system. By adding the necessary control circuits to TAU, a complete tape control unit for any system using 729 II or IV tape units can be achieved.

The common circuits contained in TAU are controls for writing, reading, backspacing, rewinding and checking. TAU has complete control of the tape unit (except for selection) and initiates all control and data flow functions from system to tape and tape to system.

Besides the basic functions mentioned above, TAU also can read and write at a high density or a low density rate on either the 729 II or IV tape units. The high density rate is 500 bits per inch and the low density is 200 bits per inch. TAU has the necessary oscillators and control circuits to switch to either density under an external command signal.

Figure 1.1-1 illustrates the relationship of TAU to an over-all system. As can be seen, TAU has the only direct communication link with the tape unit. To perform any particular tape operation, the external system makes the request to TAU. TAU performs the operation and returns the results to the system. All data are also relayed through TAU between tape and system.

Because it is not known what systems will use TAU, timing and data lines are made available for use by the external system. These timing and data lines logically tie TAU into any added control circuits to achieve the complete tape control.

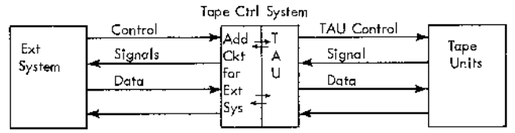


FIGURE 1.1-1. TAU SYSTEM RELATIONSHIP

1.2.00 PHYSICAL DESCRIPTION

TAU is an assembly of internally cabled gates. The unit is made in two forms to fit either the standard large module (sliding gate) or the standard small module (swinging gate). The card chassis assembly for the sliding gate is designed for mounting in gate positions B or D. The card chassis assembly for the swinging gate module is designed for mounting in gate positions 1, 2, 3, and 4 of the lower module.

The names given to the two different packages are TAU 1 for the sliding gate module and TAU 2 for the swinging gate module . TAU 1 (sliding gate) contains all the basic TAU functions plus the added circuits for the dual density operation for both 729 II and 729 IV tape units. TAU 2 (swinging gate) also includes all the necessary circuits for all basic TAU functions, but because of space limitations, there are two TAU 2's. Each TAU 2 is packaged in the swinging gate module. One package is for 729 II operation at both densities and the other is for 729 IV operation at both densities. There are other minor differences between TAU 1 and TAU 2, but they are identical as to logic. Any minor variations between the two will be noted when the operations are explained in the later sections of the manual.

When the system designer mounts TAU in an available frame, he must provide the power supply, CE test panel, and external cables necessary for the efficient operation and maintenance of the unit.

The circuits used in TAU are the standard alloy junction transistor current switching circuits.

1.3.00 MACHINE LANGUAGE

All data registers in TAU use binary coded decimal (BCD) form. TAU operates on one character at a time. A character in TAU is made up of a 6-bit combination (B, A, 8, 4, 2, 1) and a check bit (C). The check bit can be written or read to make the bit structure either odd or even, depending upon the operation being performed. In a system not using the BCD system, the bit arrangement for the TAU registers must be performed in the external control area because information is not alter in TAU, but simply routed through in the form in which it was received.

1.4.00 GENERAL MACHINE LOGIC

Except for selection circuits, tape units are under complete control of TAU. Any tape operation called for by an external system must make the request of TAU. Upon receiving the request for operation signal, TAU will start and control the timing and data transfer from beginning to end. TAU circuits provide all necessary timings for initiating and stopping tape movement, developing all necessary delays for any read or write operation and for all data transfer and checking procedures. Following is a logical description of TAU operations.

1.4.01 Write

To perform a write operation in a tape unit (Figure 1.4-1), TAU must first receive a write request signal from the system. This signal is called "write call" and initiates the proper circuits in TAU. TAU sends a "go" signal to the tape unit and tape starts moving. Because it takes time for the tape to reach its proper speed, TAU initiates a write delay before the write circuits become active. When the write delay is completed, TAU starts a write clock to control writing. Input data lines from the system are active to TAU. The write clock pulses set the data into a read-write (R-W) register in TAU. As soon as the information is in the R-W register, it becomes available to the tape unit. Another write clock pulse is developed into a write pulse and sent to the tape unit, where it initiates the writing action. The write clock, when started, is in repetitive cycles, and the writing action continues until stopped by another request signal from the system. This request signal, called "disconnect call,"

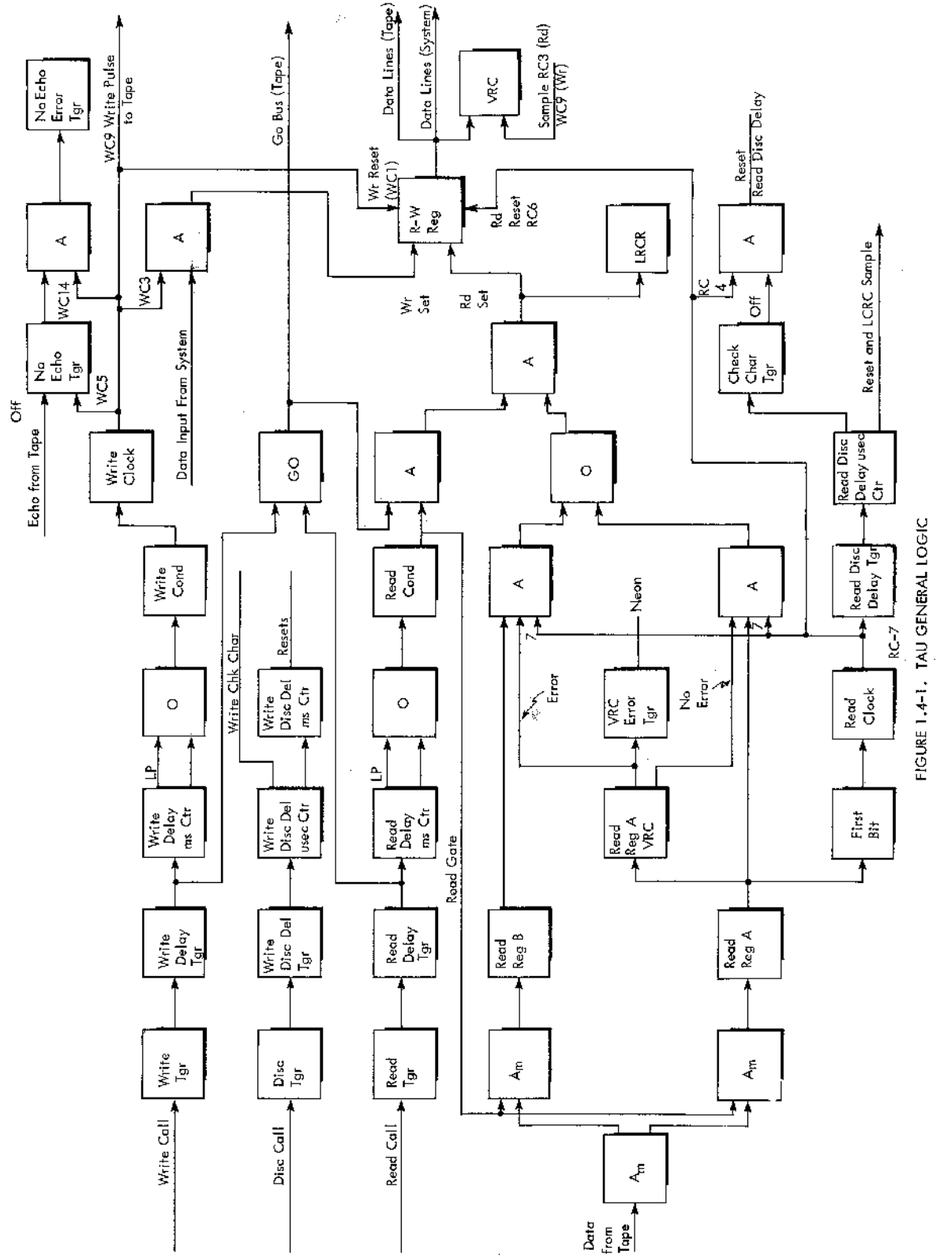


FIGURE 1.4-1. TAU GENERAL LOGIC

initiates circuits in TAU to complete the operation. The operation is completed by writing a check character and stopping the tape, under TAU timing control.

As data flow through TAU, error checking circuits are active to insure proper operation. These error circuits are explained in Section 3.3.00.

1.4.02 Read

A read operation (Figure 1.4-1) is started when TAU receives a "read call" signal from the system. As in the write operation, TAU develops a "go" signal to start tape moving. A read delay is initiated before the read circuits become active, to allow the tape to attain proper speed. When the read delay is completed, final amplifiers are conditioned to accept information from tape. When a character is read from the tape, it is sent to TAU through the final amplifier, and set into two registers called read register A and read register B. The two read registers have different acceptance levels to discriminate against noise pulses (read register A) and low output levels (read register B). The first character set into the read registers starts a read clock for one cycle. The read clock controls the data flow through TAU. During the read clock cycle, read register A is checked for error. If read register A is in error, a read clock pulse sets the read-write (R-W) register to read register B. If read register A has no error, the read clock pulse sets the R-W register to read register A. Once the character is set into the R-W register, it becomes available to the system. The read clock stops after the R-W register is set. The next character set into the read registers starts the clock again for one more cycle and so on, until the complete record is read. In each read clock cycle, a timing circuit is activated to try to stop the read operation, but as long as characters arrive in specified time intervals, it is reset before it can complete its function. Because the check character time is greater than the normal character time interval, the timing circuit activated during the last normal character cycle is allowed to run long enough to initiate the stopping action. The end operation circuits process the check character, perform read circuit resets, complete error checking procedures, and stop the tape.

During the read operation, error detection circuits are active to insure proper read operation. The checking procedures during a read operation are covered in Section 4.1.02.

Read During Writing

The two-gap head on the tape unit makes it possible to read the record being written. The read portion of the write operation is used to check the record on tape for error. The write control circuits initiate a read operation. This read operation operates the same as a normal read operation, except that the data being read are never set into the R-W register. All checking of the record read is done with the data in the read registers. The write operation is not completed until the read operation is finished. The error conditions in the read check during writing are covered in Section 4.1.02.

1.4.03 Backspace

A backspace operation is essentially a read operation in a backward direction. The only difference is that, in a backspace operation, no data are transferred from the tape to the system. The operation consists only of getting from the end of a record back to its beginning.

When the "backspace call" request signal is received in TAU, the operation is started. All tape motion in a backward direction must be done with the tape unit in read status. TAU first checks the status of the tape unit. If the tape unit is in write status, TAU initiates forward tape movement for a short time before setting read status to insure that noise, created in changing to read status, will be far enough out on the tape to be erased in the next write operation. Once the tape unit is in read status, TAU will set backward status and then start the tape moving. Characters are set into the read registers and start the read clock as in any read operation. A timing circuit is started from each read clock cycle and, provided characters arrive in timed intervals, the timing circuit is reset on the next character cycle. When the beginning of the record is reached, the timing circuit stops the operation and resets the tape unit to forward status. The R-W register is not set during the backspace operation and no error checking circuits are active.

1.4.04 Write Tape Mark

A write tape mark operation is a one-character write operation. On receiving the write tape mark call signal, TAU activates the normal write operation circuits. Because this is a write tape mark operation, the R-W register is conditioned within TAU to set to 8, 4, 2, and 1, the bit structure of a tape mark. A write clock pulse then sets the character into the R-W register, making it available to the tape unit write circuits. Another clock output is developed into a write pulse and sent to the tape unit initiating the writing action. At the same time the write operation is started, a disconnect operation is also started to end the operation. This insures a one-character record (tape mark), and a check character is written on tape. All normal checking circuits are active.

In a read operation, TAU recognizes a tape mark and makes the recognition available to the system. In every read operation a first character trigger is turned on for the first read cycle. If the character that sets into read register A is a tape mark, a "first character tape mark" line is made available to the system.

1.4.05 Rewind

Two rewind operations are included in TAU. One is a normal rewind operation, and the other is a rewind-unload operation. Both operations are identical for the actual rewind operation, but the rewind-unload operation causes the tape to unload.

A rewind call signal turns on a rewind trigger in TAU. The output of the rewind trigger is sent to the tape unit, where it initiates the rewind. As soon as the tape unit goes into rewind status, TAU resets the rewind trigger and the TAU operation is complete.

A rewind-unload call signal turns on a rewind unload trigger in TAU. The output of the trigger initiates the rewind action in the tape unit and, in addition, sets control circuits for unloading the tape when the rewind is completed. As soon as the tape unit is in rewind status, the rewind-unload trigger is turned off and TAU operation is complete.

1.4.06 Erase

An erase call signal to TAU turns on an erase trigger. With the erase trigger on, the next write operation is forced to take a longer write delay before allowing writing to begin. In effect, it causes a tape unit to skip over a section of tape.

1.4.07 Error Checking

In all operations where data are being transferred from TAU to either the system or tape unit, the information, while in TAU, is checked for various errors. The error checks performed in TAU consist of vertical redundancy checks, write echo checks, write compare checks, and a longitudinal redundancy check. Any of these errors turns on a TAU error trigger. The output of the trigger is available to the system, and is the only indication of an error to the external system. Besides the TAU error trigger, a read register A vertical redundancy error, a R-W register vertical redundancy error, and an echo error will turn on triggers in the TAU that are used only to light indicator lamps. Following is a description of each type of error condition.

Vertical Redundancy Check

The vertical redundancy checker (VRC) determines the vertical bit structure of a character for either an odd or even bit count. Normally the VRC is set to check for an even bit count, but an "odd redundancy call" signal from the system turns on an odd redundancy trigger that conditions the VRC for an odd bit count. Whenever a character bit structure count does not agree with the type of vertical redundancy check called for, a VRC error line becomes active. There are two VRC's in TAU. The outputs of read register A condition one VRC and the outputs of the R-W register condition the other. Any time data appear in the R-W register they are checked. If the bit count is different from the type of check called for (odd or even), a clock pulse samples the error line and turns on the TAU error trigger and the R-W register VRC error trigger. The R-W register VRC error trigger is used only as a neon indication on the TAU wiring panel.

In any read operation, the output of read register A is checked. If a vertical redundancy error exists in a read check during writing operation, the TAU error trigger and read register A VRC error trigger are turned on. If the error exists in a normal read, the read register A VRC error trigger is turned on but the TAU error trigger is not. The VRC error line in a normal read is used to gate the outputs of either read register A (no error) or read register B (error) to the R-W register.

Echo Check

To insure that something is being written on tape during a write operation, TAU checks for return echoes from the tape unit. During the write operation, a no-echo trigger is turned on. When writing takes place in the tape unit, the tape write circuits develop an echo and return it to TAU. Any echo return will reset the no-echo trigger. If the tape writing circuits are not active, no echoes are developed and the no-echo trigger remains on. At the end of the write cycle, the no-echo trigger output is sampled. If the trigger is on, the echo error and the TAU error triggers are turned on.

Write Compare

While read checking during a write operation, the character in read register A is compared against the character in read register B. If they are not alike, the TAU error trigger is turned on.

Skew Error

A skew error trigger is turned on whenever bits appear after a normal character gate time. The read clock allows a definite amount of time to read all bits of any one character. After this time, all bits of any character should have been read. If any bits appear after this time, the skew error and TAU error triggers will be turned on.

Longitudinal Redundancy Check Register (LRCR)

The LRCR is a seven-trigger binary register which keeps an odd-even count of each bit track. The count of bits in a horizontal track in a write operation should always be even. Assuming no error, the record that is read should also have an even count for each bit track. Before completing any read operation, the LRCR output is sampled. If any trigger is on at this time, the TAU error trigger will be turned on.

1.4.08 Dual Density

The dual density feature of TAU allows TAU to write and read either the 729 II or IV tape units at a high density rate (556 bits/inch) or a low density rate (200 bits/inch).

TAU 1 contains all the necessary circuits to operate both 729 II and IV tape units at either density. Because of space limitations, TAU 2 is packaged to operate on 729 II at either density and another TAU 2 is necessary to operate 729 IV tape units at either density.

TAU 1

A request signal from an external system is received by TAU and sent to the tape unit hi-lo density trigger. The status of the density trigger, returned to TAU, together with the select and ready line of either the 729 II or IV tape unit, conditions the proper oscillators in TAU. The conditioned oscillators feed the read and write clocks and other timing circuits necessary to time TAU to the correct density.

TAU 2

The dual density operation for TAU 2 is identical to that of TAU 1 except that the "sel and ready mod" tape unit is not used to condition the oscillators. This line is not necessary because there is a separate TAU 2 for each tape unit. On TAU 2 the density line from the tape unit serves only to condition the proper oscillator for either density whereas in TAU 1 the proper oscillator for 729 II or IV operation, as well as the dual density condition, had to be met.

2.0.00 TIMING AND CONTROL

2.1.00 TIMING

All the necessary timings and delays required by TAU are generated by oscillator driven binary counters. The timing circuits included in TAU consist of a read clock, a write clock and a delay counter. Because TAU can operate with 729 II and IV tape units at either density, the timings of the various control circuits must vary. By selecting different oscillators, the output of the timing circuits can be varied. Figure 2.1-1 lists the timings and clock pulses for the two different tape speeds at both densities.

2.1.01 Read Clock

The read clock is a four-stage modified binary counter. The clock triggers are labeled RC1, RC2, RC4 and RC8. By gating combinations of the four triggers, pulses from RC1 through RC11 can be obtained. All timings from the read clock will be referred to as RC1, RC2, RC3, and so on to RC11.

Each first bit of a character read during a read operation allows oscillator drive pulses to start stepping the clock. All necessary timings required for data flow and checking on any read operation are obtained from the read clock.

2.1.02 Write Clock

The write clock is a four-stage modified binary counter. Write clock triggers are labeled WC1, WC2, WC4, and WC8. As in the read clock, by gating combinations of the triggers, pulses from WC1 through WC15 can be obtained. All write clock pulses will be referred to as WC1, WC2, WC3, and so on.

Early in a write operation, TAU turns on a control trigger (write condition) which gates oscillator drive pulses to the clock. Since the clock is a binary counter , 16 drive pulses are necessary for one complete cycle. As long as write condition remains on, the clock is in repetitive cycles. When the write operation is ending, write condition is turned off and the clock stops. The clock input is gated also with the WC8 trigger, which insures that all clock triggers are off when the clock stops. All timing pulses for data flow through TAU during a write operation are obtained from the write clock.

2.1.03 Delay Counter

The delay counter is a 9-stage modified binary counter. The delay counter triggers are labeled in binary order from DC1 to DC256. Since the delays required by TAU range from microseconds to milliseconds , the delay counter can count in both the microsecond mode and the millisecond mode. It also has facilities for starting and stopping at any specified point in a cycle. The outputs of the delay counter are obtained by gating combinations of the triggers. Because the delay counter is widely used in all TAU applications, the outputs are labeled according to the gating lines and the count at

DELAY COUNTER USEC CTRL

	729 II Lo	729 II Hi	729 IV Lo	729 IV Hi
Osc	240KC	667KC	360KC	1MC
RDD36	150usec	54.0usec	100usec	36.0usec
RDD128	532usec	192 usec	355usec	128.0usec
RDD136	566usec	204usec	377usec	136.0usec
RDD144	600usec	216usec	400usec	144.0usec
WDD60	250usec	90usec	166usec	60.0usec

DELAY CTR MILLISEC CTRL

	729 II	729 IV
Osc	667KC	10KC
RDD4	.6ms	0.4ms
RDD26 + RDD38	5.7ms (RDD38)	2.6ms (RDD26)
RDD30*	4.5ms	3.0ms
RDD64	9.6ms	6.4ms
RDD152	22.5ms	15.2ms
WDD20	3.0ms	2.0ms
RD44	6.6ms	4.4ms
RD160	24.0ms	16.0ms
WD52	7.8ms	5.2ms
WD80	12ms	8.0ms
WD320	48ms	32ms
D50	7.5ms	5.0ms
D96	14.4ms	9.6ms
D160	24.0ms	16.0ms
Bksp 180	27.0ms	18.0ms
St Rd Cond 32	4.8ms	3.2ms

* TAU 2 only

READ CLOCK OUTPUT

Timing Ref Rise of 1st Bit	729 II Lo	729 II Hi	729 IV Lo	729 IV Hi
Osc	240KC	667KC	360KC	1meg
RC3	12.8usec	4.8usec	8.6usec	3.3usec
RC4	16.9usec	6.3usec	11.4usec	4.3usec
RC5	21.1usec	7.8usec	14.1usec	5.3usec
RC6	25.3usec	9.3usec	17.0usec	6.3usec
RC7	29.5usec	10.8usec	19.7usec	7.3usec
RC7 Reset (Rd)	31.6usec	11.6usec	21.1usec	7.8usec
RC7 Reset (Wr)	44usec	16.1usec	29.5usec	10.8usec

WRITE CLOCK OUTPUT

Timing Ref Rise of 1st Bit	729 II Lo	729 II Hi	729 IV Lo	729 IV Hi
Osc	240KC	667KC	360KC	1meg
WC1	Reference	Reference	Reference	Reference
WC3	8.32usec	3.00usec	5.56usec	2.00usec
WC5	16.6usec	6.00usec	11.1usec	4.00usec
WC9	31.5usec	11.5usec	21.1usec	7.75usec
WC14	54.1usec	19.5usec	36.1usec	13.0usec
WC15	66.6usec	24.0usec	44.5usec	16.0usec

FIGURE 2.1-1. TIMING RELATIONSHIPS

the output circuit. Listed in Figure 2.1-1 are the timing outputs for 729 II and IV operation.

The counter operation is controlled from control triggers turned on during specific TAU operations. Depending upon the timing necessary, either millisecond or microsecond control is conditioned by the controlling trigger. The millisecond or microsecond control gates the proper oscillator drive pulses to the counter. The drive pulses are obtained from outputs of six oscillators. Three oscillators are used for 729 IV operation for the millisecond and microsecond mode, and three oscillators are used for 729 II operation in the millisecond and microsecond mode. The correct oscillators are conditioned by a "sel and rdy Mod II" from the tape unit. All outputs of the delay counter are used to obtain all the delays for tape motion and for completing TAU operations.

2.2.00 INPUT-OUTPUT CONTROLS

Input data and control lines to TAU from the external system are listed in Figure 2.2-1. Also listed are all output lines from TAU to the tape unit. The timing and control data lines required by the external system from TAU are made available at edge connectors. Figure 2.2-2 lists all the lines that are available at the edge connectors.

2.2.01 Interrupts

The pulses and control lines listed in Figure 2.2-3 are interrupt lines made available by TAU. These lines are normally jumpered closed at edge connectors with no change in function. However, when an external system wishes, the interrupt line may be broken and used for a control purpose in the external system. The result of the logic circuit in the external system must be tied back to TAU and complete the function which the interrupt line normally completed, as illustrated in Figure 2.2-4. The basic logic of TAU that is controlled by interrupt lines can be altered by an external system. Because it is impossible to cover all cases when the interrupts are used, the line names in TAU are always labeled as if the line were not interrupted. It is recommended that in study of TAU, in any particular system, the reader familiarize himself with the interrupt lines and their related function and timing in TAU. All illustrations in the manual are treated with the understanding that none of the interrupt lines have been interrupted.

FROM CONTROL UNIT		FROM TAPE UNIT
Early Sample	Machine or Pwr-On Reset	Data Lines
Amplifier Bias	Reg A Only	Write Echoes
Data Lines	Reg B Only	Sol and Rdy M4
All Request Signals	Compare CK	Sel and Rdy M2
Turn on TI	Sel and Rdy MIV	Sel and LP
Turn Off TI	Sel Rdy and Rd	Sel, Rdy and Rd
Manual Op	Sel Rdy and Wr	Sel, Rdy, and Wr
Manual Data Lines	Set Hi Density	Sel Not LP
Manual Write Disc	Set Lo Density	Sel and TI Off
Manual Stop of Error	Thermal Interlock	Sel and TI On
Manaul Error Reset		Hi Density
		Sel and Rewind

FIGURE 2.2-1. TAU EXTERNAL INPUTS

TO CONTROL UNIT		
RC3	WD	Go Reset
RC6	WD52	Set Read Status
WC5	WD80	Read Condition
WC1	WD768	Set Write Status
WC9	WDD	Erase
Write Pulse	WDD20	Backspace
WC14	WDD60	Backward
DC8	Data Lines	Rewind
DC16	Check Char	Rewind Read
DC32	First Char TM	Rewind-Unload
DC64	Error	Sel and Rew
DC128	Busy	Sel and Not LP
RDD	Load Point	Sel and TI On
RDD36	Sel and Load Point	Sel and TI Off
RDD128	Write Tgr	TR Reset
RDD136	Go	Echo Error
RDD144 Only us Sample		Thermal Interlock
RDD152		Reset WR Tgrs
		High Density
TO TAPE UNIT		
Write Bus	Reset Wr Tgrs	Rewind-Unload
Go	Write Pulse	Turn Off TI
Set Rd Status	Backward	Turn On TI
Set Wr Status	Rewind	Set Hi Density
		Set Lo Density

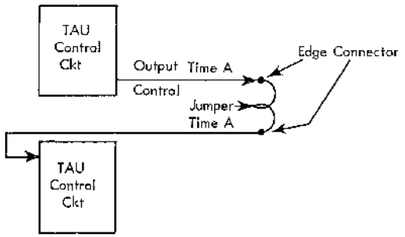
FIGURE 2.2-2. TAU EXTERNAL OUTPUTS

TAU 1 INTERRUPTS	
Name	Function
RC7	Turn on Read Disc Dly
Write Condition	Develop Wr Clock Sample
	Write Clock Drive
WC3	Set R/W Register to Input Data
RDD TR Reset	Reset Rd Disc Delay (RDD)
RDD144 Delay	Reset Rd Disc Delay (RDD)
RDD4	Reset Read Condition
Ungaged VRC	R/W Register VRC Error
Read LRCR Error	Error Line
Error	Turn on TAU Error Tgr
Bksp or Rewind	Busy
Sel and Ready	Read Only Trigger
	Initiate Read Delay
	Write Trigger
	Initiate Write Delay
	Write TM
	Erase
	Backspace
	Turn On Rewind Trigger
	Turn On Rewind Unload Tgr

TAU 2 INTERRUPTS	
Name	Function
Oscillator	Read Clock Drive and Sample
Write Condition	Wr Clock Drive and Sample
WC1	Reset R/W Register
Micro-Sec Pulse	Delay Counter Drive Pulse
	Write Clock Pulse
Milli-Sec Pulse	Delay Counter Drive Pulse
TR Reset	Reset Odd Redundancy Tgr
R/W Reg Error VRC	R/W Reg Error Tgr
	TAU Error Tgr
Read LRCR Error	TAU Error Tgr

FIGURE 2.2-3. TAU INTERRUPTS

NO INTERRUPT



INTERRUPT

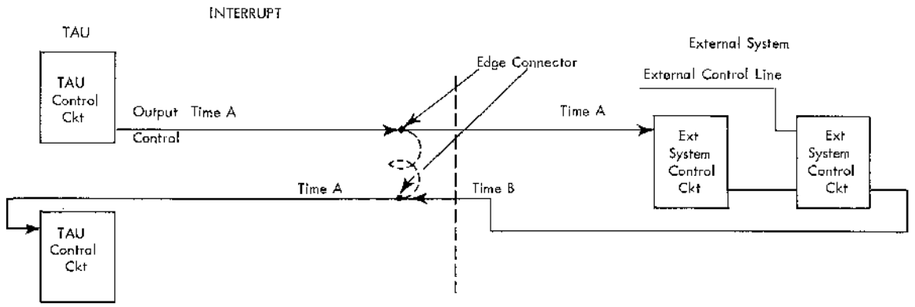


FIGURE 2.2-4. INTERRUPT LOGIC

3.0.00 FUNCTIONAL UNITS

3.1.00 FINAL AMPLIFIER

Each of the seven final amplifiers is fed from the 7-bit read bus channel from the tape unit. The inputs to the amplifiers are peak amplitude sensed. The final amplifiers have two outputs, a high level and a low level. Seven high and seven low output signals are developed for input to the read registers.

3.1.01 Amplifier Description

The basic TAU final amplifier consists of three SMS cards. Each card serves a specific function in the operation between the input read bus and the output pulse used to set the read registers.

Two more cards are added to each of the basic amplifiers to make the second channel of the dual channel system.

The first card (AFC) is used to perform the five functions listed below.

1. Amplify the input signal 2.2 to 2.4 times (transformer).
2. Provide two signals 180^{O} out of phase (transformer).
3. Impress a DC bias to provide a noise clipping level (transformer plus external control cards).
4. Rectify out-of-phase signals to provide in-phase signals (first transistor stage - emitter followers).
5. Provide two outputs, one of which is impressed with additional noise clipping (high and low clipping channels).

The normal read signal input is eight volts peak-to-peak and all acceptance level percentages are based on this figure. The sine wave frequency range for proper operation is 7.5kc to 32kc. This range of frequencies is designed to provide maximum reliability for operating 729 II and 729 IV Tape Units.

The noise clipping applied to the first card is provided by three external cards which can be varied over a wide range of values. The clipping value is switched between read and write operations to the values shown below.

Clipping Level (-12v Reference)				
Write		Read		
-2.4v	B	- .6v	B	
+1.2v	A	+2.2v	A	Additional clipping provided to channel A
+2.4v		+0.6v		+ inverse channel B clipping voltage
+3.6v	A	+2.8v	A	Effective clipping for channel A

The output of the first card is the half wave of the input amplified twice.

The second card (FC) provides two functions for the final amplifier system:
Differentiation and clamping
Amplification and integration

The time constant of the differentiation is selected to provide a flat response over the frequency range mentioned. After differentiation, the negative portion of the signal is clamped out. The positive portion is amplified about 20 times and integrated in the emitter follower output stage. This provides a signal output that has a fall time coincident with the input peak and, as such, is an effective peak senser. The integration provides a sharp cut-off to frequencies above the band pass to protect the system from noise.

The third card (FD) provides two functions:

DC sensing
Pulse generation

The input circuit to this card is essentially a Schmidt trigger. The input signal will charge the integrator of the previous card from -12 volts towards -6 volts. When the signal rises to about -10 volts, the trigger will turn on. Because the rise of the integrator is slow and the fall fast, the time difference between the input peak and the fall of the trigger is more consistent. It is for this reason that the fall of the input signal is used to form the output pulse. The pulse is generated in an LC timing network and has a duration of about 0.6 usec.

3.1.02 Clipping Level Description

Four cards are used to establish the various clipping levels used in TAU.

The basic card (WU--) affects the clipping level of both the A and B channels. This circuit contains a voltage divider and a transistor switch which can be activated, when required, to alter the divider output. As presently used, the switch is turned on when TAU is in "not write status." This results in less clipping voltage at the output.

A second card (ABP-) is connected in parallel with the basic card to further control the clipping voltage. The card has a number of output voltage possibilities and can be switched independently of the basic clipping card.

Because the two cards previously explained affect both channels equally, a second set of cards is necessary to control the relationship between the A and B channels.

These cards (ABQ- and ABR-) impress a positive bias on the output of the AFC-amplifier card in order to produce additional clipping on the A channel when the B channel is operating at a very high sensitivity. As in the case of the previous cards, these cards are switched when not in write status.

3.2.00 REGISTERS

3.2.01 Read Registers

TAU has two read registers; one, read register A, is set from the high level output signals from the final amplifier, and the other, read register B, is set from the low level output signals from the final amplifier. Each read register contains seven triggers, one for each bit of the 7-bit code. Because of skew on the tape, the character bits remain in the read registers for a length of time determined by the read clock cycle. This is done to insure that all the bits of a particular character have been received by TAU, before the character is placed in the R-W register. The length of time the character bits are allowed to remain in the read registers is a little less than half of the normal character time interval. If the full character is not in the read registers by this time, an error is indicated in the read cycle.

In a normal read, the character in either read register A or read register B is gated to the R-W register. If the character in read register A is correct (no vertical redundancy error) it is sent to the R-W register; however, if the character in read register A is not correct (read register A vertical redundancy error), the character in read register B is unconditionally sent to the R-W register. When the R-W register is set, the LRCR is also set. The operation is the same for a read check during writing operation, except that the character is sent only to the LRCR and not to the R-W register.

3.2.02 Read-Write Register (R-W)

The R-W register is a group of seven triggers, one for each bit of the 7-bit code. All data passing between the external system and a tape unit pass through the R-W register. The R-W register is the swinging door through which the data are allowed to flow either way. During writing, the input data lines are set into the R-W register, and the register output is the data output of TAU to the tape unit. During reading, the R-W register is set from the read register and the R-W register output is again the output of TAU, only this time to the external system.

3.3.00 ERROR CHECKING

3.3.01 Vertical Redundancy Checker (VRC)

The outputs of read register A and the R-W register feed VRC's. Both VRC's are conditioned by an odd redundancy trigger that can be turned on and off by the external system. The VRC's are a combination of plus and minus OR circuits that determine the vertical bit structure of a character. The output of the VRC is an error line. By use of the odd redundancy trigger, the VRC error line can be conditioned to be active for either odd or even redundancies.

Figure 3.3-1 shows the VRC circuit used in TAU. The inputs to the checker are the seven bit lines of the 7-bit code and the odd redundancy conditioning line. The bits are compared in pairs for even or odd outputs. The results of two group comparisons are then compared in pairs for even or odd outputs, to give two final groups which are also compared for the odd-even result. The final result of the last comparison is the output of the VRC.

Figure 3.3-2 shows the second-level logic of the TAU VRC. The labels above the input lines show the condition of the lines when the input is active. The names below the line represent the condition of the line when the input is inactive. The outputs of the AND blocks are considered odd if only one of the inputs is present, and even if none or both of the inputs are present. The status (plus or minus) is the level of the line when the given condition is present. The odd redundancy input is used to condition the C bit input to check for either the odd or even redundancy check.

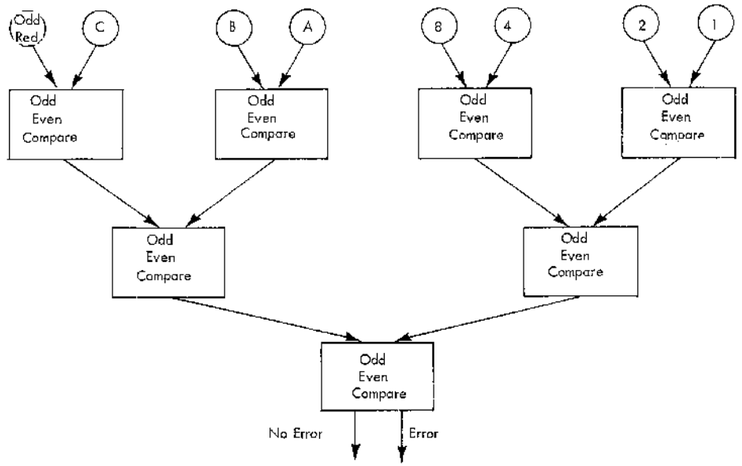


FIGURE 3.3-1. VERTICAL REDUNDANCY CHECKER LOGIC

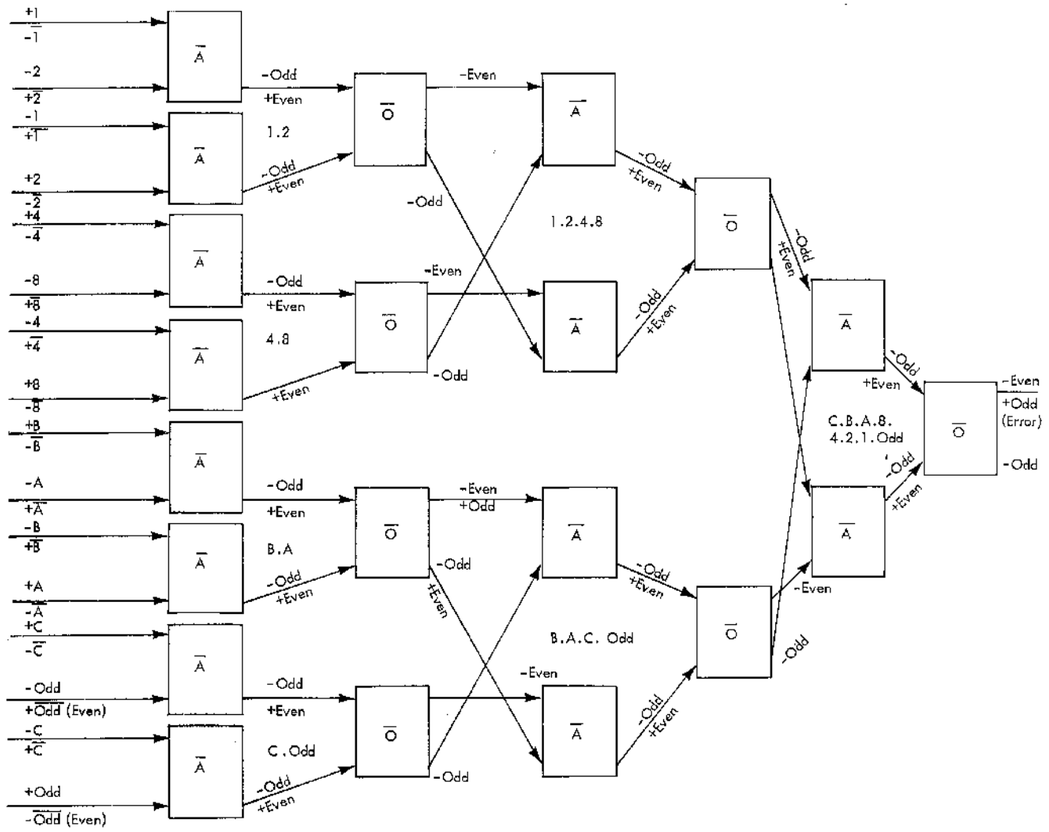


FIGURE 3.3-2. VERTICAL REDUNDANCY CHECKER (VRC)

3.3.02 Longitudinal Redundancy Check Register (LRCR)

The LRCR is a group of seven triggers, one for each bit of the 7-bit code. All the triggers are binary triggers. At the start of any read operation all triggers are off. As character bits are set into the LRCR, each trigger being set will be turned on with the first bit, off with the second, on again with the third, and so on throughout the record. Since a record, when written, is always made even when the check character is written, the LRCR, after setting to the check character, should finish with all triggers off (even count). If this is the case, no error is indicated. However, if any trigger is on after the check character sets, the active trigger output will indicate an LRCR error.

Figure 3.3-3 illustrates the LRCR action with a simple record, on tape, as shown at the upper left. When the record is read, each character is checked for a VRC error as well as the LRCR error. All bits have an even count both vertically and horizontally. The action is noted in the sequence chart below the tape. In the A track, as an example, the first A bit read will turn on the A trigger in the LRCR. The second bit read will turn the trigger off, the third A bit will turn the trigger on, and so on through the record. At the end of the record the trigger in the LRCR will contain an odd or even count of each bit track just read. When the check character is read, any triggers which were on will be turned off.

The dotted circles note the bits which are dropped to indicate an LRCR error. Two bits are shown being dropped to indicate that the character is still even vertically and a VRC will not occur. The dotted lines represent the error condition in the sequence chart. Notice that when the LRCR sample is active the B and A triggers are on and an error will occur. If only one bit had failed to read, the record would indicate a VRC as well as the LRCR. With only one bit dropped, the second character would have an odd bit count causing the VRC error. The LRCR would still show an error because the bit track in which the bit was dropped would have an odd horizontal count.

The logic diagram at the right of Figure 3.3-3 shows the LRCR register and the sample. If any trigger has an output when the register is sampled, the A circuit will have an output to turn an error trigger on. The LRCR is always sampled well after the check character is read, to insure that all characters have been entered.

3.3.03 Echo Error

In each write cycle, a no-echo trigger is turned on before sending a write pulse to the tape unit. When any writing takes place on the tape unit (from a TAU generated write pulse), the active write circuits develop an echo pulse and send them to TAU. Any echo pulse received by TAU resets the no-echo trigger. Late in the write cycle the status of the no-echo trigger is sampled. If the no-echo trigger is on, the TAU error trigger and a no-echo error trigger will be turned on. If the trigger is off (echo return), no error will be indicated.

3.3.04 Write Compare

In every read during a write operation, read register A and read register B are compared with each other. Any uneven comparison will indicate an error by turning on the TAU error trigger. The compare circuit is a group of -AND circuits conditioned by the outputs of both registers. By allowing the read circuits to become active earlier than normal, a compare check is used to detect inter-record gap noise.

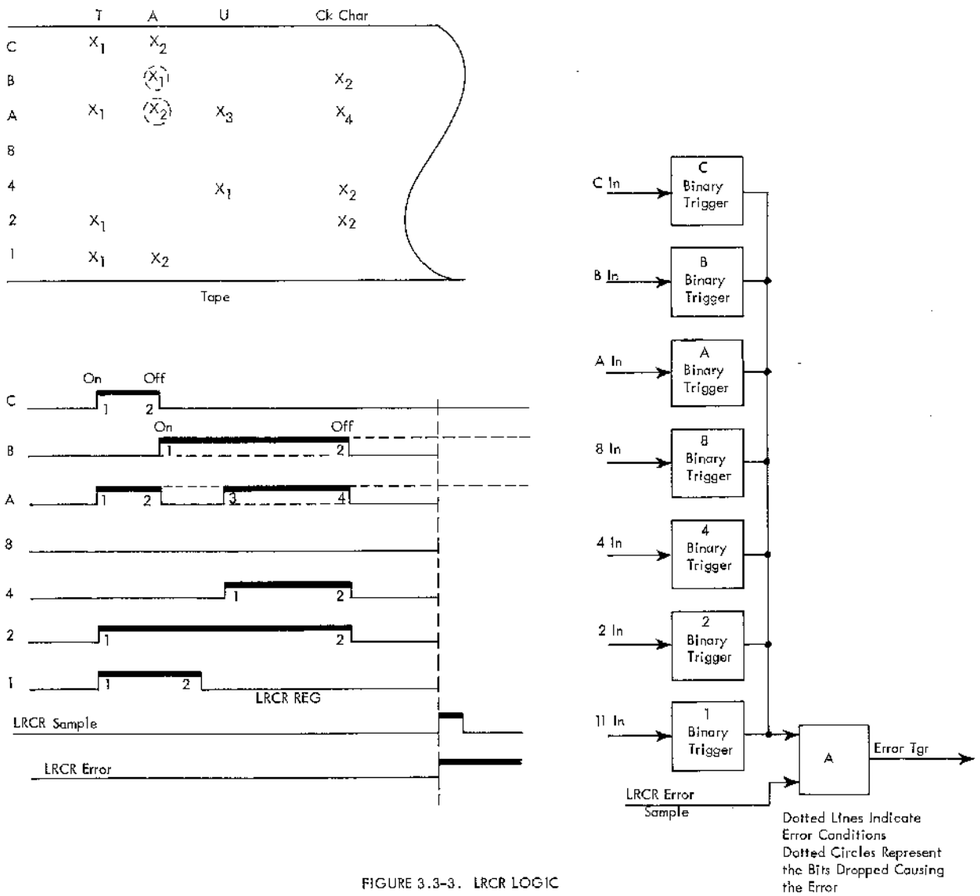


FIGURE 3.3-3. LRCR LOGIC

3.3.05 Skew Error

As a check against any excessive speed variation of tape movement between the write and read heads, a skew error circuit is used. A momentary slow-down of the moving tape at the time of writing will cause the written characters to be spaced closer together. If the tape is traveling at normal speed when the characters are read, a skew error will result. The momentary slowing down of the moving tape arises if the tape driving mechanism should momentarily slip or bind. During this period when tape is traveling at a slower rate, less tape is passing under the write head. With the write pulse frequency remaining constant, the magnetized areas on the tape become closer together. The spacing of the characters on tape is a function of the tape speed and writing frequency. When the tape unit is back at its normal speed, the closer spaced characters will have a smaller time interval between them. The reading circuits were designed to accept characters at the normal time interval. If any characters appear earlier than the normal time interval, the skew error circuit will become active.

Figure 3.3-4 illustrates the action. In graph A is a typical tape envelope (ignoring start time). The tape speed is constant until T5 time, where the slowing down takes place. At T9 time the tape is traveling at its normal speed.

Graph B is the speed line. Speed is a function of distance traveled, divided by the time. Any point on the graph up to T5 shows the distance tape travels with respect to time and is directly proportional. The ratio is a constant denoting that the tape is travelling at a constant speed. From T5 to T9, however, is the slowing down point. The graph illustrates that, for a given time, the distance travelled is much less at the T5 to T9 time. If characters are written at timed intervals and plotted on the graph, the character spacing would be as illustrated on the right end of the graph.

Chart C shows the error circuit action when these characters are read. Only characters 4, 5, and 6 are shown in the sequence chart. When the first character is sensed, a read clock cycle is started. A portion of the read clock cycle is allotted to allow time for all bits of a character to be read. At the completion of this time the character is placed in the R-W register. Also, at this time, a skew gate trigger is turned on to check for the error condition. Since characters 4 and 5 are spaced correctly apart, a skew error is not indicated. However, characters 5 and 6 are spaced closer than normal. Character 6 will be read when the skew gate is active and turn on the skew error and TAU error triggers. Character 6 was written when the tape had slowed down and the condition has been noted by the skew error condition. Characters 6, 7, and 8 are shown packed together. This is referred to as bit or character packing.

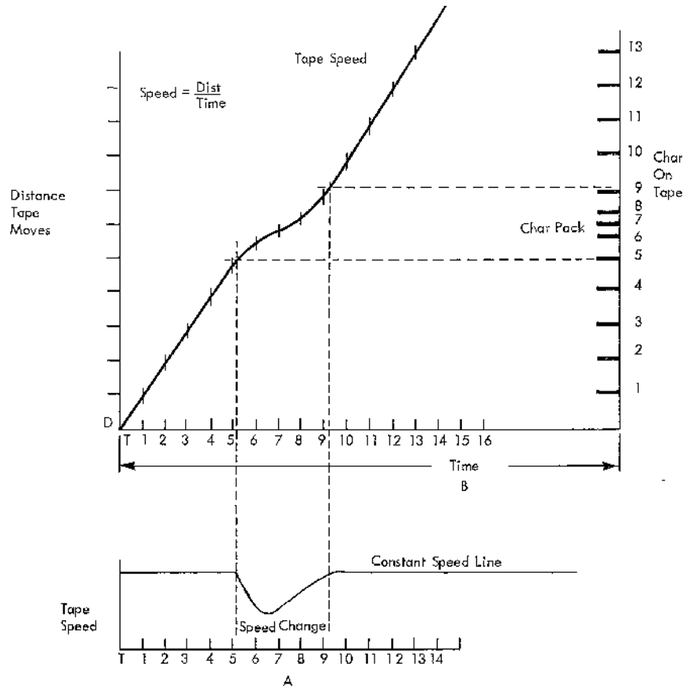
This circuit is active only when a momentary slow-down of tape occurs. There must be an excessive speed change in tape movement between the write head and the read head.

3.4.00 CLOCKS AND COUNTER

3.4.01 Read Clock

The read clock in TAU consists of four binary triggers separated by a 400 nanosecond delay line. The high-low density line and the selected tape unit (II or IV) determines one of four oscillators used to obtain the drive pulses. The oscillator output is fed to a 400 nanosecond* single shot where the drive pulses are developed. The

* One nanosecond equals one milli micro-second.



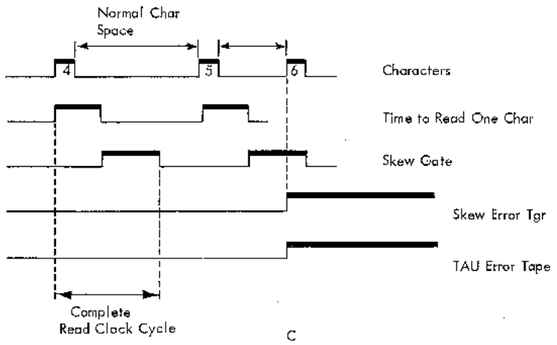


FIGURE 3.3-4. CHARACTER PACKING

400 nanosecond drive pulses feed all four triggers in parallel. Because of the 400 nanosecond delay between each clock trigger, the only trigger conditioned when the drive pulse arrives will be the only one set. The previous trigger will be reset by the same pulse. When any one trigger is set, the next trigger in the ring is conditioned after the 400 nanosecond delay. By this time, the drive pulse has disappeared and another drive pulse is necessary to set the next trigger. By this method, then, the first drive pulse will turn on the RC1 trigger, the second drive pulse will reset RC1 and turn on RC2, the third will turn RC1 back on (RC1 and RC2 both on will give RC3 time), the fourth drive pulse will reset both RC1 and RC2 and turn on RC4, and so on through the read clock cycle. At the completion of each read clock cycle all triggers are reset off.

The oscillator used to drive the clock is normally clamped off until reading is to begin. Because there is no way of knowing just when characters will start being sent from tape, the read clock cycle is not started until the arrival of the first bit of each character read. By starting the read clock with the first bit line, a timing relationship for each character of a record can be realized. The read clock will run through one complete cycle for each character of a record.

The length of the read clock cycle is dependent upon the type of read operation to be performed. The normal read clock cycle is shorter than that of a read check operation. In a normal read operation the clock will run from RC1 time to RC7 time. One output of the RC7 timing circuit is fed through a 400 nanosecond delay line and is then used to trigger a 1000 nanosecond (1 usec) single shot used to reset the read clock triggers. A read check operation runs from RC1 through RC11 time. The extra time required on a read check operation is used as a further check of the data just read.

In a read check operation the read clock timings are slightly different than a normal read. Specifically, RC7 time is actually RC5 time. A write operation control line conditions the RC7 timing circuit to allow an output with the RC1 and RC4 triggers. The reason for this timing change is an added marginal check for the record being read. Also, the RC7 reset line is actually at RC11 time. Again a write operation control line conditions the circuit to obtain the added time.

It is extremely important to realize these variations because the system line names are not so labeled. The RC7 and RC7 reset lines are labeled in the system, but, as mentioned, during a write operation the RC7 time is RC5 and the RC7 reset time is actually RC11. The clock operation otherwise is the same as in a normal read. The RC7 reset line (RC11 when writing) flips a 1000 nanosecond (1 usec) single shot to reset all the read clock triggers at the completion of the read clock cycle.

3.4.02 Write Clock

The write clock consists of four binary triggers separated by a 400 nanosecond delay line. The triggers are driven in parallel by a 400 nanosecond timing pulse derived from a crystal oscillator. A control trigger (write condition) comes on early in a write operation and gates oscillator pulses to the clock. The clock operates in a binary fashion similar to the read clock (1 on, 2 on, 1 and 2 on, and so on). After the fifteenth drive pulse the WC1, 2, 4, and 8 triggers will be on. The sixteenth drive pulse resets all the triggers to normal, and one cycle is complete. Since write condition is still on, the oscillator continues driving the clock and another write cycle is started. As long as

write condition is on, the clock remains in repetitive cycles. The WC8 trigger also conditions the oscillator drive pulses to insure that the write clock will complete its cycle when write condition goes off.

3.4.03 Delay Counter

The delay counter consists of nine binary triggers. The DC1 trigger is driven directly from the selected oscillator, forming the drive timing pulse and sample pulse. The next four triggers are driven in parallel by a 400 nanosecond timing pulse, while the next four are driven in series by the output of the previous trigger.

The drive pulses to the clock are conditioned from a speed control circuit. This circuit has either a millisecond control output or a microsecond control output. Since the operation of the counter is so varied, each operation needing the delay counter outputs has a control trigger to start the delay counter at the proper time and in the proper mode. Whenever an operation using the delay counter is complete, the control trigger resets the counter in preparation for the next operation.

The frequency of the drive pulses to the counter is determined by either 729 II or IV operation and the high-low density status.

4.0.00 INTERNAL OPERATIONS

4.0.01 Figure References

Flow Diagrams

To clarify TAU operation, flow diagrams have been included for write, read, read check, backspace, and rewind. The flow diagrams show the word sequence of the way TAU performs an operation, and in no way show how the operations have been performed. With TAU operating correctly, the flow charts tell the sequence of events TAU uses in completing an operation from beginning to end. The diagrams use a 3-block notation. The oval block is used at the beginning to indicate the operation to be performed. It is also used at the end when the operation is complete. The rectangles indicate the event TAU is performing. The diamond blocks are decision blocks with the outputs labeled. The write-up that follows in this section has a brief explanation of each block of the flow diagram.

Block Diagrams

Included for read, write, error while writing, and backspace are block diagrams for each of the operations. The block diagrams represent all the necessary timings, conditions, and writing lines TAU uses to perform the operation.

Sequence Charts

A timing sequence chart is also included for read, write, backspace and error conditions while writing. The sequence chart shows the timing relationships for existing conditions of an operation during the operating cycle.

4.1.00 BASIC TAU OPERATIONS

4.1.01 Write Operation

To initiate a write operation, the external system must generate a write call and send it to the TAU. The TAU directly controls all tape movement, develops the write pulses, and controls the data flow from the system through TAU to the tape. The complete write operation of TAU is shown in Figures 4.1-1 through 4.1-5. Following is a brief explanation of each block of the flow diagram.

Write Call

This call is a request signal generated within the external system and sent to the TAU to start the operation.

Busy

If the TAU were performing another operation at the time of the request signal, the busy line would be active and prevent the write call from performing its function. If the TAU were idle, however, the write call signal would initiate action in TAU.

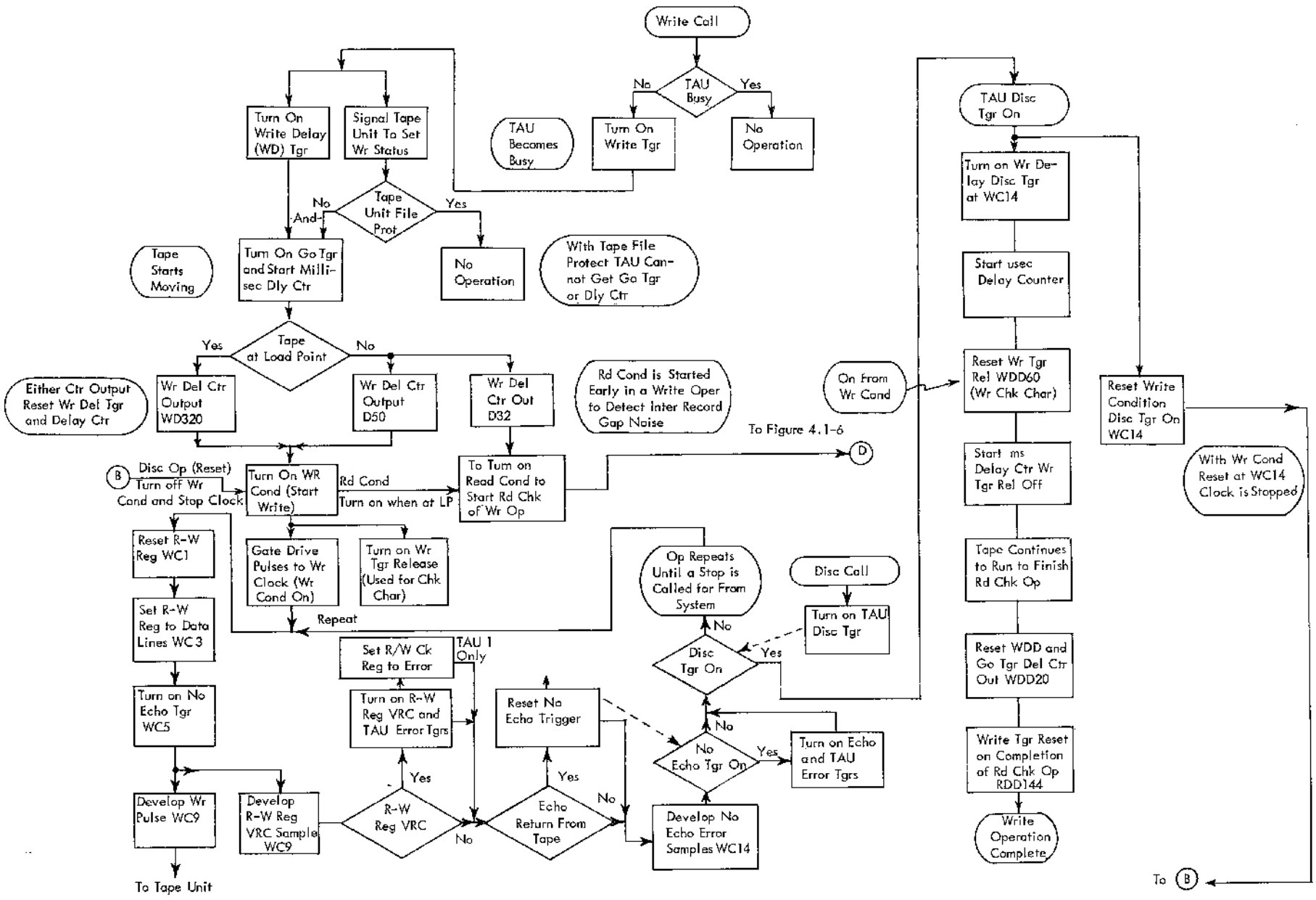


FIGURE 4.1-1. WRITE OPERATION

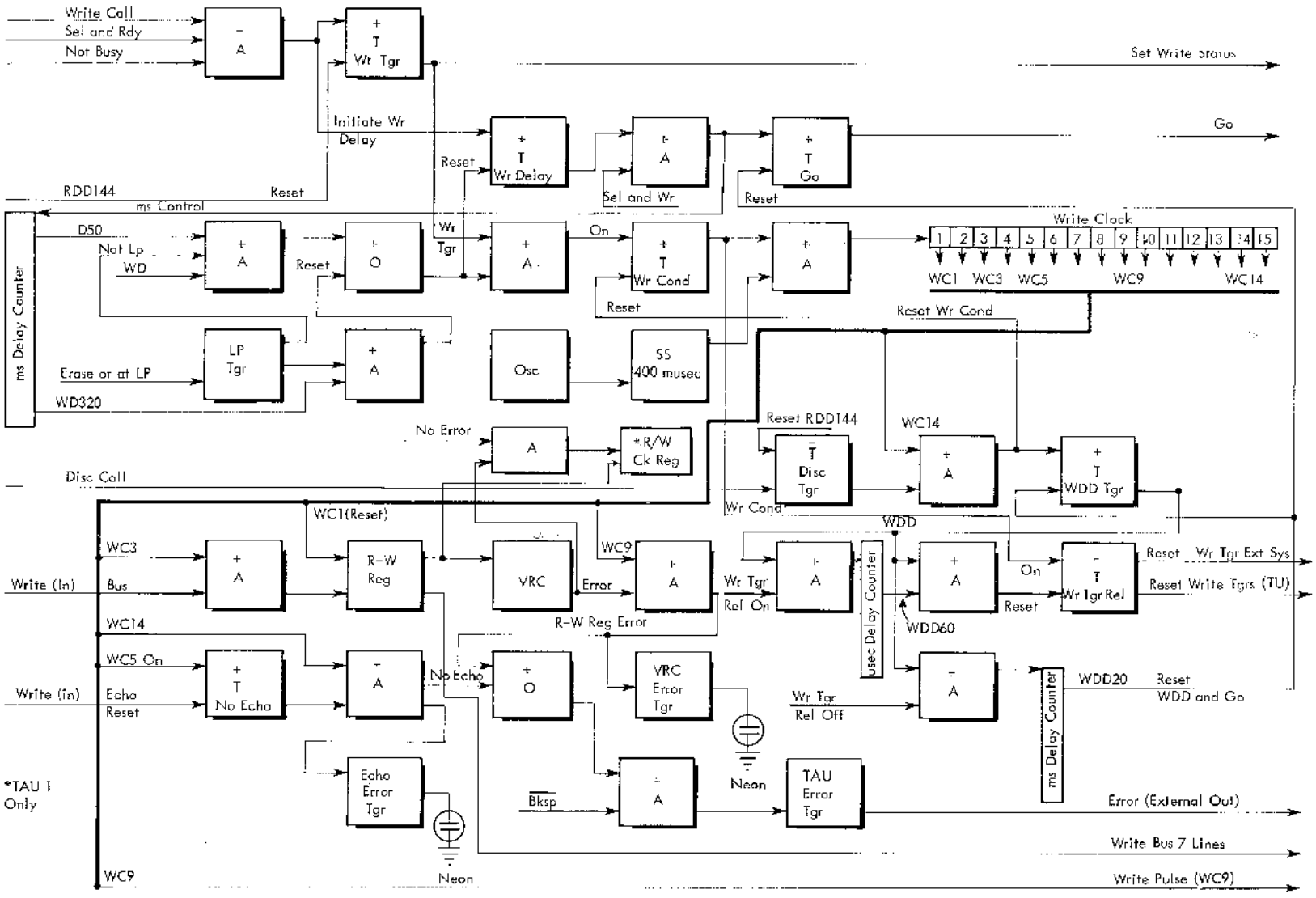


FIGURE 4.1-2. TAU WRITE OPERATION LOGIC

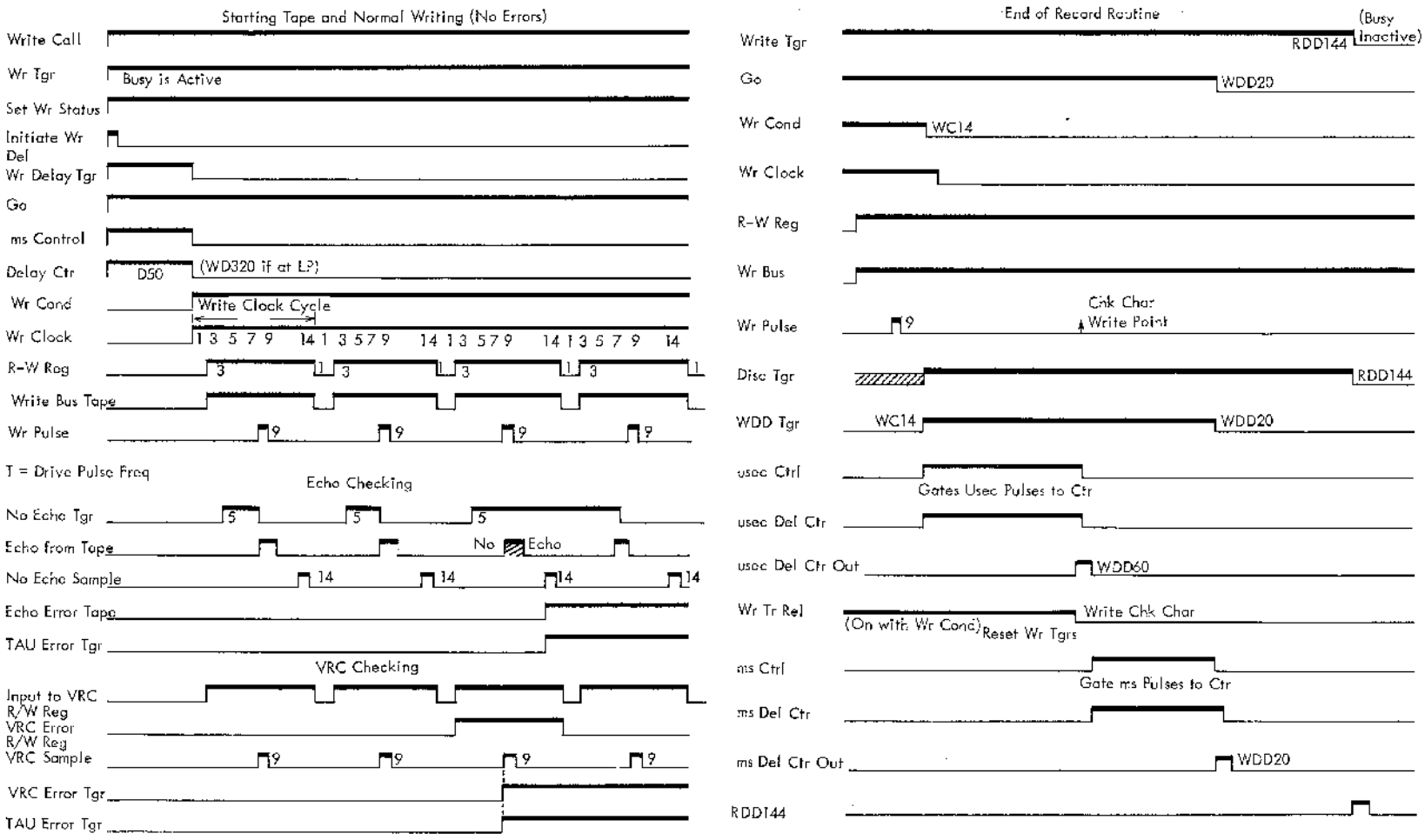


FIGURE 4.1-3. TAU WRITE OPERATION

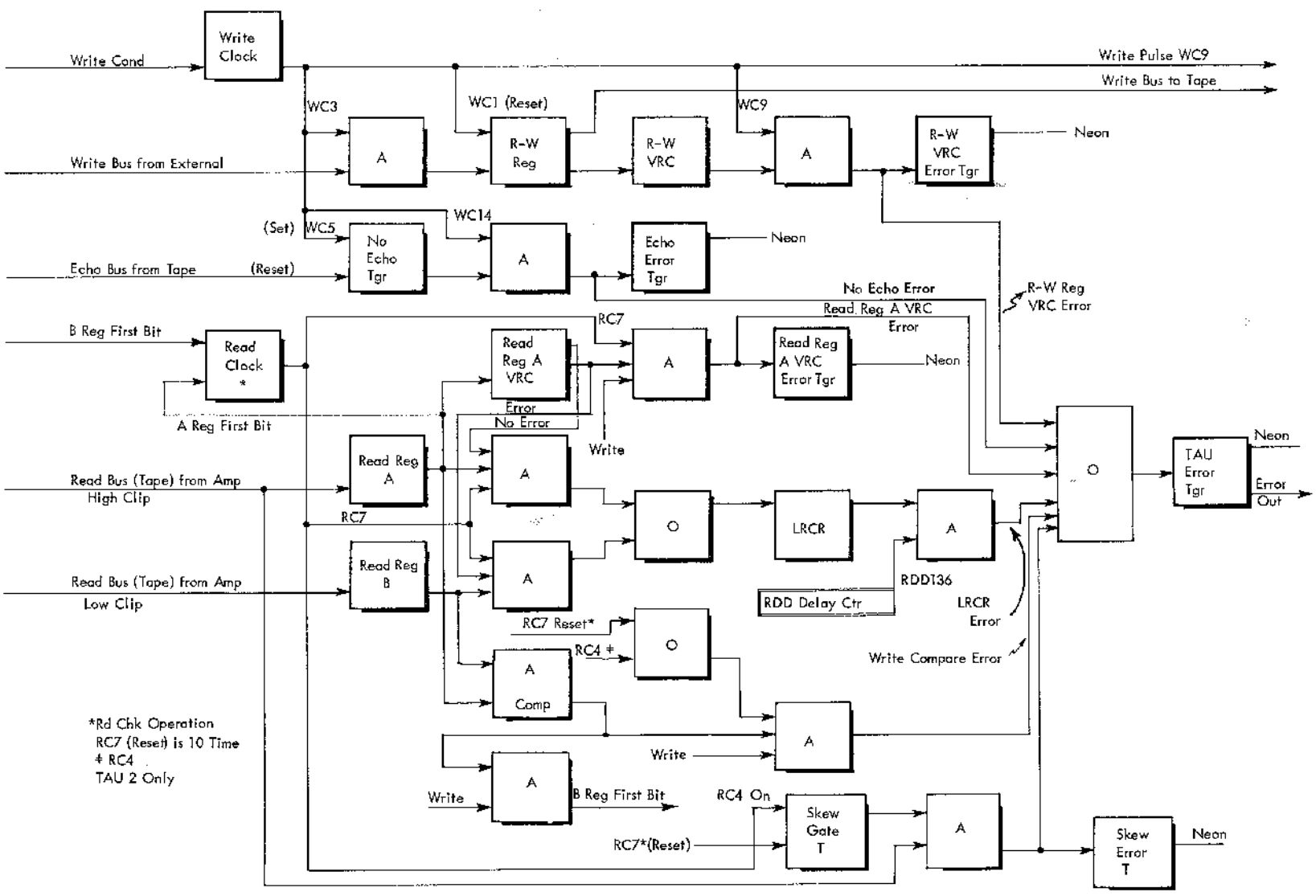


FIGURE 4.1-4. ERROR CONDITIONS WHEN WRITING

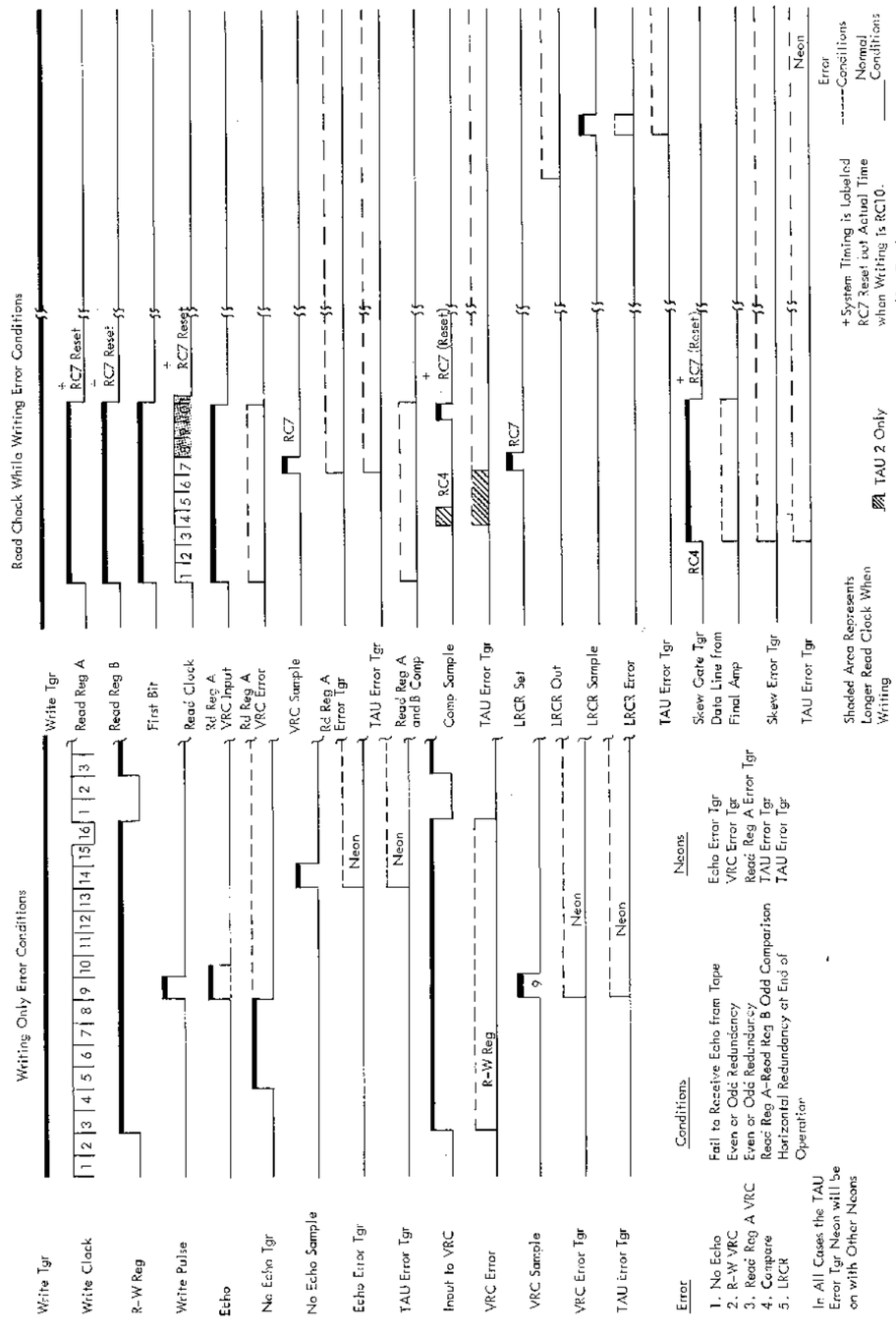


FIGURE 4.1-5. ERRORS DURING WRITING

Write Trigger

The write call signal turns on the write trigger in TAU. With the write trigger on, the busy line becomes active and prevents another operation until writing is complete. The write trigger signals the tape unit to set the unit in write status.

Write Delay Trigger (WD)

At the same time the write trigger is turned on, the write delay trigger is also turned on. The write delay trigger controls the starting of the tape and the necessary time delay before the actual writing circuits become active.

Tape Unit File Protected

If the tape unit is in a file protect status, the set write signal from TAU is blocked. TAU is dependent on write status signal from the tape unit. If the tape unit cannot go to write status, the TAU operation is blocked and no operation will result. If the tape unit is not in file protection the set write status signal from TAU sets the tape unit in write status. The tape unit then returns the signal "sel and write" to TAU.

Go Trigger

With the write delay trigger on and "sel and write status" active from the tape unit, the go trigger in TAU is turned on. The go trigger output is sent to the tape unit and initiates tape movement.

Millisecond Delay Counter

With the tape unit in write status, the write delay trigger starts the delay counter. The write delay trigger conditions the counter for millisecond control and the counter starts stepping. The counter drive pulses are determined by the oscillator, selected by either 729 II or IV operation. The reason for the delay is to allow the tape to reach its proper speed before initiating the active write circuits.

Load Point

If the tape unit is at load point when it is selected, the load point trigger in TAU will be on. The load point trigger conditions the write delay counter output.

Delay Counter Output

If the load point trigger is off, the delay counter WD32 pulse will turn on write condition. If the load point trigger is on, the delay counter must count to WD320 before an output is available to turn on write condition. The added delay, if at load point, is necessary to insure that the load point reflective spot is well beyond the R-W head before writing is allowed to take place. In either case the tape is up to speed before write condition is turned on. The same delay pulse used to turn on write condition also resets the write delay trigger and the delay counter.

Write Condition

This trigger is turned on upon completion of the write delay. Write condition has the direct control of the actual writing by controlling the write clock. The flow of data

through TAU and the timing relationships for control are originated with the write clock. Write condition allows oscillator drive pulses to start stepping the clock. As long as write condition remains on, the write clock will be in repetitive cycles. When write condition comes on, the write trigger release trigger is turned on. This trigger is used at the end of the write operation to write the check character.

Read Condition

If the tape unit is at load point, read condition is turned on at the completion of the write load point delay. If the tape unit is not at load point, read condition is turned on when the delay counter reaches D32, which is before the write delay timing. Read condition is turned on in order to read the information as a check of the write operation. The early turn-on allows the read circuits to become active soon enough to detect possible inter-record gap noise.

Write Clock

This clock produces basic timing pulses for actual writing. The actual timing of the pulses is listed in Figure 2.1-1. All clock outputs are listed with a WC designation; for example, WC1 time, WC5 time, and so on.

Reset R-W Register

At WC1 time of any write clock cycle, the R-W register is reset. This clears out the last character in the R-W register in preparation for setting it to the input data lines for a new character.

Set R-W Register

At WC3 time of the write clock cycle, the input data lines are sampled. All lines that are active are set into corresponding triggers in the R-W register with the WC3 pulse. With data in the R-W register, the output lines to the tape are active.

No Echo Trigger

Unconditionally, at every WC5 time, a no echo trigger is turned on. This trigger is sampled later in the write cycle as an echo check for writing.

Write Pulse

Powered from the clock at WC9 time, the write pulse is sent to the tape unit to initiate the writing action. Since the data lines are already active to the tape (output of R-W register), the arrival of the write pulse causes the character to be written.

R-W Register VRC Sample

Also at WC9 time the R-W register output is sampled for a vertical redundancy check. Whenever data appear in the R-W register, its output, besides being available on the output tape bus, is also sent through a VRC. Depending upon the type of vertical redundancy check called for (odd or even), the VRC error line will be active from the wrong type bit structure. At WC9 time the VRC error line is sampled.

R-W Register VRC

If the VRC error line is active at WC9 time, the R-W register VRC error trigger will be turned on. This trigger gives only a neon indication of the error. In addition to the R-W register VRC trigger being turned on, the TAU error trigger is turned on. The output of the TAU error trigger is available to the external system and is TAU's only method of indicating any write or read error.

In TAU 1, the first error character is placed in a R-W check register. The output of the check register is fed to indicator when the bit structure of the error character is displayed.

Echo

When writing action takes place in the tape unit, the write circuits develop an echo pulse. The echo pulse is immediately sent to TAU. When any echo is received from the tape unit, the no echo trigger is reset. Note: It takes only one echo from the tape to reset the no echo trigger. If the write circuits in the tape unit are not activated for any bits, no echos are develped and the no echo trigger remains on. This check insures that something was written, but does not indicate what.

No Echo Error Sample

At WC14 time, the no echo trigger output is sampled. If the no echo trigger is off, no action takes place. However, if the no echo trigger is on (no echoes from tape), an echo error trigger and the TAU error trigger will be turned on with the WC14 pulse. The echo error trigger is a neon indicating trigger only. The TAU error trigger output is the only error indication to the external system.

Disconnect (Disc) Trigger On

This trigger is turned on by a request from external system control to end the operation. If an end-of-write operation is not requested with disc call, the write operation continues to repeat. The next clock pulse WC1 resets the R-W register and so on through the complete write cycle again.

The write operation continues until the information from the external system is written. To end the write operation, the system must generate a disc call signal and send it to TAU. This signal arrives sometime during the last write character cycle. Upon receiving the disc call, TAU writes a check character, stops the tape, and provides the necessary resets for the write circuits. The disc operation is shown in Figure 4.1-1.

Disc Call

This call is a signal generated within the external system control to end the write operation.

Disc Trigger

This trigger is turned on when the disc call line to TAU is activated.

Disc Trigger On

If the disc trigger is on when the write clock output is at WC14, the write delay disc trigger is turned on (Figure 4.1-1).

Write Delay Disc (WDD)

This trigger is the controlling trigger in TAU that initiates the end-of-write operation. It is turned on at WC14 time of the last character cycle when the TAU disc trigger is on.

Reset Write Condition

Write condition is reset at WC14 also if the WDD trigger is on. When write condition goes off, it blocks further oscillator drive pulses to the write clock. The clock stops with all triggers off.

Microsecond Delay Counter

The WDD trigger starts the delay counter by initiating microsecond control. The oscillator drive pulses are determined by 729 II or IV operation. Figures 2.1-1 and 2.1-2 show the drive pulse for each type operation. The delay counter, while in the microsecond mode, gives the necessary time delay and then causes the check character to be written.

Reset Write Trigger Release

When the delay counter output is WDD60 (refer to Figures 2.1-1 and 2.1-2 for timing), the write trigger release is reset, causing "reset wr trigger" to reset the write triggers in the tape unit. When the write triggers in the tape unit are reset, a check character will be written. All write triggers that were on write a bit when they are reset. The WDD60 pulse also resets the delay counter.

Millisecond Delay Counter

With the WDD trigger on, the write trigger release trigger going off causes millisecond control to condition the delay counter. The delay counter now begins stepping in a millisecond mode. (Refer to Figures 2.1-1 and 2.1-2 for timings.) This delay conditions the tape unit to stop at the proper time and perform the necessary write circuit resets.

Reset WDD and Go Triggers

When the delay counter output reaches WDD20, the go trigger, the WDD trigger, and the delay counter are reset. Because the tape is still reading after the writing has finished (physical location of 2-gap head), the tape is allowed to run to complete the read check. This is the reason for the WDD20 delay. When the go trigger is reset after the delay, the tape starts to stop, but there is still the normal mechanical stop delay which further insures the time necessary to complete the read check operation.

Reset Write Trigger

The complete write operation is not completed until all operations, including the read check, are finished (Figure 4.1-7C). Since the read portion of the write operation is the last to finish, the write trigger remains on to keep the TAU in a busy status. At the completion of the read checking operation, the write trigger is reset and "busy" becomes inactive. The write operation is complete.

Figure 4.1-6 shows a sample tape record with representative timings for both tape units at both densities. All character timings are figured by using the formula $T = 1/F$ where T is time and F the oscillator frequencies. The oscillator timings are figured to three decimal places.

4.1.02 Read Operation

To initiate a read operation, the external system must generate a read call signal and send it to the TAU. The TAU controls all tape movements and controls the flow of data from tape through the TAU to the external system. In all operations performed during a read operation, TAU performs necessary checks for error conditions. The diagrams for reading are Figures 4.1-7, 4.1-8, and 4.1-9. Included in these flow diagrams is the read check during a write operation. Since a normal read and a read check during a write operation are similar in many instances, both have been included. Any deviation from a normal read is represented by a decision block labeled "read check of write operation." The outputs of the decision blocks are correspondingly labeled to cover the individual cases. During a read check operation the RC7 line is actually at 5 time. The RC7 reset line is actually at 11.5 time. Refer to Section 3.4.01. A brief explanation follows.

Read Call

This call is a request signal generated within the external system and used to start the read operation.

Busy

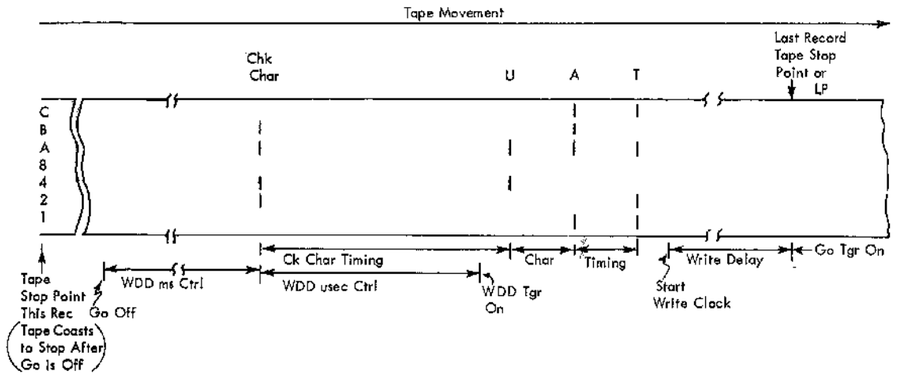
If TAU were performing another operation at the time of receiving the read call, the busy line would be active and prevent any operation on the read call signal until the other operation is completed. If "busy" were inactive, the read call signal would initiate action in TAU.

Read Only Trigger

The read only trigger is turned on with the read call signal. The output of the read only trigger activates the busy line, which prevents any other operation until reading is complete. The read only trigger output is also sent to the tape unit where read status is set. When the tape unit is in read status, it returns "sel and rd" to TAU.

Read Delay Trigger (RD)

At the same time that the read only trigger is turned on, the read delay (RD) trigger is also turned on. The RD trigger controls the starting of tape and necessary delay before the actual reading circuits become active.



	729 II Lo		729 II Hi		729 IV Lo		729 IV Hi	
Write Delay	LP 48ms	Not LP 7.5ms	LP 48ms	Not LP 7.5ms	LP 32ms	Not LP 5ms	LP 32ms	Not LP 5ms
End of Write Delay to 1st Char	37.49usec		13.5usec		24.99usec		9.us usec	
Char Timing	66.6usec		24usec		44.4usec		16us usec	
Ck Char Timing	270.8usec		97.5usec		179.9usec		65us usec	
WDD usec Ctrl	250usec		90usec		166usec		60us usec	
WDD Ms Ctrl	3ms		3ms		2ms		2ms	
Ck Char to Go Off	3ms		3ms		2ms		2ms	
Lst Chr to Wdd WDD Turn On	20.8usec		7.5usec		13.9usec		5usec	
On Complete WC Cycle (WC1-WC1)	66.66usec		24usec		44.43usec		16usec	

FIGURE 4.1-6. PHYSICAL TIMING RELATIONSHIPS

Go Trigger

With the RD trigger on and "sel and rd" active from the tape unit, the go trigger in TAU is turned on. The output of the go trigger is sent to the tape unit and starts the tape moving.

Millisecond Delay Counter

At the same time the go trigger is turned on, the read delay trigger starts the delay counter. The RD trigger conditions the counter for millisecond control and the counter starts stepping. The counter drive pulses are determined by the oscillator, selected by either 729 II or IV operation (Figures 2.1-1 and 2.1-2). The necessary delay is to allow the tape to reach its proper speed before the actual reading circuits become conditioned.

Load Point

If the tape unit is at load point when it is selected, the load point trigger in the TAU is turned on. The load point trigger conditions the delay counter output.

Delay Counter Output

If the load point trigger is off when the read operation is started, the RD44 output turns on the read condition trigger. If the load point trigger is on at the start of the read operation, the read condition trigger cannot be turned on at RD44, but must wait for the RD160 output of the delay counter. The reason for the longer delay, if at load point, is to insure that the load point reflective spot is away from the R-W head before reading begins. Notice that the delays taken for a read operation are shorter than those of a write operation. The shorter delays when reading are to insure that the read circuits become active soon enough to read the first bit of the written record. If the read and write delays were the same, there will be the chance that the first character when reading might be missed.

Read Condition

Normal Read. This trigger is turned on when the read delay operation is complete. With read condition on, the actual read circuits are conditioned for operation.

Read Check During Writing. If at load point this trigger is turned on by the same pulse that turns on write condition. If not at load point, the trigger is turned on with a DC32 pulse (write condition turned on with D50). The early turn-on when in read check is to detect inter-record gap noise by conditioning the read circuits earlier than normal. Read condition in this case is limited to its function of conditioning the read circuits.

Gate Final Amplifiers

Read condition activates a read gate line which conditions the final amplifier in TAU. With the read gate conditioning the final amplifier, any data appearing on the input data bus from the tape unit will be amplified and routed to the read registers.

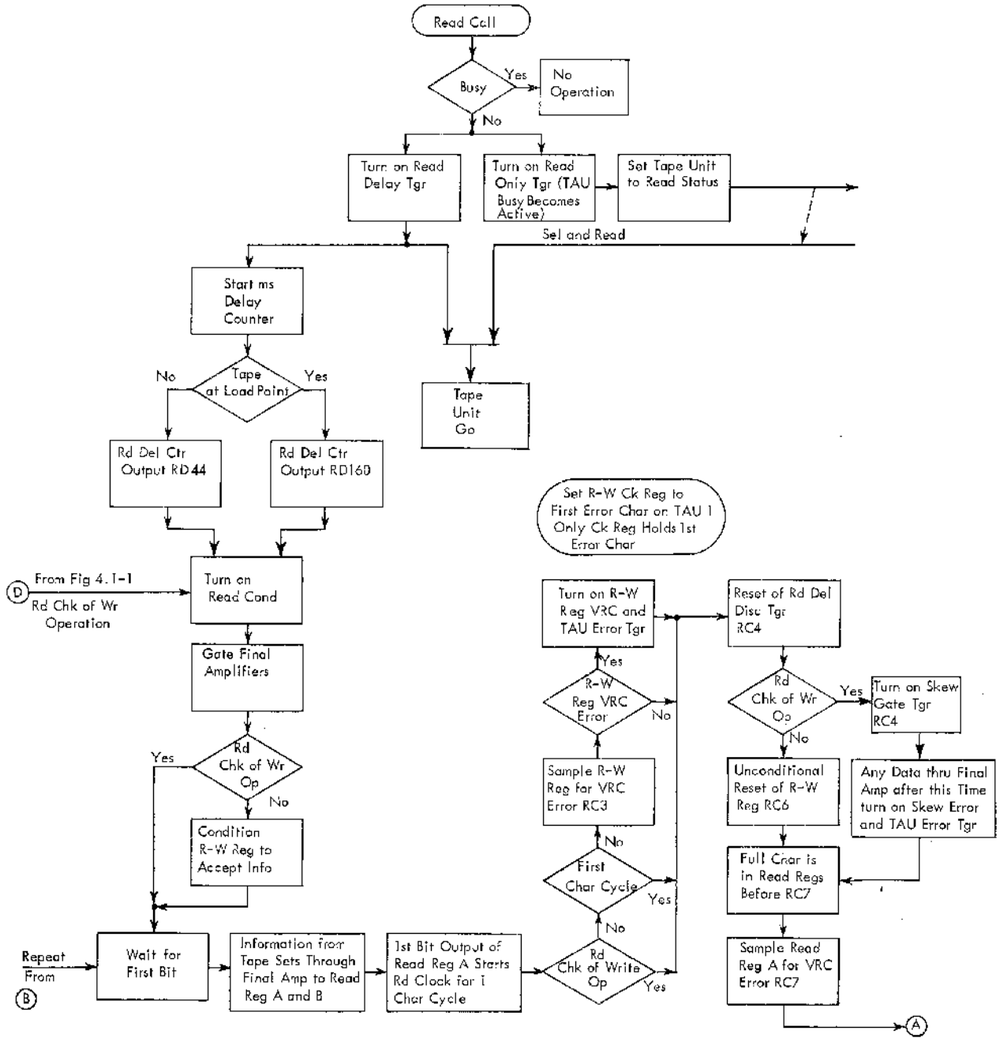
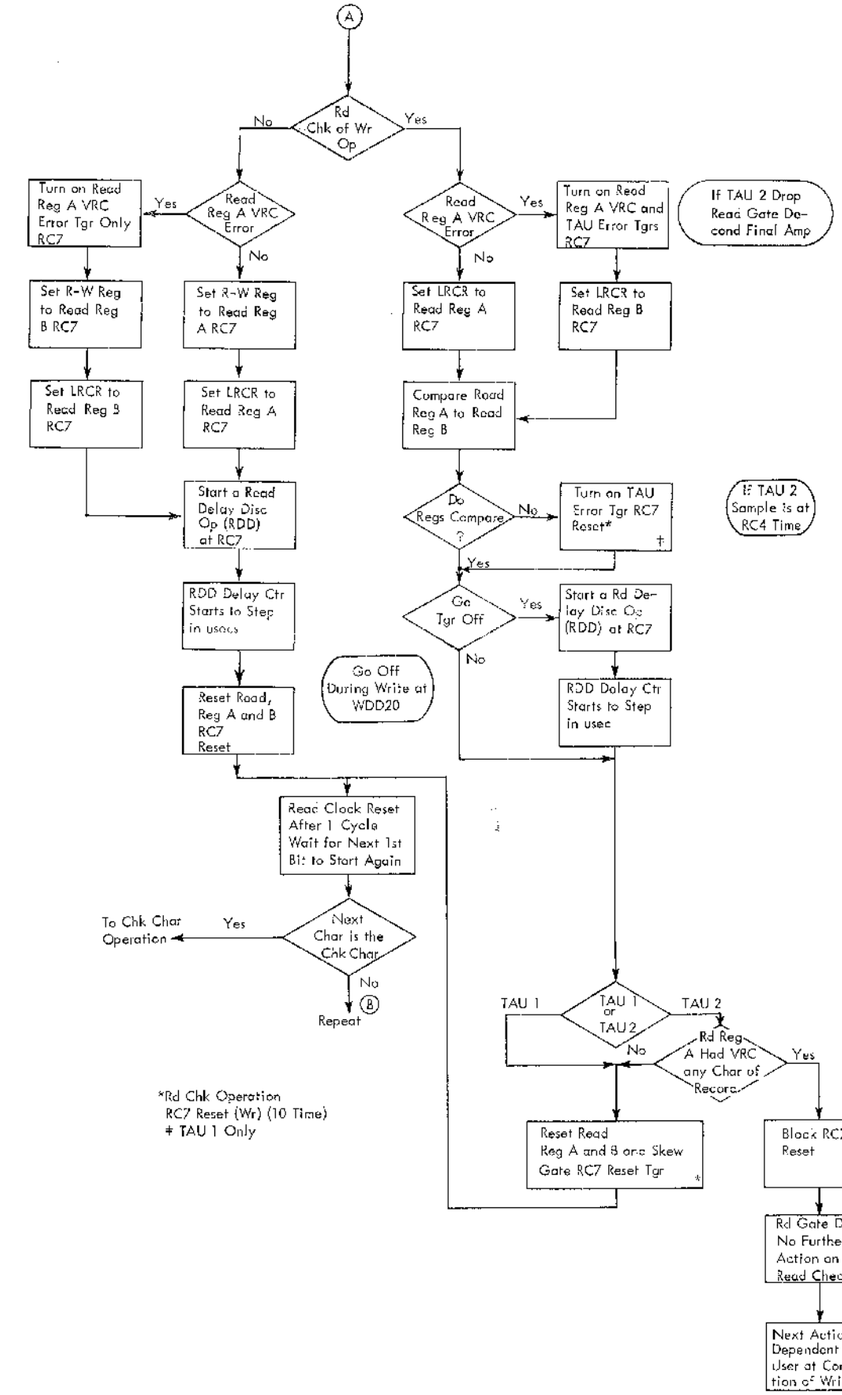
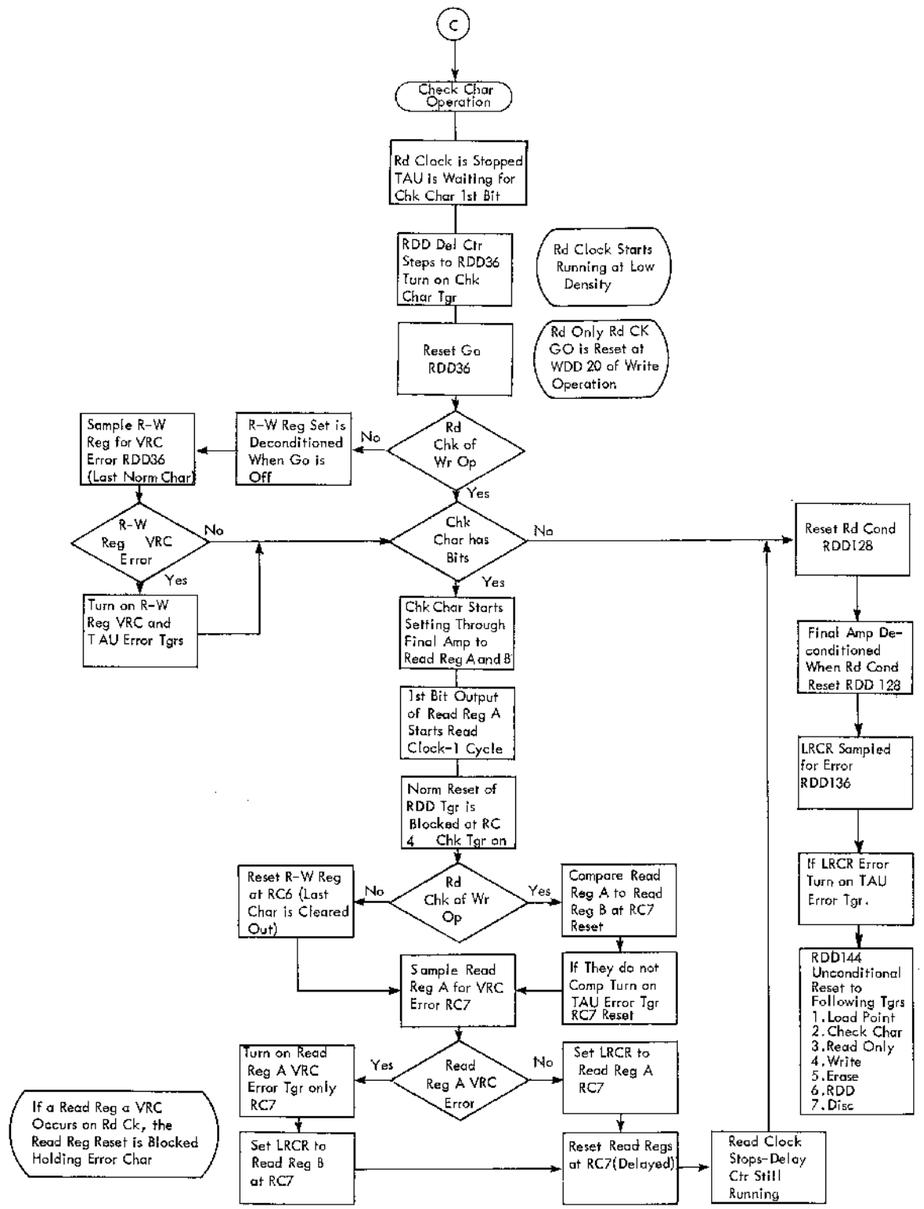


FIGURE 4.1-7A. READ AND READ CHECK OPERATION



*Rd Chk Operation
RC7 Reset (Wr) (10 Time)
TAU 1 Only

FIGURE 4.1-7B. READ AND READ CHECKING OPERATION



*Rd CK Operation Only. RC7 Reset is 10 Time

FIGURE 4.1-7C. READ AND READ CHECK OPERATION

Condition R-W Register

Normal Read. In a normal read operation, read condition, the read only trigger, and go condition the inputs to the R-W register. Since TAU must make the tape data available to the system, the R-W register must be set to these data.

Read Check During Writing. In a read check operation, the data being read from tape need only to be checked within TAU. In this operation the only data appearing in the R-W register are the data that are being written on tape. These written data are read by the read head and sent to TAU for various checks, and are not gated to the R-W register.

Wait for First Bit

Because of variable starting times between tape units and the shorter read delay, TAU does not know at exactly what time the first character will be read. Once the first bit of a character is read, a timing relationship for that character is established. TAU performs no operations until the first bit of a character is read.

Set Read Registers A and B

Whenever the read head reads data from the tape, the information is sent from the tape to the final amplifier in the TAU. The final amplifier has two outputs, a high level and a low level. The high level output sets to read register A and the low level output sets to read register B.

First Bit

As soon as any trigger in read register A is set, a first bit line becomes active. The first bit line unclamps the read clock oscillator and allows the read clock to start stepping. A read clock cycle is started.

Sample R-W Register for Vertical Redundancy

Normal Read. In a normal read operation, the R-W register is the data output to the system. The character that is being sent to the system is checked for a vertical redundancy error while in the R-W register at RC3 time of the read clock cycle. The character being checked is the character that was processed through the TAU in the previous read clock cycle. The first character of a record is not in the R-W register at RC3 time of the first clock cycle; therefore, no check is made of the R-W register at this time. During the second read clock cycle, the first character read is in the R-W register and is checked. The second character read is checked in the third read clock cycle and so on through the record. The last normal character of the record is checked during the check character processing cycles. Since the check character never appears in the R-W register, no vertical redundancy check is necessary.

Read Check During Writing. The read clock does not sample the R-W register when reading during a write operation. The data read in this operation never appears in the R-W register. The R-W register in the read during writing operation contains the data to be written on tape. The R-W register is sampled from a write clock pulse.

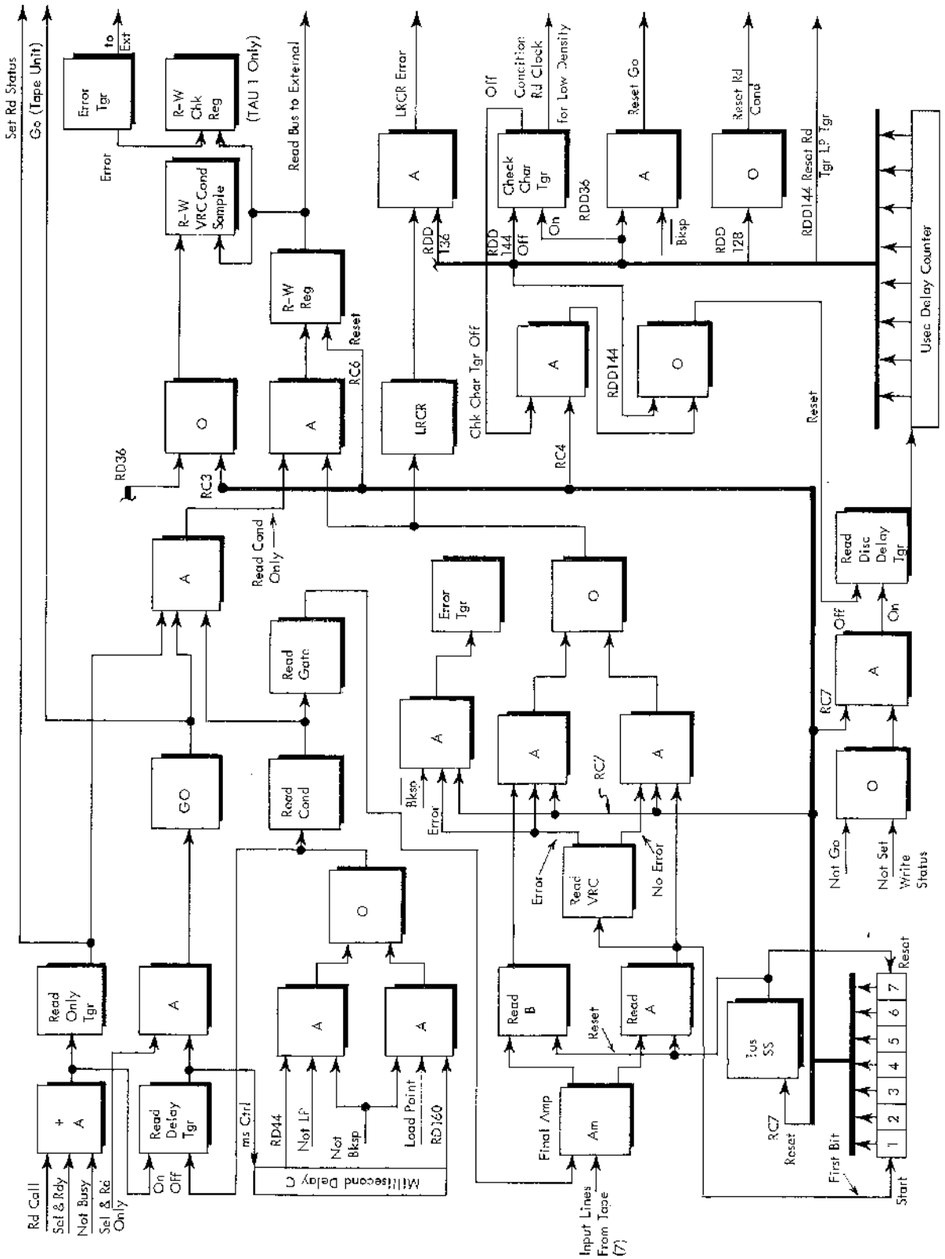


FIGURE 4.1-8. READ OPERATION LOGIC

R-W Register Vertical Redundancy Error

If, in a normal read operation, the R-W register VRC line is active at RC3 time, the R-W register VRC error trigger and the TAU error trigger will be turned on. The R-W VRC error trigger is for neon indication only, while the TAU error trigger is available to the system.

Reset of Read Delay Disc Trigger (RDD)

Each time the read clock runs (except check character) an unconditional reset is applied to the read delay disc trigger at RC4 time. This trigger is used to control the read end operation and is always turned on at the end of every normal read character cycle. Normally, the trigger is not on long enough to start the end operation because it is reset at each character time interval with the RC4 pulse. The only time the trigger is not reset in the timed interval is when the check character is the next character. In this case the check character time is much longer than normal character time intervals, and the RDD trigger remains on long enough to start the end operation.

Reset R-W Register

Normal Read. In every normal read cycle the R-W register is reset with the RC6 pulse from the read clock. The reset clears out the data from the previous cycle, so the character now in the read registers can be set into the R-W register.

Read Check During Write. Since the R-W register is used only for the writing operation, the reset from the read clock is blocked during this operation.

Read Registers

By this time read registers A and C have had the full character set into them. Before the character can be available to the system, it must first be set into the R-W register.

Read Register A VRC

Normal Read. At RC7 time of the read clock cycle, read register A is sampled for a vertical redundancy error. The outputs of the register are immediately available to a VRC. By RC7 time the full character is set into the register and the VRC will have determined if the bit structure of the character is correct (odd or even depending upon the type of check called for). If the character is redundant, the read register A error line is active. At RC7 time, the line is sampled, and if an error is indicated, the read register A VRC error trigger will be turned on. In this case the TAU error trigger is not turned on. The only indication of a read register A VRC is the neon indicating read register A error trigger. The read register A error line is used to gate either read register A (no error) or read register B (error) to the R-W register and an LRCR.

Read Check During Writing. Because this is a read check of information that was just written, the TAU error trigger is also turned on by a read register A vertical redundancy error. The read register A VRC error trigger is also on, giving a neon indication in TAU of the error. The read register A VRC error line is also used in this operation to gate either read register A (no error) or read register B (error) to an LRCR register. The data in the read registers are not set into the R-W register when doing a read during a write operation. In a read check operation the read register VRC is also sampled at RC7.

Read Check. The skew gate trigger is turned on at RC4 during a read check operation. Any data appearing through the final amplifier after this time are gated by the skew gate trigger to turn on the skew error and TAU error triggers. This check is necessary to check for any excessive speed variations between the write and read head on the tape unit (Refer to Section 3.3.05). The skew gate trigger is reset with the RC7 reset line (10 time) of the read clock cycle. The time allotted to check for the skew error, then, is from RC4 to RC7 reset (10 time).

Read Delay Disconnect (RDD)

Normal Read. At RC7 time of every normal read operation a read delay disc trigger is turned on. The RDD trigger controls the end of the read operation. With a RDD trigger on, the delay counter starts stepping in microseconds. If the delay counter counts to the RDD36 output, the operation is set to terminate. Normally, the RDD trigger is reset with the RC4 pulse from the next character cycle, and never reaches the RDD36 point because the timing of the individual characters being read is less than the time to count to RDD36. The delay counter can only reach RDD36 when the next character is the check character, because the check character timing is longer than the RDD36 time. Because of this longer check character timing, the read clock does not start until later and the RC4 pulse arrives too late to reset the RDD trigger. In this case TAU recognizes the next operation as a check character operation, and sets up delays to process the check character and stop the read operation.

Read Check During Writing. The RDD trigger is not turned on at RC7 time of the read clock cycle. As long as writing is being performed, the RDD turn on is blocked (go trigger and write status). When writing is complete and the go trigger is off, the RDD trigger is turned on with an RC7 line at RC7 time of the last read clock cycle. Since writing is complete, the only operation then is to complete reading the record. In this case the RDD trigger is turned on to control the end of the read check portion of the operation. Once the RDD trigger is on, it performs as in the normal read operation by stepping the delay counter.

Reset Read Register A and B

Normal Read. The read registers are reset in preparation for receiving the next character by an RC7 reset pulse. The RC7 reset pulse is an RC7 pulse that has been delayed 400 nanoseconds. The delay in resetting the read registers is to allow time for the transfer of data to the R-W register and LRCR, to perform the VRC and compare check.

Read Check During Writing. The reset of the read registers is delayed until 10 time on a read check operation. The delay is necessary to perform the skew error check. The reset pulse is an RC7 reset line (10 time); it also resets the skew gate trigger.

In TAU 2 operation only, the reset of the read register is blocked if read register A indicates a VRC error. By blocking the reset of the read registers, the first character in error is frozen in read register A and is identified. To prevent any following character from getting into the read register and destroying the error character, the final amplifier is deconditioned by dropping the read gate. The time between the error indication to the time the final amplifier is deconditioned is approximately 10 microseconds. If the skew conditions of the next character were such that bits were read before the

final amplifier was fully deconditioned, the read registers would be set to them, thereby destroying the bit structure of the error character. The possibility of this occurring is remote, but if the conditions were justified, it would occur. This circuit is applicable only to TAU 2.

Read Clock Stops

Normal Read. The RC7 reset pulse triggers a 1 microsecond single shot. The single shot output (1 usec pulse) resets all read clock triggers off. Another first bit is necessary to start the clock.

Read Check. The RC7 reset line (10 time) triggers the 1 microsecond reset single shot. All read clock triggers will be reset with the single shot pulse.

TAU 2 Only. If there is a VRC check in read register A, the reset is blocked. This causes the error character to be held in read register A, thereby holding up the first bit line. The read clock will continue to run as long as the character is held in the read register A.

As long as characters are being read in character spaced time intervals, the read clock cycle operation repeats with every first bit. When all characters of the record have been read, TAU starts operation for check character processing and for stopping the complete operation.

Check Character

At the end of the last read clock cycle the RDD trigger is turned on and starts the delay counter stepping in microseconds. Since the next character is the check character, the time between it and the last character read is longer than the normal character spacing. Because of this longer interval, the RDD delay counter operation counts to RDD36. At this time the check character trigger is turned on. With the check character trigger on, the reset of RDD is blocked. If the check character has bits, causing the read clock to run, the RC4 pulse does not reset the RDD trigger.

Reset Go

At the same time the check character trigger is turned on, the go trigger is also reset (RDD36). When go is off, the tape starts stopping. However, the mechanical delay in stopping allows sufficient time for the read operation to be completed.

Deconditioned R-W Register (Normal Read)

With go off, the R-W register can no longer be set from the read registers. Because the check character is not an integral part of a record, it is not sent out to the external system. However, the check character is placed in the LRCR to complete the checking operation. The R-W register is not used for reading during the read checking operation and will already be deconditioned by the write circuits.

R-W Register VRC (Normal Read)

Normally the R-W register is sampled for a vertical redundancy error with an RC3 pulse from the read clock in the next character cycle. Because this is the last character in the R-W register, TAU does not know if the read clock will run another cycle or not. If the check character has bits, the read clock runs and can sample the R-W register. However, it is possible that the check character can have no bits. In this case the read clock does not run another cycle (no first bit), and the last character is not checked. To avoid this possibility, the RDD36 pulse is used as the sample. If the R-W register VRC error line is active, the R-W register VRC error trigger and the TAU error trigger will be turned on. The TAU error trigger output is active to the system. The R-W register VRC error trigger is only a neon indication of an error in TAU.

In a read check during writing, it is not necessary to sample the R-W register as it is not used in reading.

Check Character

All that remains to be done before the read or write operation can be completed is to process the check character, check the LRCR for error, stop the tape unit, and perform resets to the read-write control circuits. The check character processing varies depending on whether the check character has bits or not. The end results are the same for either case.

As soon as the check character trigger comes on, it automatically conditions the read clock to run at low density regardless of the density it was previously reading at. The read clock is slowed down when reading the check character in order to allow a maximum amount of time to read all bits. To understand fully the necessity for this operation, first look at the character writing on the tape unit. The physical write head has a certain amount of skew which is compensated for electronically when writing. The mechanical skew of the write head is compensated for by delaying the write pulse for each bit track in the tape unit. By this method, skew is reduced to a minimum when writing. When the check character is written, however, the skew compensation is lost because the check character is not written with a write pulse but by resetting the write triggers in the tape unit. The resetting of the write triggers causes the check character bits to be written with the mechanical write head skew present. This means, then, that the skew of the check character is different than that of the normal characters whose skew was compensated for. To allow the maximum amount of time to read all bits of the check character, the read clock is slowed down to low density to insure that all bits will be read without causing an error. All read clock timings for check character operation are at low density operation.

If the check character has bits, it sets into the read registers as does any character. The first bit starts the read clock for one more cycle and the check character is treated throughout the cycle as any other character. Since the check character trigger is on, however, the reset to the RDD trigger is blocked at RC4 and the delay counter continues to run. In a normal read operation only, the R-W register is reset at RC6 time, clearing out the last character (last character of record). The check character is in the read registers by this time. At RC7 time the output of read register A is sampled for a vertical redundancy error. If the error line is active, the read register A VRC error trigger will be turned on.

With the check character in the read registers, the RC7 pulse from the clock gates either read register A or read register B into the LRCR. Read register A is gated out if there is no read register A vertical redundancy error, and read register B is gated out if read register A has a vertical redundancy error. In a read check during writing, read register A and read register B are compared. If they do not compare, the TAU error trigger is turned on.

The RC7 reset pulse resets the read registers to normal.

The RDD delay counter runs throughout the check character operation. With the RDD128 pulse from the delay counter, read condition is reset. With read condition off, the final amplifiers are deconditioned and will not accept anything through them. At RDD136 the LRCR is sampled for error. By this time the check character has been set into the LRCR and, assuming no error, all triggers should be off. If, however, one or more of the LRCR triggers are on (pick up or drop of bits), the RDD136 pulse will turn on the TAU error trigger.

When the delay counter reaches RDD144, the control circuits in TAU are reset. They are: load point trigger, check character trigger, read only trigger, write trigger, erase trigger, RDD trigger, and the disc trigger. The normal read operation or the write operation is complete.

4.1.03 Backspace

The purpose of a backspace operation is merely to get from the end of record back to the beginning of it. To initiate a backspace operation in TAU, a "backspace call" signal must be sent to the TAU from the external system. No checking is necessary during a backspace and the data being read is not sent out of TAU. A backspace operation is essentially a read operation in a backward direction. It is accomplished by reading characters into the read register to start the read clock. When the record has been backspaced over, characters are not available in the character spaced time intervals, and TAU sets up circuits to stop the operation when this condition exists. There are three possible conditions the tape unit can be in when the backspace call arrives. The tape unit can be at load point, in read status, or in write status. Each condition will be explained. Figures 4.1-10, 4.1-11, and 4.1-12 are the diagrams of the operation.

Backspace Call

This call is a request signal generated within the external system and sent to TAU to start the backspace operation.

Busy

If TAU is performing a read, write, or another operation, it will not initiate any action with the backspace call signal.

At Load Point

If the selected tape unit is at load point when the backspace call arrives, TAU will not take any action. There are no conditions where it is necessary to backspace over load point.

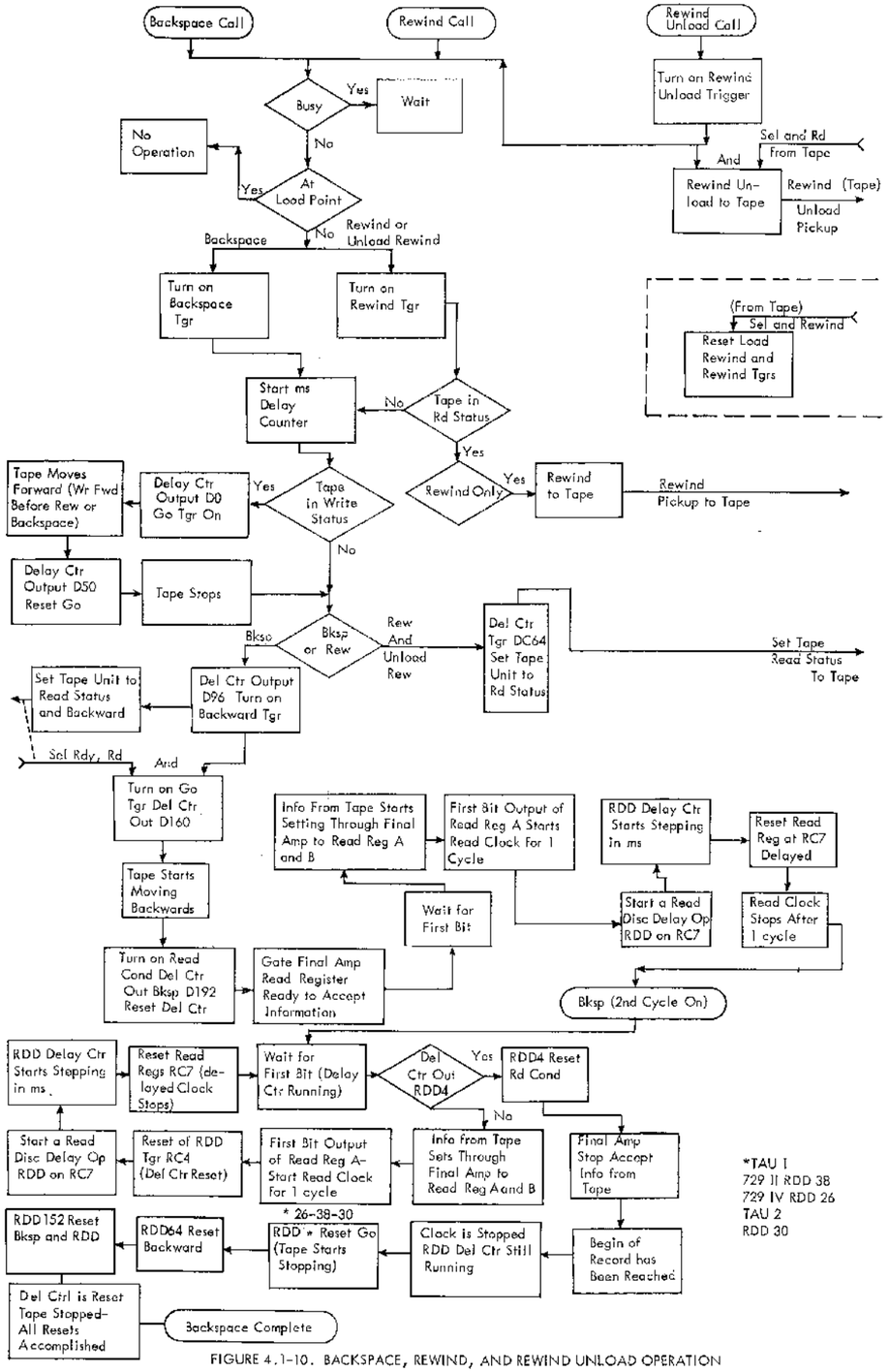


FIGURE 4.1-10. BACKSPACE, REWIND, AND REWIND UNLOAD OPERATION

Backspace Trigger

With TAU not busy and the selected tape unit not at load point, the backspace call signal turns on the backspace trigger. The backspace trigger controls the operation.

Millisecond Delay Counter

The backspace trigger conditions the delay counter to start stepping in milliseconds. The output of the delay counter conditions the start of the backspace operation.

Tape Unit in Write Status

All tape movement in a backward direction must be done with the tape unit in read status. If the tape unit is in write status, TAU must set it to read status. Because noise is deposited on the tape when changing from write to read status, the tape must first be moved forward before starting the actual backspacing. This is done to insure that noise deposited during the status change is far enough out on the tape to be erased in the next write operation. The write status line from the tape unit conditions the delay counter output for this operation.

Go Trigger On. The delay counter output D0 turns on the go trigger when write status is active.

Tape Moves. The tape starts moving forward.

Reset Go. The tape is moving forward. When the delay counter output is D50, the go trigger is reset and tape stops after the normal mechanical stop delay.

Backward Trigger

When the delay counter output is D96, the backward trigger is turned on. The output of the backward trigger sets the tape unit to read and backward status. If tape is in write status, the status change noise is now far enough out on tape to be erased in the next write operation. If the tape is in read status at the start of the operation, the tape is not moved forward first because there is not any status change noise.

Turn on Go

When the tape unit is in read status, "sel, rdy and rd" is active to TAU. With "sel, rdy and rd" active to TAU, the delay counter output D160 is allowed to turn on the go trigger. Because of the backward status, the tape starts moving backwards. The delay between backward and go is necessary to allow the mechanical transfer to backward status to take place.

Read Condition

When the delay counter output is D192, read condition turns on. With read condition on, the final amplifiers are conditioned to accept information from tape. The R-W register is not used in the backspace operation and will not be conditioned to accept data from the read registers. Read condition is delayed until D192 to allow tape to reach speed before reading.

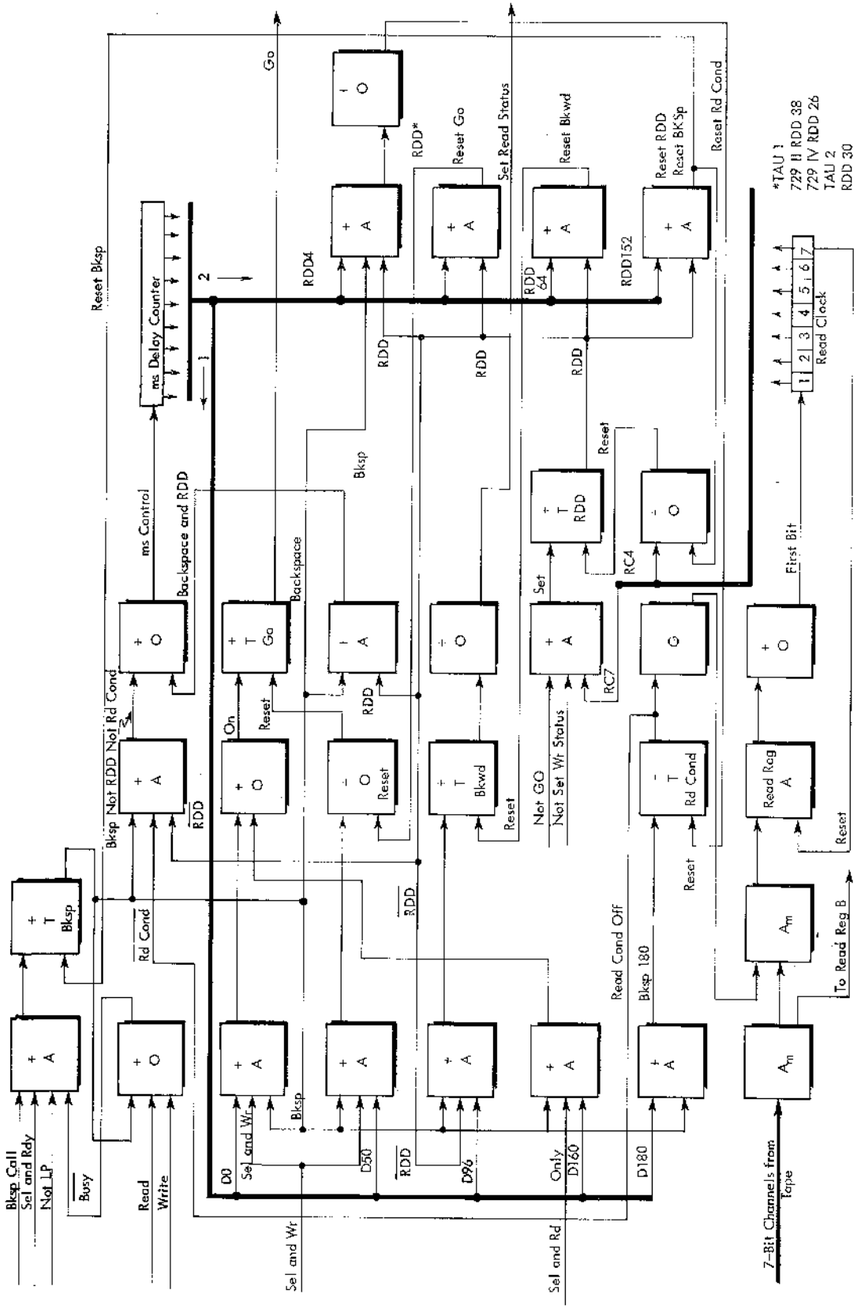


FIGURE 4.1-11. BACKSPACE LOGIC

First Character Cycle

TAU waits for the first bit. Because of backspacing over a record, the first character read is the check character. When the character is read, it starts setting into read registers A and B.

First Bit. The first bit output of read register A starts the read clock for one cycle.

Turn on RDD Trigger. When the read clock output is RC7, the RDD trigger is turned on. The RDD trigger tries to end the operation. However, as long as bits are being read at timed intervals, the RDD trigger will be reset before it can accomplish ending the backspace.

Millisecond Delay Counter. The RDD trigger conditions the delay counter to start stepping in milliseconds. The outputs of the delay counter are the pulses used to reset backspace. As long as the RDD trigger is on, the counter will step.

Reset Read Registers. The RC7 delayed pulse from the read clock resets the read registers in preparation for receiving the next character. Only read register A is used in the backspace operation. No checking is done and no data is transferred while backspacing. The whole operation is controlled by first bits from read register A. As long as first bits arrive in timed intervals, TAU recognizes that the record is still being read. When the first bit stops for a longer interval of time, the RDD delay counter resets the backspace operation. This happens only when the beginning of the record has been reached. The time from the beginning of a record to the check character of the previous record is very long. TAU recognizes this time difference and resets the backspace operation.

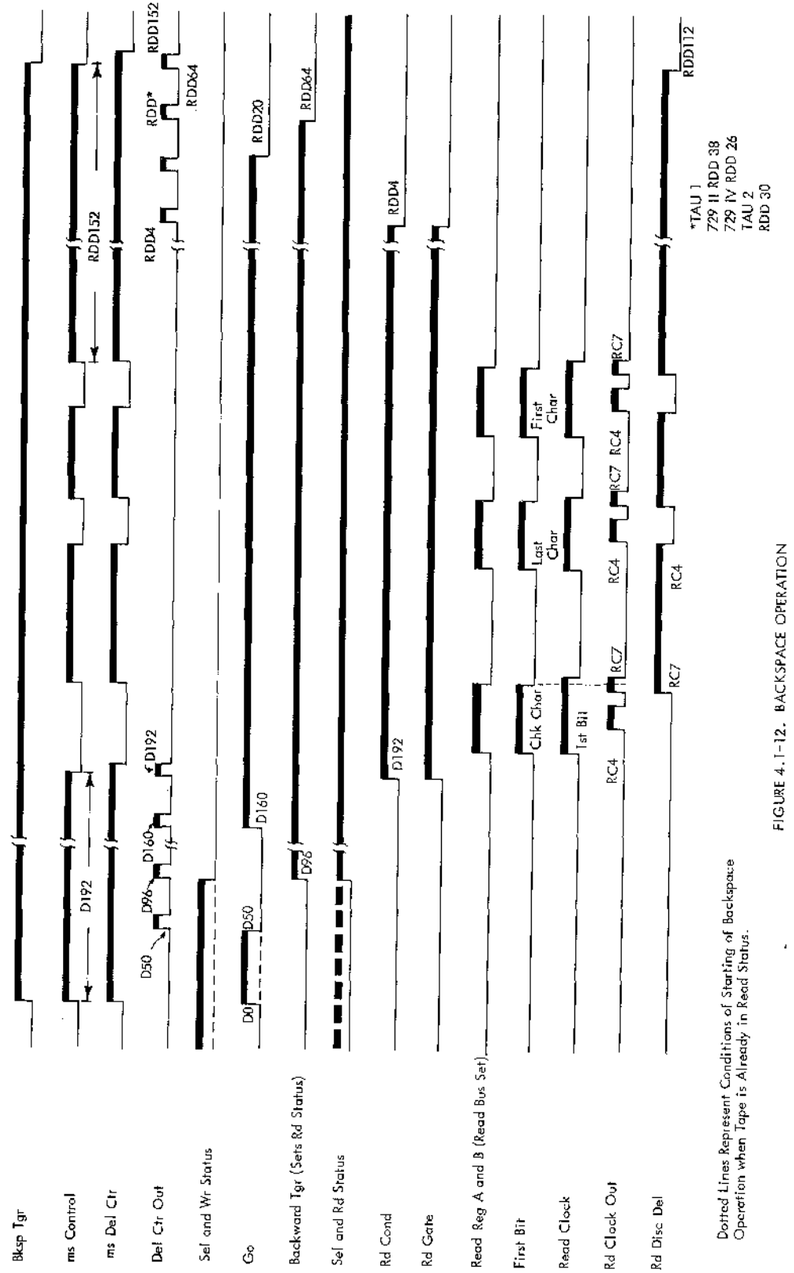
Read Clock Stops. After one cycle the read clock automatically stops. Another first bit is needed to start it for another cycle.

Second to Last Character Cycle (Figure 4.1-10)

Wait for First Bit. At the end of the first character cycle the RDD delay counter was left running. TAU is waiting for another first bit.

Delay Counter Output RDD4. If the RDD delay counter reaches RDD4, TAU resets the backspace operation. The time between characters (including the check character) in any record is always less than the time for the RDD4 output to become active, except when the last character (first character of the record) has just been read. As long as characters are being read, the first bit starts the read clock before the RDD4 pulse is available. An RC4 pulse resets the RDD trigger, which stops and resets the delay counter. An RC7 pulse turns on the RDD trigger and starts the delay counter stepping again. The RC7 delayed pulse resets the read register and then the read clock stops. TAU again is waiting for a first bit and the delay counter is running. After the last character has been read and TAU has completed the read clock cycle for that character, no first bits are available. Since the delay counter was left running, the RDD4 pulse is available to stop the operation.

Reset Read Condition. The RDD4 pulse resets read condition. With read condition off, the final amplifiers are deconditioned and nothing further can set into the read registers. TAU has recognized that the beginning of the record has been reached.



Dotted Lines Represent Conditions of Starting of Backspace Operation when Tape is Already in Read Status.

FIGURE 4.1-12. BACKSPACE OPERATION

Reset Go. The delay counter output RDD* resets the go trigger. Tape stops after the normal mechanical stop delay. Go is allowed to remain on from RDD4 to RDD* to insure that tape will stop with the write head far enough in front of the record so that the next read or write operation does not miss the first character of the record.

* Note: In TAU 1, 729 II it is RDD38; 729 IV, it is RDD26. In TAU 2 it is RDD30. The reason for the three different RDD times when resetting the Go trigger on a backspace is that these times were found to be the best within the tape unit specification. Because of space requirements in TAU 2, the RDD time was set at RDD30. This is an average between 729 II and IV tape units.

Reset Backward. The backward trigger is reset with the delay counter RDD64 pulse. When backward goes off, the tape unit is automatically set to forward status. Because of the possibility of buckling the tape when going to forward status with the tape still moving backward, the reset of the backward trigger is delayed until the tape is stopped.

Reset Backspace RDD Trigger and Delay Counter

The RDD152 pulse from the delay counter resets backspace. The reason for the delay between the reset of backward and backspace is to give time for the mechanical action of moving to forward status to take place. As long as backspace is on, "busy" is active, preventing any other operation to TAU. When backspace goes off, TAU is ready for another operation and all mechanical action in the tape unit is finished.

The RDD152 pulse also resets the RDD trigger. When the RDD trigger goes off, it resets the delay counter. All TAU control circuits are normal and the backspace is complete.

4.1.04 Tape Mark

A tape mark is a 1-character record with a check character. The tape mark consists of 1, 2, 4, and 8 bits. Because a tape mark is a 1-character record, the check character will have the same bit structure. A tape mark is normally used to indicate the end of a group of records.

Write

To write a tape mark on tape, a "write tape mark call" signal must be received by TAU. If TAU is not busy, the request signal turns on the write tape mark trigger. The write tape mark trigger turns on the write trigger and the disconnect trigger. With the write trigger on, a normal write operation is started (Figure 4.1-1). Because the disc trigger is also on, the write operation is limited to one write cycle (Figure 4.1-1). With the write tape mark trigger on, the normal input data lines are deconditioned and the write data gate to the R-W register is conditioned for the 8, 4, 2, and 1 bits. At WC1 time of the write clock the R-W register is reset, and at WC3 time the R-W register is set. Because the 8, 4, 2, and 1 lines are conditioned by the write tape mark trigger, the R-W register sets to them and a tape mark is sent to the tape unit. At WC9 time, the write pulse is sent to the tape unit and the tape mark is written. If the odd redundancy trigger is on, a C-bit will also be written with the 8, 4, 2, and 1 bits. At WC14 time the write delay disc (WDD) trigger is turned on and the operation stops in a normal manner. Because the write operation wrote only one character, the 8, 4, 2, and 1 write triggers are left on in the tape unit. When TAU resets the write triggers in the tape unit to write the check character, the 8, 4, 2, and 1 triggers will reset and

write an 8-, 4-, 2-, and 1-bit check character. The C-bit will also be written if an odd redundancy had been called for. All write check circuits are active in the normal manner. When the read check during a write operation is completed, the RDD144 pulse resets the write tape mark trigger.

Read

When a tape mark is read during a read operation, a first character tape mark line becomes active to the system. The recognition of a tape mark in TAU is conditioned by a first character trigger. Whenever read condition is turned on unconditionally, the first character trigger is turned on. At RC7 time of a normal read operation, the first character tape mark line becomes active and conditions the tape mark recognition circuit. If the character in read register A contains a tape mark at this time, the first character tape mark line becomes available to the system. At RC7 time of the read clock cycle, the first character trigger is reset, deconditioning the tape mark recognition circuit, and the first character tape mark line becomes inactive. The read operation concludes in the normal manner. If the operation is a read check during writing, the tape mark recognition circuit is not conditioned. Even though the first character trigger is turned on, the first character conditioning line to the tape mark recognition circuit is blocked by "sel and write." The only time a tape mark can be recognized by the system is during a normal read operation. The first character trigger is allowed to turn on in either a normal read or a read check during write operation. The first character trigger is useful as a good sync point during the read check during write operation, and for this reason it is allowed to turn on. The first character tape mark line is also active in a backspace operation. The backspace operation where the line is necessary is a backspace file operation. In this operation it is necessary to backspace over groups of records until a tape mark is sensed. In order to prevent the backspace file from completing as in a normal backspace, the operation must be controlled from the external system. By use of the RDD4 interrupt pulse, the system can control the backspace file operation in TAU and also condition the tape mark recognition circuit.

4.1.05 Erase

The erase trigger in TAU is turned on with an "erase call" signal from an external system. The output of the erase trigger conditions the delay counter for a longer than normal write delay by duplicating the output of the load point trigger. Regardless of where the tape is when a write operation starts, the erase trigger output forces a load point write delay. This allows TAU to skip over a section of tape before writing is allowed to begin. The erase triggeris reset with the RDD144 pulse upon completion of the read check during write operation.

4.1.06 Odd Redundancy

An "odd redundancy call" signal turns on an odd redundancy trigger in TAU. The odd redundancy trigger conditions all VRC's for odd redundancy operation by conditioning the C-bit line. The trigger also allows a C-bit to be written on a write tape mark operation. An even redundancy call resets the trigger off. In this case all VRC's are conditioned for even redundancy operation. The C-bit for a write tape mark operation is deconditioned.

4.1.07 Manual Operation

The CE panel and all manual control circuits are located in the control unit of the external system. To operate TAU 1 manually, the external control unit manually duplicates all request signals to TAU in addition to making available manual input data lines. To operate TAU 2 manually, the external system sends manual request signals to TAU 2 along with manual input data lines.

Operations

All operations in TAU operate in a normal manner except writing, which has one variation. Normally during writing, the write delay trigger and the delay counter are reset when the write delay operation is complete. When TAU is performing a manual write operation, the write delay trigger and the delay counter are prevented from being reset by the manual operations line from the external control unit. Because of this, the delay counter steps in a millisecond mode throughout the operation. The outputs of the delay counter are available to the external control unit for manual timing relationships. The disc call signal from the external control unit resets the write delay trigger and the delay counter in addition to turning on the disc trigger. With the disc trigger on, the write operation completes in a normal manner.

Manual Errors

A manual stop on error line is active from the external control unit during manual operations. If, in any manual operation, the TAU error trigger is turned on, the manual stop on error line will cause an error stop line to keep "busy" active in TAU. With "busy" active from the error condition, no further operation can be performed until the error condition is reset. A manual error reset line is available from the external control unit.

Resets

Also available from the external control unit is a "machine or power on reset" line which, when active, causes all circuits in TAU to be reset to their normal status.

4.1.08 Dual Density

TAU 1

The dual density feature of TAU 1 allows TAU to write and read either the 729 II or IV tape units at a high density rate (556 bits/inch) or a low density rate (200 bits/inch). TAU 1 contains all the circuits necessary for reading and writing at the four distinct frequencies.

To write or read at either density, the external system must send a request signal to TAU. The request signal, either "set hi density," or "set lo density," is received in TAU, powered, and sent to the tape unit. A hi lo density trigger is set in the tape unit with the request signal. The output of the density status trigger is returned to TAU as a high density line. When the line is active (+P), TAU considers it as high density, or if the line is inactive (-P), TAU considers it as low density. The status of the high density line together with the status of a "sel and rdy M2," picks one of four different oscillators for the read clock operation and one of four other oscillators for the write clock

and delay counter microsecond control operation. The timing relationships for 729 II and IV operations at either density are shown in Figures 4.2-1 and 4.2-2. Since the physical speed of the tape units remains the same, millisecond control is not changed for the dual density operation. Millisecond control is conditioned only by 729 II or IV operation.

The hi lo density trigger can also be controlled by a push button on the tape unit, giving the operator a manual control of either density operation. The density status trigger in the tape unit is always reset to high density when power is applied.

TAU 2

Each TAU 2 logically operates in the same manner for dual density operation. The only difference is that one TAU 2 is for 729 II operation and contains a different set of oscillators than the other TAU 2, which is for 729 IV operation. The following explanation includes both 729 II operation and 729 IV operation.

A request signal, either "set hi density" or "set lo density" is generated within an external system control unit and sent to TAU 2. TAU 2 powers the signal and sends it to a tape unit to set the status of a hi lo density trigger. The output of the density status trigger in the tape unit is a high density line. The high density line is returned to TAU 2 to condition the output of one of two oscillators for the read clock, and one of two oscillators for the write clock and the delay counter microsecond control. When the high density line from the tape unit is active (+P) TAU 2 considers the line as being high density. When the line is not active (-P) TAU 2 considers it as being low density. The timing relationships for both 729 II operation and 729 IV operation at either density are shown in Figures 4.2-1 and 4.2-2.

Since the physical speed of the tape is not changed in dual density operation, the millisecond control oscillator for each TAU 2 remains the same.

The hi lo density trigger in the tape unit is also controlled by a pushbutton on the tape unit, allowing an operator manual control of either density operation. The density status trigger in the tape unit is always reset to high density when power is applied.

4.1.09 Rewind and Rewind Unload

TAU can control a tape unit for two separate rewind operations. One is a normal rewind operation that rewinds the tape back to its load point. The tape is left loaded and will be ready for any further operation. Rewind unload is the second type of rewind that can be initiated by TAU control. The rewind unload is identical to the normal rewind with one exception. While the normal rewind is completed when the tape reaches load point, the rewind unload operation is not completed until the tape reaches load point and is unloaded. Figure 4.1-9 is the flow diagram of both operations.

Normal Rewind

If TAU is busy or the tape unit is at load point when the "rewind call" signal is received from the external system, no action will be initiated. If the tape is not at load point and TAU is not busy, the rewind call signal will turn on the rewind trigger. Since a rewind is tape movement in a backward direction, the tape unit must be in read status. If it is, a rewind control line is sent to the tape unit and initiates the rewind action. As soon as

the tape unit is in rewind, it returns the control line, sel and rewind, which resets the rewind trigger. Even though the tape may be rewinding, the TAU operation is completed as soon as the tape unit is in rewind status.

If the unit is in write status when the rewind call is received, TAU must first set the tape unit to read status before the rewind can be initiated. Because of noise deposited on tape when changing from write to read status, the tape is first moved forward in write status before setting read status. With the rewind trigger on in TAU and the "sel and write" line active from the tape unit, TAU starts a millisecond delay counter to control the forward movement of the tape. As in the backspace operation, the delay counter output D-0 turns on the go trigger, starting the tape moving. The tape continues moving until the delay counter output D-50 becomes active and resets go, stopping the tape. The tape has been moved forward and stopped. When the delay counter trigger DC-64 comes on, read status will be set in the tape unit. As soon as the tape unit is in read status, the control line sel and rd from the tape unit allows the output of the rewind trigger to initiate a rewind in the tape unit. As mentioned before, as soon as the tape unit is in rewind status, the rewind trigger and delay counter are reset. The TAU operation is complete.

Rewind Unload

Unconditionally, on receiving the "rewind unload call" signal from an external system, the rewind unload trigger is turned on in the TAU. The rewind unload trigger output duplicates a normal rewind in addition to unloading the tape unit when the rewind is finished. If the tape unit is in read status, the rewind control line becomes active in the tape unit as soon as the rewind unload trigger comes on in the TAU. As soon as the tape unit goes into rewind status, the control line "sel and rewind" is sent to the TAU and resets the rewind unload trigger. If the tape unit is at load point when rewind unload is sent to the tape unit, the tape unit controls will ignore the rewind and simply unload the tape. In either case "sel and rewind" becomes active from the tape unit and resets the rewind unload trigger.

Another condition exists if the tape unit is in write status when the rewind unload signal is received. Until the tape unit is set into read status, the rewind unload control line cannot become active to the tape unit. As in the case of backspace or a normal rewind, the tape must be moved forward before read status can be set. Again, this is because of the status change noise that is deposited on tape when changing from write to read status. To set up the controls for moving tape forward, the rewind unload trigger turns on the rewind trigger. As explained previously, the rewind trigger causes the delay counter to move the tape forward if it is in write status. A delay counter output also sets the tape unit in read status after the tape has moved forward. Once read status is set in the tape unit, the rewind unload control line becomes active to the tape unit and starts the operation. As soon as the tape unit is in rewind status, "sel and rewind" from the tape unit resets the rewind unload trigger, the rewind trigger, and the delay counter. The normal "rewind control" line is prevented from becoming active by the rewind unload operation. The rewind trigger in a rewind unload operation is used only to move the tape forward and to set read status.

5.0.00 DIAGNOSTIC CONTROLS (TAU 1 AND TAU 2)

The following lines have been incorporated in TAU for use in an external test panel. The lines are used as a diagnostic test of TAU and are controlled from the external system.

1. +N Early Sample (Gated to error trigger).
   a. Advances turn on of skew gate tgr by one read count in read and write operations.

2. +P Amplifier Bias
   a. Read only, read register acceptance. Levels switch to write acceptance.
   b. Read while write, read register acceptance. Levels switch to read acceptance.

3. +P Compare Check (Gated to error trigger)
   a. Read only, compare "A" register with "B" register.

4. +P "A" register only.
   a. Read only, force "A" register gate to read write register.

5. +P "B" register only
   a. Read only, force "B" register gate to read write register.

6. -P Manual Stop on Error
   a. Causes Busy Signal preventing next operation.

7. Skew Gate (Read only)
   a. Turned on with early sample at RC6.
   b. Checks skew within character by shortening time allotted to receive one character.
   c. Skew check indicates abnormal skew condition on character read.
   d. VRC only could be skew or drop-out of bits.
   e. Skew and VRC differentiates between possible drop of bits and abnormal skew. With skew check present it indicates definite abnormal skew.

8. Allow A register VRC trigger to function during A only and prevent it from functioning during B only.